1.1 kW 48 V to 12 V zero-voltage switching switched capacitor converter (ZSC) with XDPP1100 controller

REF_1100W_4TO1_ZSC_QB

About this document

Scope and purpose

This document presents the design and performance of a highly efficient 1.1 kW zero-voltage switching (ZVS) switched capacitor converter (SCC), ZSC for short, for 48 V intermediate bus converter applications. The reference board has an input voltage range of 40 to 60 V DC and output voltage range of 10 to 15 V DC, achieving a power density of 564 W/in^3 (34.6 W/cm^3) and 97.3 percent peak efficiency. The board is capable of 90 A output current with 1000 LFM airflow at room temperature. A higher power level is attainable if heatsinks are mounted.

The ZSC quarter-brick converter incorporates an e-fuse with OptiMOS™ 5 80 V linear FET (IPT013N08NM5LF) with a wide safe operating area (SOA) and 1.3 mΩ on-resistance, two high-side switches that require high voltage rating with OptiMOS™ 6 40 V source-down MOSFET (IQE013N04LM6), and the remaining two high-side switches and all three half-bridge synchronous rectifiers with OptiMOS™ 5 25 V MOSFET (BSZ011NE2LS5I). The superior characteristics of Infineon's power transistors result in very low losses and hence enable high power capability with high efficiency and power density. All MOSFETs are driven by EiceDRIVER™ gate driver 2EDB7259E. Infineon's digital power controller XDPP1100-Q024, the industry's smallest digital controller with PMBus interface, is used in the design, providing the utmost flexibility in efficiency optimization, soft-start implementation and enhanced protection.

The reference board follows the standard DOSA mechanical outline for high-current quarter-bricks. It is designed as a testing platform, with easy access to probe test points, and easy reworking/replacement of components.

Intended audience

Power supply design engineers

Reference board/kit

Product(s) embedded on a PCB with a focus on specific applications and defined use cases that may include software. PCB and auxiliary circuits are optimized for the requirements of the target application.

Note: *Boards do not necessarily meet safety, EMI and quality standards (for example UL, CE) requirements.*

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Safety precautions

Note: Please note the following warnings regarding the hazards associated with development systems.

Table 1 Safety precautions

	**Warning:** *The evaluation or reference board contains DC bus capacitors, which take time to discharge after removal of the main supply. Before working on the system, wait five minutes for capacitors to discharge to safe voltage levels. Failure to do so may result in personal injury or death. Darkened display LEDs are not an indication that capacitors have discharged to safe voltage levels.*
	**Caution:** *The device surfaces of the evaluation or reference board may become hot during testing. Hence, necessary precautions are required while handling the board. Failure to comply may cause injury.*
	**Caution:** *The evaluation or reference board contains parts and assemblies sensitive to electrostatic discharge (ESD). Electrostatic control precautions are required when installing, testing, servicing or repairing the assembly. Component damage may result if ESD control procedures are not followed. If you are not familiar with electrostatic control procedures, refer to the applicable ESD protection handbooks and guidelines.*

Table of contents

1 Introduction and ZSC operating principle

ZSC is an Infineon proprietary converter, based on the Dickson converter. It utilizes loop parasitic inductance to achieve LC resonant operation, reducing high inrush current during charge transfer. In theory, optimum efficiency occurs when the switching frequency of the system matches the LC resonant frequency, since all FETs are naturally switching at zero voltage and zero current. However, perfectly matching the frequencies is impossible.

A small external inductor is added to control the current in the network when MOSFETs switch, thus aiding in zero-voltage turn-on of all switches. This ZVS inductor only carries low AC current, and guarantees ZVS instead of relying on perfect matching between LC resonant frequency and switching frequency. Therefore, this topology is not susceptible to component value tolerances and variations.

1.1 ZSC 4:1 topology

The schematic of the ZSC 4:1 topology is shown in Figure 1. L_{R1} and L_{R2} represent parasitic loop inductance that achieves soft charging of the resonant capacitors. L_{ZVS} is the added external inductor, providing the current to discharge C_{OSS} of FETs and hence realizing ZVS in all switches.

Two pulse-width modulated (PWM) signals PWM1 and PWM2 are complementary with close to 50 percent duty cycle. PWM1 is applied to Q1, Q3, Q5, Q8 and Q9 (highlighted in red in Figure 1) and PWM2 for Q2, Q4, Q6, Q7 and Q10 (highlighted blue in Figure 1). The voltage conversion ratio $V_{OUT} = ¼\ V_{IN}$. In steady-state, the voltages across the capacitors are: $V_{CR2} = ¼\ V_{IN}$, $V_{Cfly} = ½\ V_{IN}$, and $V_{CR1} = ¾\ V_{IN}$. The voltage stress of the switches is V_{OUT}, except for Q2 and Q3, which is $2 \times V_{OUT}$.

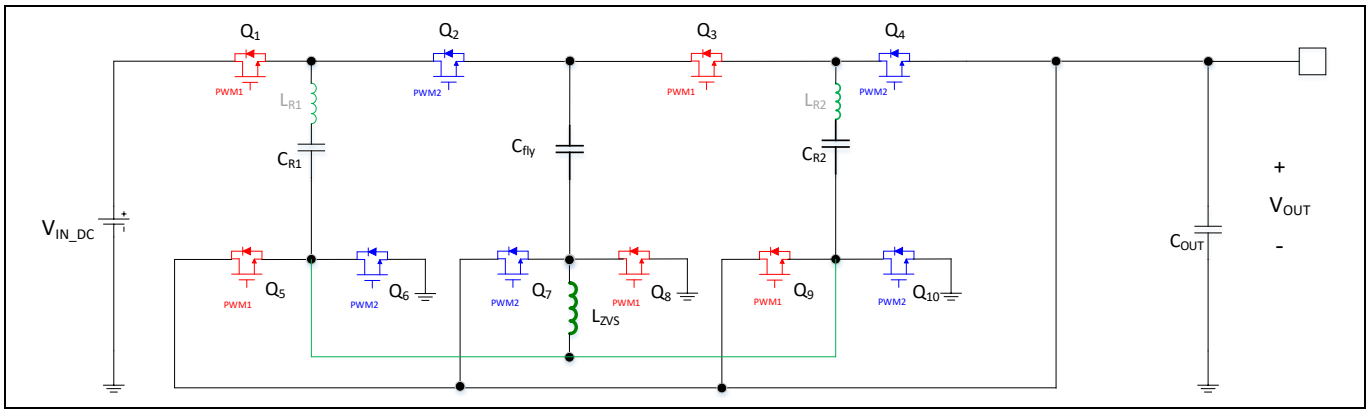

Figure 1 Simplified schematic of the ZSC 4:1 topology

1.2 Resonant tank

There are two resonant tanks: one formed with C_{R1} and L_{R1}, and the other one with C_{R2} and L_{R2}. During operation, the capacitors in these tanks get charged when PWM1 is active (high), and get discharged when PWM2 is active (high). This results in two modes: charging mode and discharging mode. Note that Q5 and Q9 are effectively in parallel in the equivalent circuit, as are Q6 and Q10.

In charging mode, shown in Figure 2, there are two charging paths: first, C_{R1} is charged from input power supply, delivering power to the load. Meanwhile C_{fly} is discharging and C_{R2} is charged up, while power is also transferred to the load.

In discharging mode, shown in Figure 3, C_{R1} discharges the stored energy and charges up C_{fly}, delivering power to the load, and C_{R2} discharges the stored energy to the load.

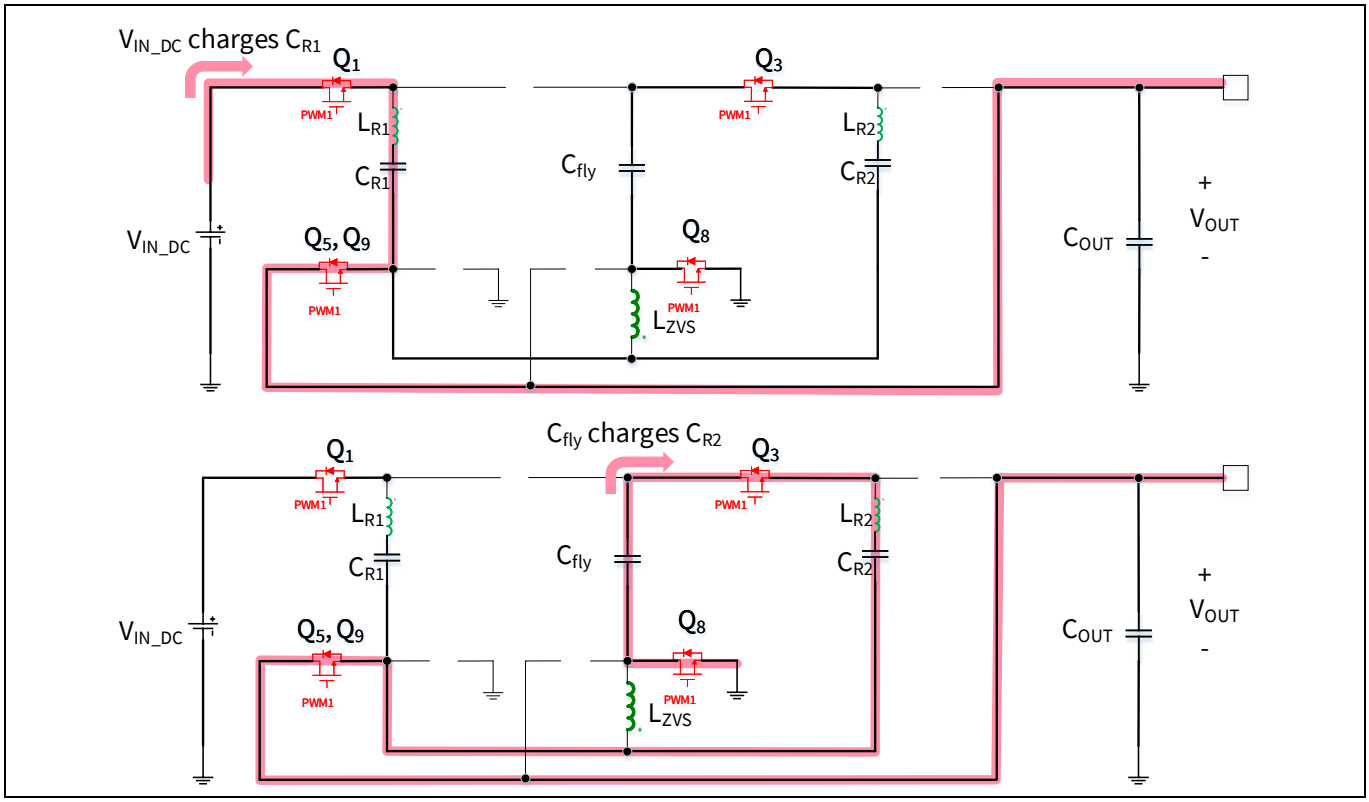

Figure 2 **Charging mode: Cr1 is charged from V_{IN} (top); and Cr2 charged from C_{fly} (bottom)**

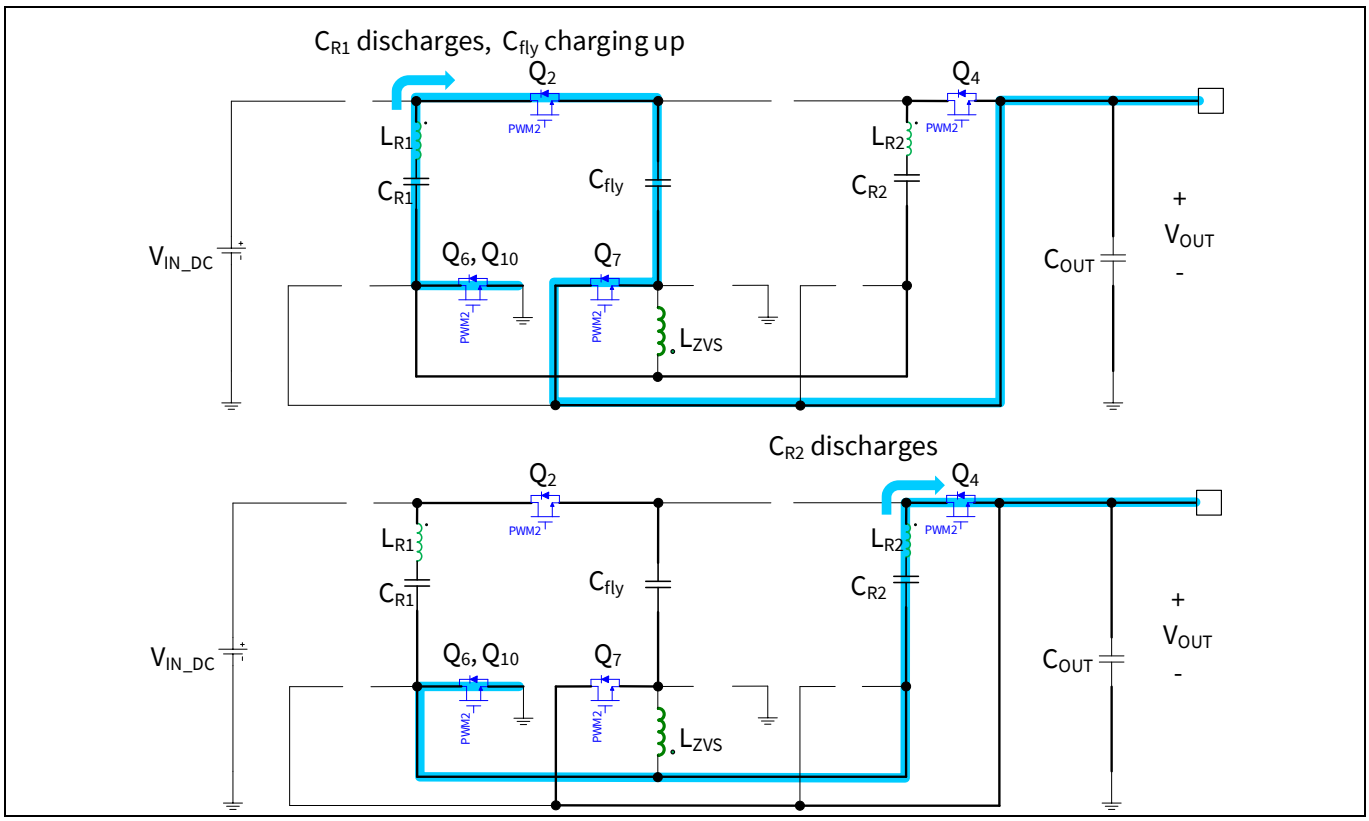

Figure 3 **Discharging mode: Cr1 discharges while charging up C_{fly} (top); and Cr2 discharges (bottom)**

1.3 Switching frequency for unmatched resonant tank

A perfectly matched resonant tank in this ZSC 4:1 topology means that both resonant tanks (C_{R1} and L_{R1}, C_{R2} and L_{R2}) need to have the same resonant frequency f_{RES}. However, component tolerances and variations of the parasitic will always lead to different resonant frequencies. Therefore, the switching frequency f_S will be either higher (over-resonant, f_S greater than f_{RES}) or lower (under-resonant, f_S less than f_{RES}).

It is better to operate over-resonant, as the MOSFETs switch off before the sinusoidal resonant current reaches 0 A. The RMS current is lower compared to under-resonant, and the efficiency will still be high.

1.4 Soft start requirement

When the converter is in the off-state with all capacitor voltages at 0 V, Q1 MOSFET is exposed directly to V_{IN}, which is above the voltage rating. Therefore, soft-start circuitry is required to ramp up V_{IN}, during which time the converter is operating so that V_{OUT} = ¼ V_{IN} is maintained at all times.

Available options include an input buck regulator, as well as e-fuse and hot-swap controllers.

2 The board at a glance

A picture of the 4:1 ZSC quarter-brick reference design is shown in Figure 4. The 3D rendering of the PCB is shown in Figure 5.

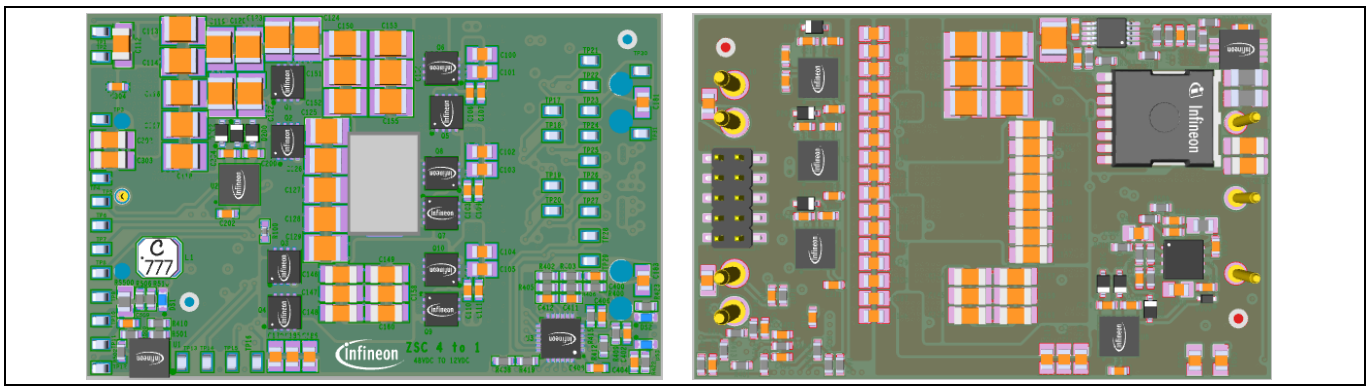

Figure 4 Top and bottom side of the 4:1 ZSC quarter-brick

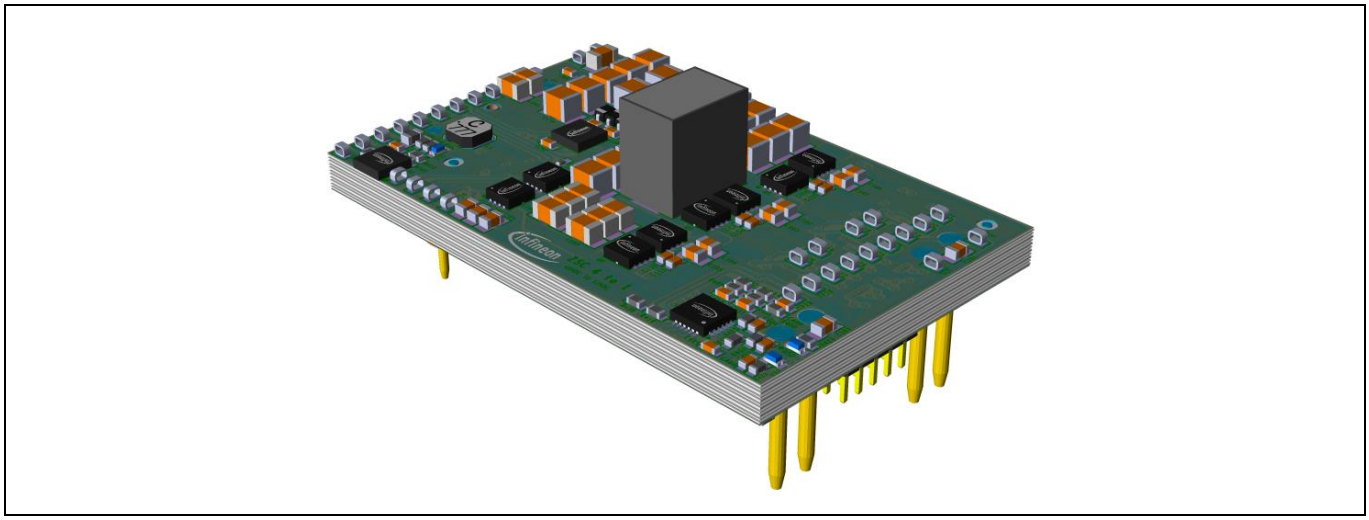

Figure 5 3D PCB view of the 4:1 ZSC quarter-brick

2.1 Main features

- Infineon OptiMOS™ 5 25 V power transistors: BSZ011NE2LS5I, 1.1 mΩ typical in 3.3 x 3.3 mm PQFN package
- Infineon OptiMOS™ 6 40 V power MOSFET: IQE013N04LM6, 1.1 mΩ typical in 3.3 x 3.3 mm PQFN package
- Infineon OptiMOS™ 5 80 V N-channel linear FET: IPT013N08NM5LF, 1.3 mΩ, 330 A in TOLL package
- Infineon 2EDB7259E EiceDRIVER™: functional isolated MOSFET gate driver

2.2 Board parameters and technical data

- Input voltage range: +40 to +60 V DC
- Minimum V_{IN} to turn on: 40 V
- Airflow: 1000 LFM (at maximum output current)
- Protection features: input and output overvoltage, overtemperature and overcurrent

All other board parameters are summarized in Table 2.

Table 2 Parameters and recommended operating conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Minimum input voltage to turn on	VIN_ON		40.0		V	
Output voltage	V_{OUT}		12.0		V	
Output power	P_{OUT}			1100	W	
Output current	I_{OUT}			90	A	
Switching frequency	f_{SW}		600		kHz	
Junction temperature	T_J			125	°C	

3 System and functional description

3.1 Getting started

The ZSC quarter-brick can be mounted on a standard test fixture, as shown in Figure 6. The input and output connections and the on/off switch that controls the EN pin logic level are also highlighted.

Figure 6 ZSC quarter-brick mounted on the test fixture

- Connect the power supply (PSU) and electronic load to the connectors as shown in Figure 6.
- Set the on/off switch to the desired position.
- Make sure there is sufficient airflow.
- Set the input voltage to the desired value above V_{IN_ON}, and turn it on.
- Toggle the on/off switch if desired.

3.2 Description of the functional blocks

Additional details of the board and locations of different functional blocks are shown in Figure 7. The power stage consists of capacitors, MOSFETs and drivers, and the ZVS inductor. The auxiliary supply block includes a switched-mode converter providing 6.5 V, and a linear regulator for 3.3 V. The e-fuse and its controller are on the back of the board.

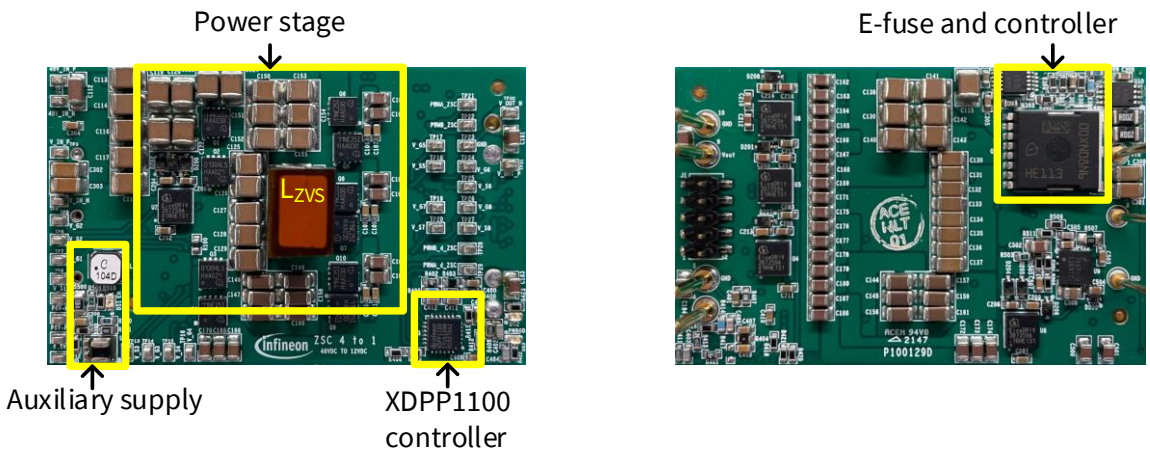

Figure 7 Photo of the ZSC quarter-brick, showing the locations of the power stage, auxiliary supply, controller and e-fuse

3.3 Basic operation

The XDPP1100 controller is factory programmed by default. The board is made ready to operate by following the procedures outlined in Section 3.1.

Caution: *Do not apply high load current during start-up. This could stress the e-fuse and cause possible failure. The controller firmware patch has the option to enable overcurrent protection (OCP) during start-up. It will shut down the converter if high current is detected during start-up.*

3.4 Special operation: programming the controller

When it is necessary to program the XDPP1100 controller, the following steps are recommended.

- Plug in the I^2C communication cable (according to the test fixture documentation).
- Turn on V_{IN} to 34 V. This will enable the auxiliary supply while disabling the e-fuse so that only 6.5 V and 3.3 V are on, while the power stage is off.
- Program the controller as needed.

4 System design

4.1 Schematics

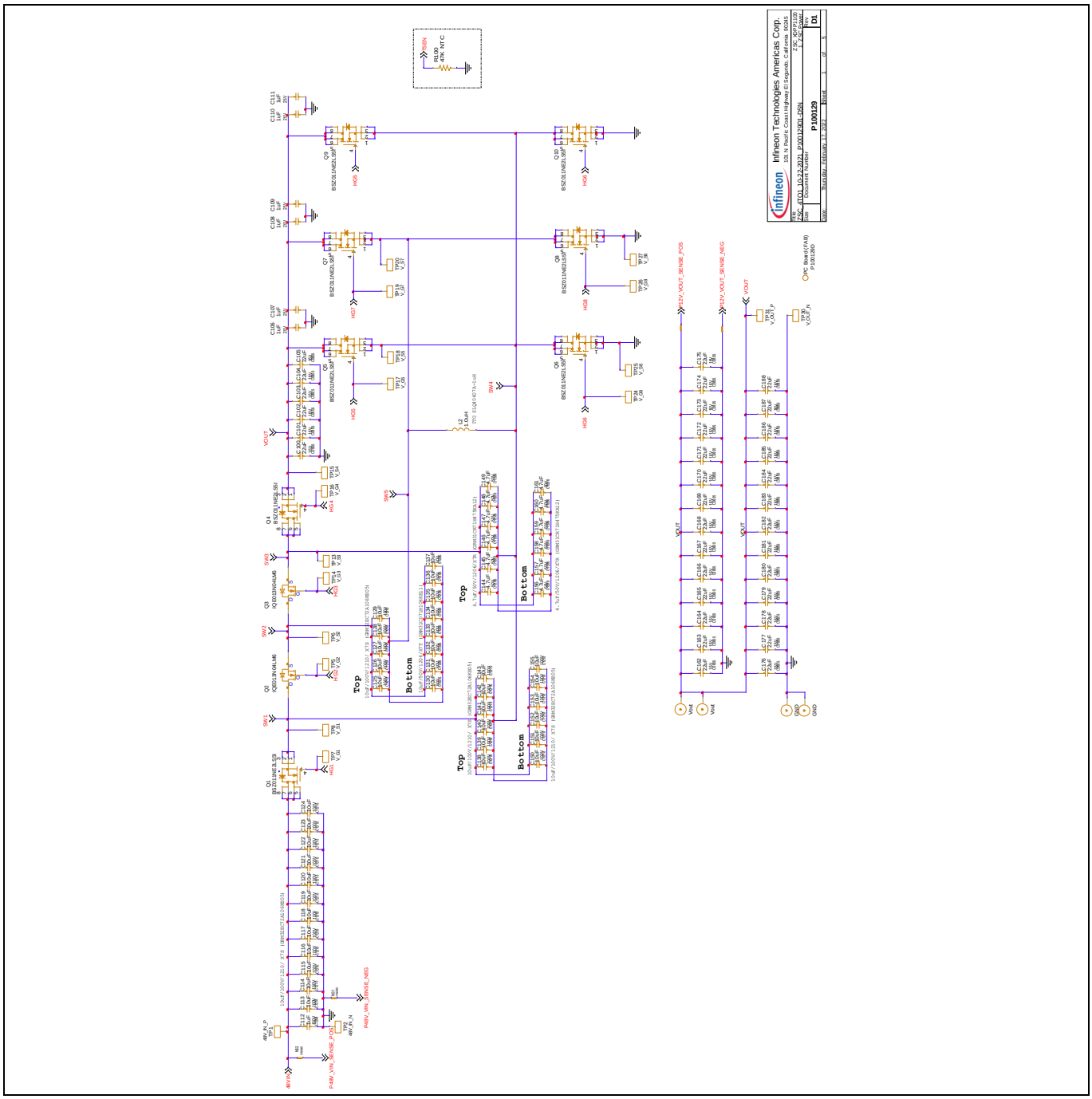

Figure 8 ZSC power stage schematic

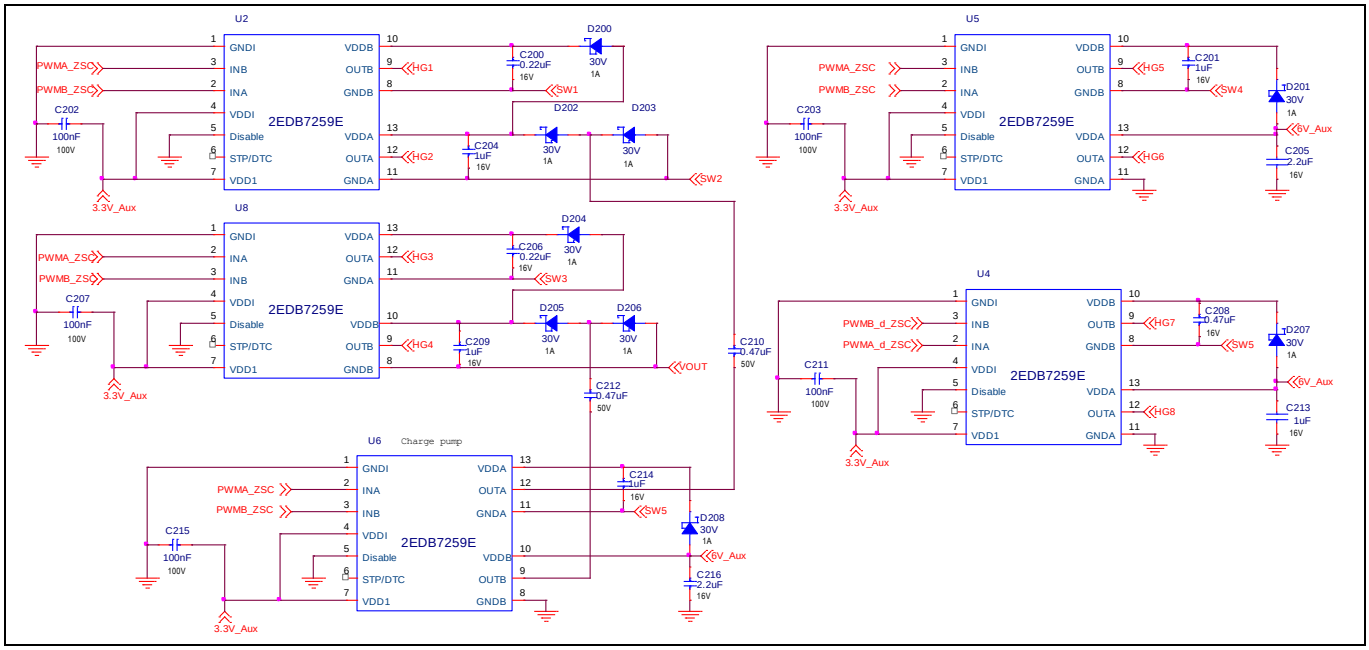

Figure 9 Driver schematic

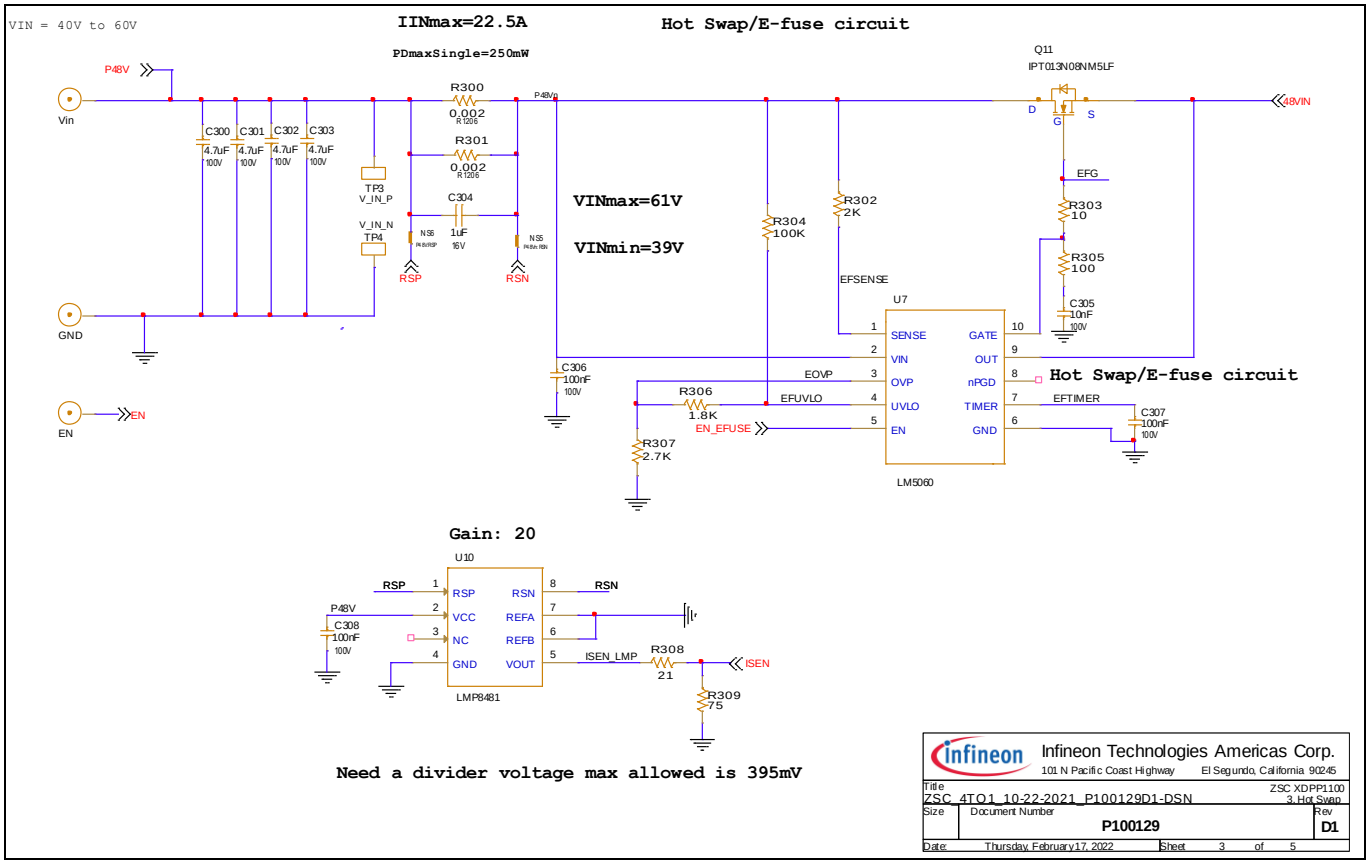

Figure 10 E-fuse hot-swap schematic

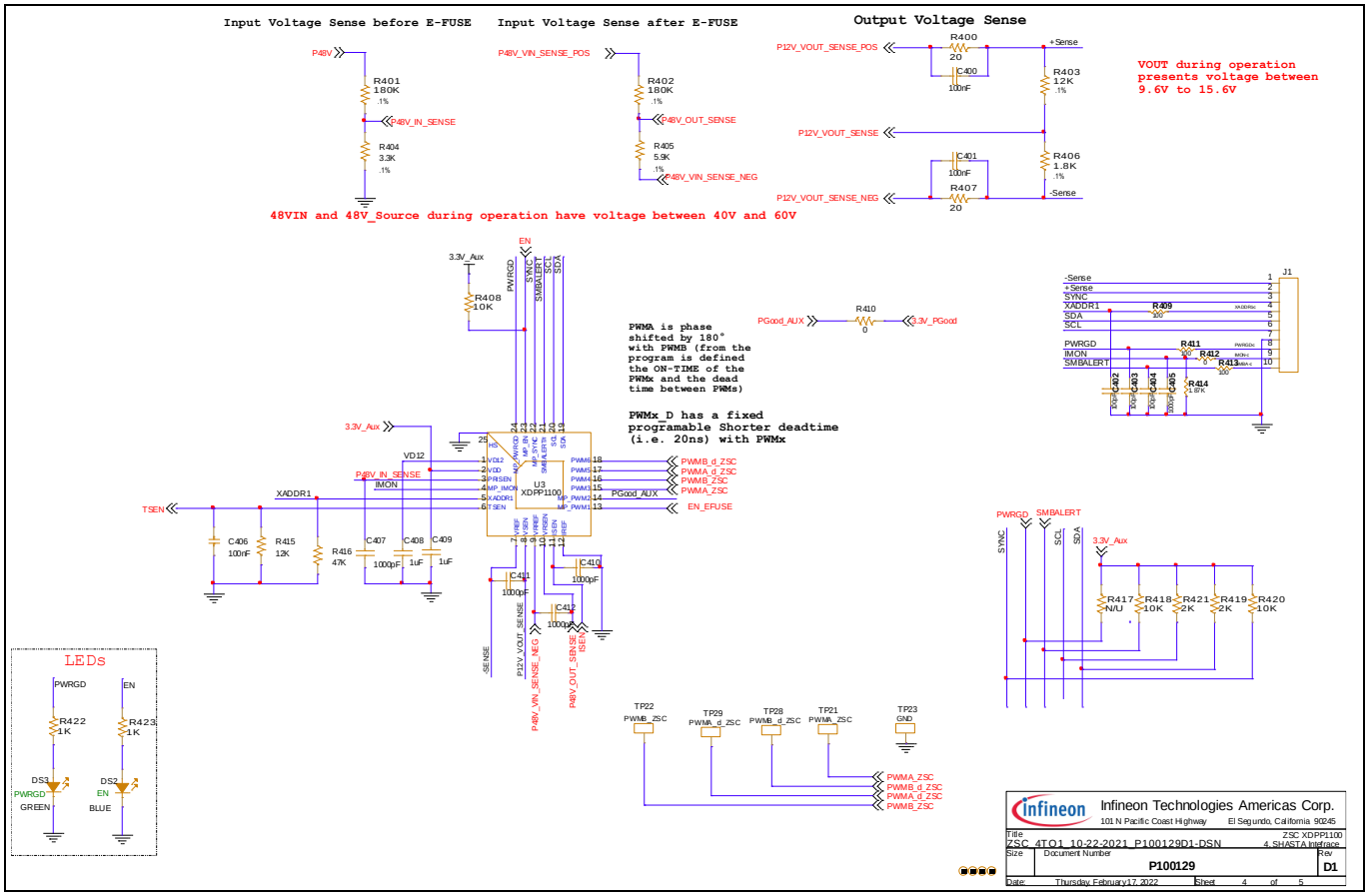

Figure 11 XDPP1100 controller interface schematic

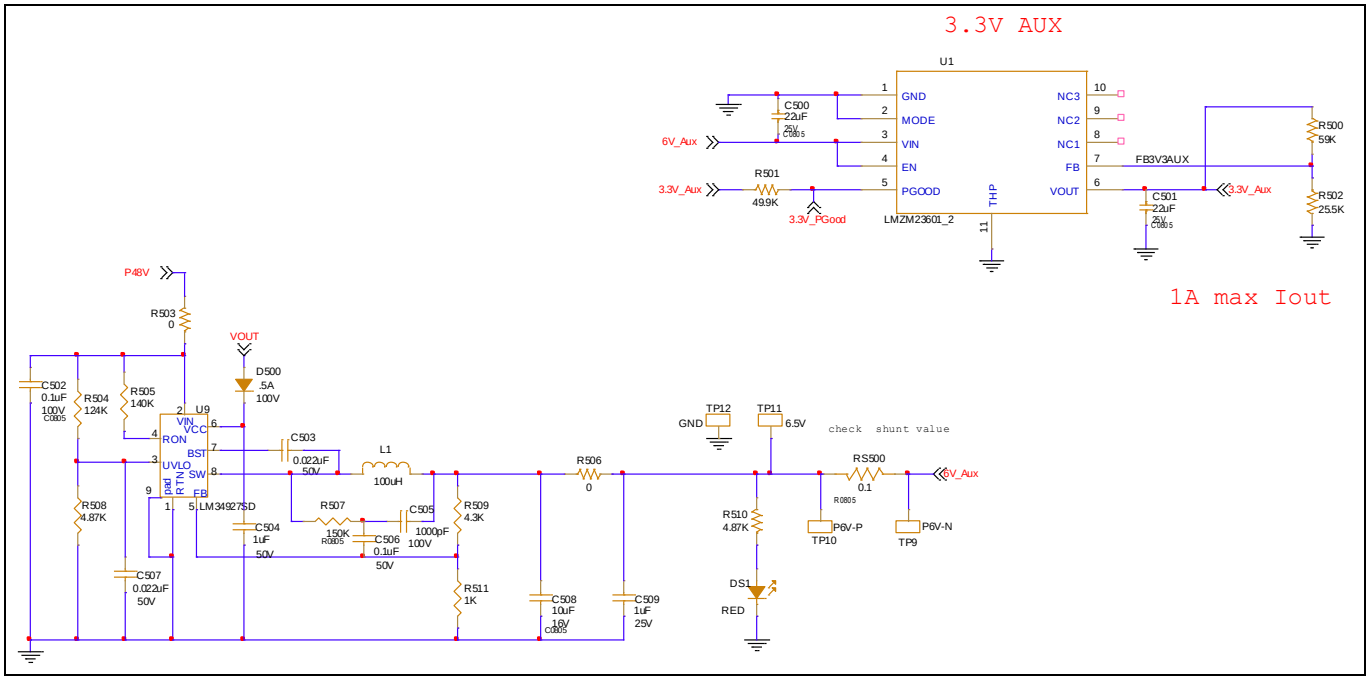

Figure 12 Auxiliary voltage schematic

4.2 Layout guidelines

As explained in Section 1, the resonant inductors Lr1 and Lr2 are realized with parasitic inductances around the loop with no physical inductors. These include:

- PCB inductance (traces, polygons, planes and vias)
- MOSFET inductance (package clips, lead frame, bond wires)
- Capacitor inductance (terminals, MLCC layers)

The main contribution to the loop inductance is the MOSFET. Nevertheless, it is very important to pay attention to the following key points in the PCB layout.

4.2.1 Resonant loop symmetry

It is highly recommended to achieve symmetric resonant loops to minimize resonance mismatch, in turn simplifying the tuning procedure and obtaining optimum performance. This includes symmetrical component placement, symmetrical power planes/polygons and routing, and identical via placement.

4.2.2 ZVS inductor loop

During the dead times, the current in the ZVS inductor continues to flow and discharges C_{oss} of the associated MOSFETs prior to turn-on. This dead time loop is different from the resonant loops.

Keeping the dead time loop small helps to reduce the dead times and improve system efficiency.

4.2.3 Extra clearance between different capacitor nets

To reduce the proximity effect between the flying capacitor and resonant capacitors, it is recommended to have 20 to 40 mils clearance for those associated polygons.

4.2.4 Input and output decoupling capacitors

Input decoupling capacitors should be placed as close to Q1 as possible to stabilize input voltage potential. There should also be enough output bridge capacitors between V_{OUT} and GND power planes to obtain good AC decoupling. This also helps to reduce the loop area in both resonant and dead time intervals.

4.2.5 Equalized trace width

Since the RMS current for resonant loops and flying capacitor loop are similar, it is recommended to have the same total trace width for all current paths.

4.2.6 Gate drive signal routing

Gate drive signal routing should not break any power plane. It is recommended to have a separate gate return trace connected to the source, instead of sharing the power plane connection. In addition, gate drive and its return path should be minimized to reduce parasitic loop inductance. Note that for high-side MOSFETs, the gate drive loop includes the charge pump/bootstrap circuitry.

4.3 Bill of materials

The resonant capacitors are among the most critical part of the design. Besides component tolerance, the values of these ceramic capacitors also change with voltage. Since they have fixed DC bias with small AC ripple, one method of calculating the actual capacitance is using the DC bias characteristics curve from the

manufacturer, as shown in Figure 13. For example, the capacitor used for Cr1 is 100 V rated 10 µF. At 36 V of nominal operating voltage, the actual capacitance drops by 62 percent and is 3.8 µF. The calculation results for all capacitors Cr1, C_{fly} and Cr2 are listed in Table 3. Note that two different capacitors are used for C_{fly}.

Each tank is comprised of many capacitors in parallel. The quantity is determined by the current flowing through each tank. Care must be taken to ensure that the current per capacitor does not exceed the rating.

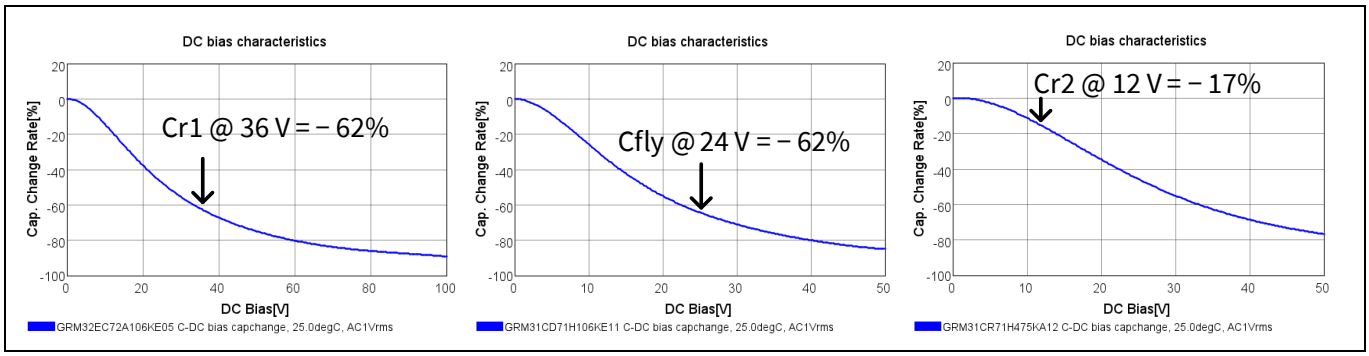

Figure 13 Capacitance change vs. DC bias for Cr1, C_{fly} and Cr2

Table 3 Summary of actual capacitance for Cr1, C_{fly} and Cr2

	Quantity	Description	PN	DC bias [V]	Total C [µF]
Cr1	12	10 µF 100 V	GRM32EC72A106KE05	36	45.6
C_{fly}	5	10 µF 100 V	GRM32EC72A106KE05	24	57.4
	8	10 µF 50 V	GRM31CD71H106KE11	24	
Cr2	12	4.7 µF 50 V	GRM31CR71H475KA12	12	46.81

The complete bill of materials (BOM) is available from the downloads section of the Infineon website. The critical part of the BOM is shown in Table 4.

Table 4 BOM of the critical parts of the ZSC quarter-brick

Item	Ref. designator	Description	Manufacturer	Manufacturer part number
5	C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C127, C128, C129, C138, C139, C140, C141, C142, C143, C150, C151, C152, C153, C154, C155	10 µF 100 V X7S	Murata	GRM32EC72A106KE05L
6	C130, C131, C132, C133, C134, C135, C136, C137	10 µF 50 V X7T	Murata	GRM31CD71H106KE11
7	C144, C145, C146, C147, C148, C149, C156, C157, C158, C159, C160, C161	4.7 µF 50 V X7R	Murata	GRM31CR71H475KA12
32	L2	1.0 µH	ITG	SLQ40407A-1R0MHF
33	Q1, Q4, Q5, Q6, Q7, Q8, Q9, Q10	OptiMOS™ 5 25 V	Infineon	BSZ011NE2LS5IATMA1
34	Q2, Q3	OptiMOS™ 40 V	Infineon	IQE013N04LM6ATMA1
35	Q11	80 V linear FET	Infineon	IPT013N08NM5LF

Item	Ref. designator	Description	Manufacturer	Manufacturer part number
70	U2, U4, U5, U6, U8	2EDB7259E	Infineon	2EDB7259E
71	U3	Digital power controller	Infineon	XDPP1100-Q024

5 XDPP1100 configuration

5.1 E-fuse control

The e-fuse is controlled by pin (13) of XDPP1100, which is mapped to PWM1 by default. Therefore, a patch is required to modify this pin functionality, as well as implementing the soft-start procedure that allows PWMs to be enabled before the e-fuse. Besides timing, there are some other settings for the start-up and shutdown, as described in the following section.

5.2 Start-up and shutdown

Due to the limitation of the e-fuse, the current handling capability is reduced during start-up. Therefore, a different OCP threshold is used during start-up, which is much lower than the steady-state value. Two additional OCP MFR PMBus commands are added: MFR_IOUT_OC_FAULT_LIMIT and MFR_IOUT_OC_WARN_LIMIT, as shown in Table 5.

In addition, high pre-bias voltage on V_{OUT} will also cause voltage stress and start-up issues. Another PMBus command MFR_PREBIAS_THRESHOLD is added so that the converter won't start until the pre-bias is below the set voltage. Finally, during normal shutdown, the PWM stays on until V_{OUT} goes below the voltage defined by MFR_VOUT_OFF_THRESHOLD.

Table 5 Start-up and shutdown MFR commands and settings

Command	Value	Comment
MFR_CONFIG_DELAY	0	
MFR_IOUT_OC_FAULT_LIMIT	0x10	OC fault limit [A] during start-up for e-fuse protection
MFR_IOUT_OC_WARN_LIMIT	0x04	OC warn limit [A] during start-up for e-fuse protection
MFR_PREBIAS_THRESHOLD	0x02	If V_{OUT} is pre-biased above this voltage [V], EN_EFUSE stays low
MFR_VOUT_TARGET	0x0A	Once V_{OUT} is above this voltage [V], OC warn/fault limits are restored to the standard PMBus command values
MFR_VOUT_OFF_THRESHOLD	0x02	During normal shutdown and V_{IN}/V_{OUT} UV fault, PWM stays on until V_{OUT} goes below this voltage [V]

5.3 Flow diagram

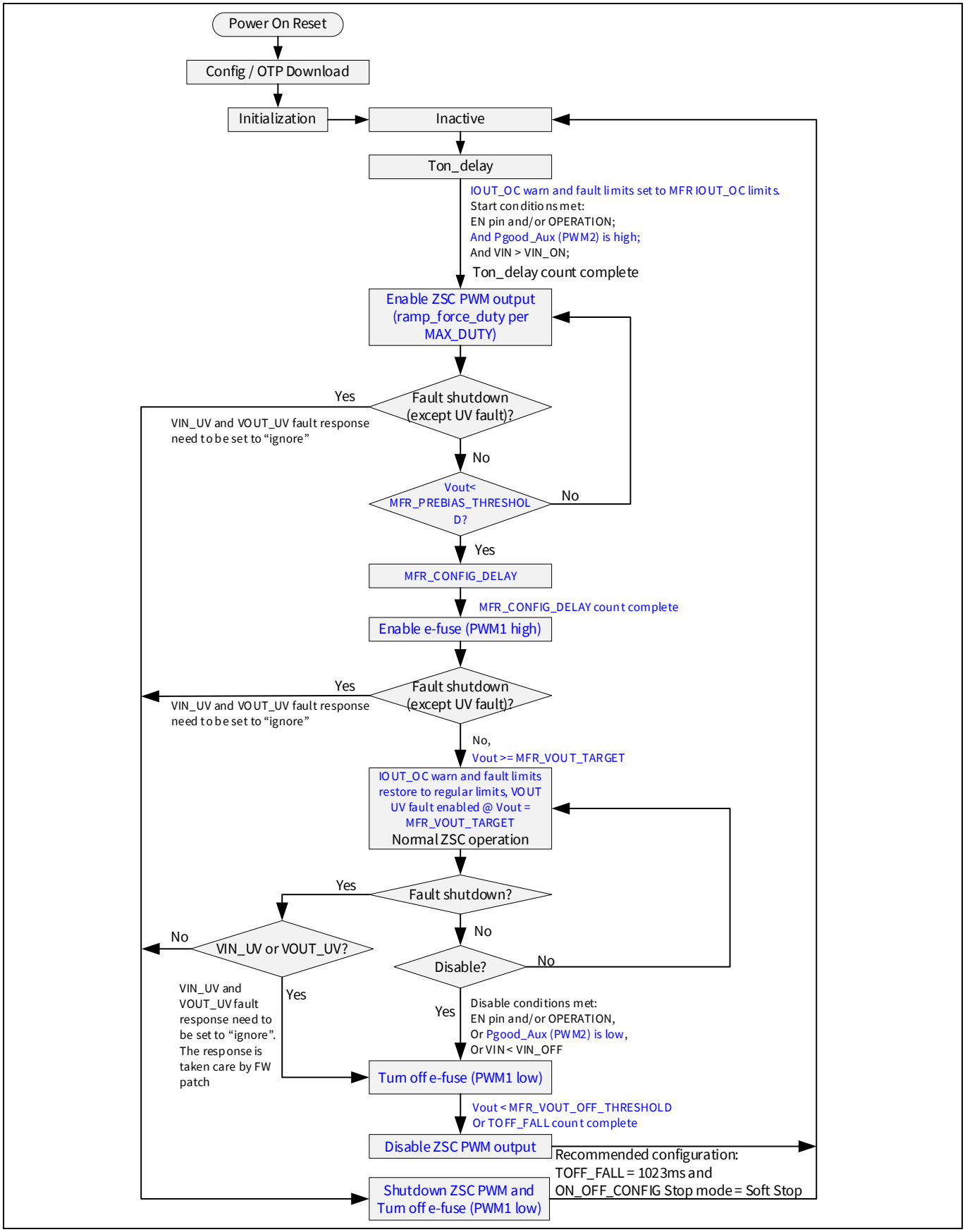

Figure 14 Flow diagram of the patched XDPP1100 for ZSC quarter-brick

6 System performance

6.1 Start-up and shutdown

According to the start-up and shutdown MFR commands in Table 5, during start-up, the e-fuse will not be enabled if V_{OUT} is above the pre-bias threshold. In the example test waveform shown in Figure 15, MFR_PREBIAS_THRESHOLD is set to 1 V. When the output voltage is pre-biased above the threshold, the e-fuse is held off until the pre-bias is lower. If there is no pre-bias condition, the normal start-up sequence is executed.

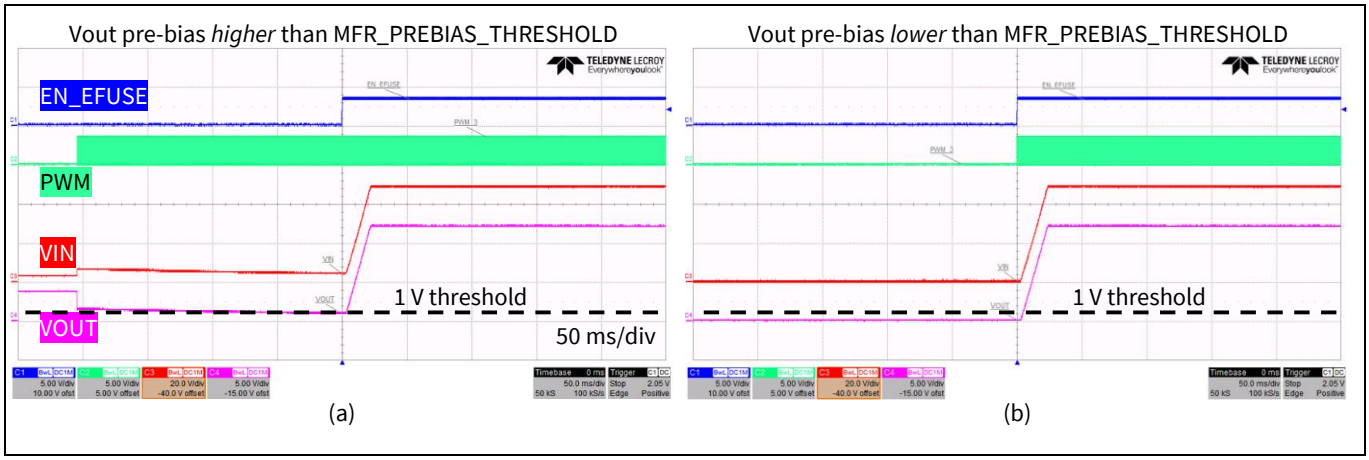

Figure 15 Start-up waveform: (a) V_{OUT} pre-bias higher than threshold and (b) lower than threshold

With TOFF_FALL set to 1023 ms and the stop mode to “Soft Stop” in ON_OFF_CONFIG, the shutdown waveforms are shown in Figure 16. MFR_VOUT_OFF_THRESHOLD is set to 2.

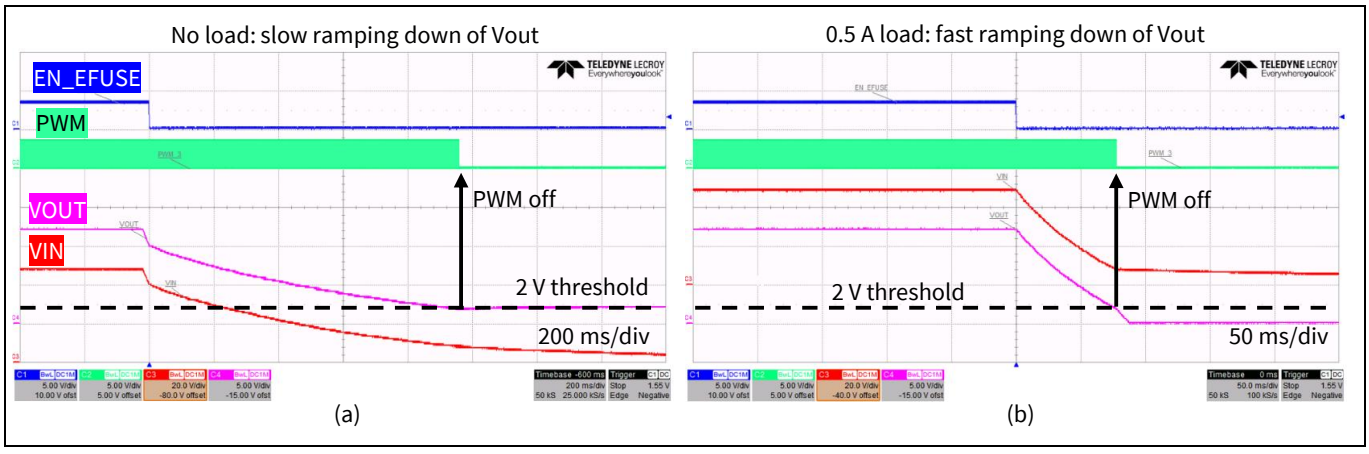

Figure 16 Shutdown waveform: (a) no load and (b) 0.5 A load

6.2 Efficiency and loss

Efficiency and loss are measured at three different input voltages (40 V, 48 V and 60 V). Maximum output power is limited to 1100 W. The results in Figure 17 include losses of the onboard 6.5 V and 3.3 V auxiliary power supply and gate drive power, which is approximately 1.7 W. Figure 18 shows the power stage efficiency and loss, excluding auxiliary power supply and gate drive power.

Note: Efficiencies have been captured with a dwell time of 5 minutes.

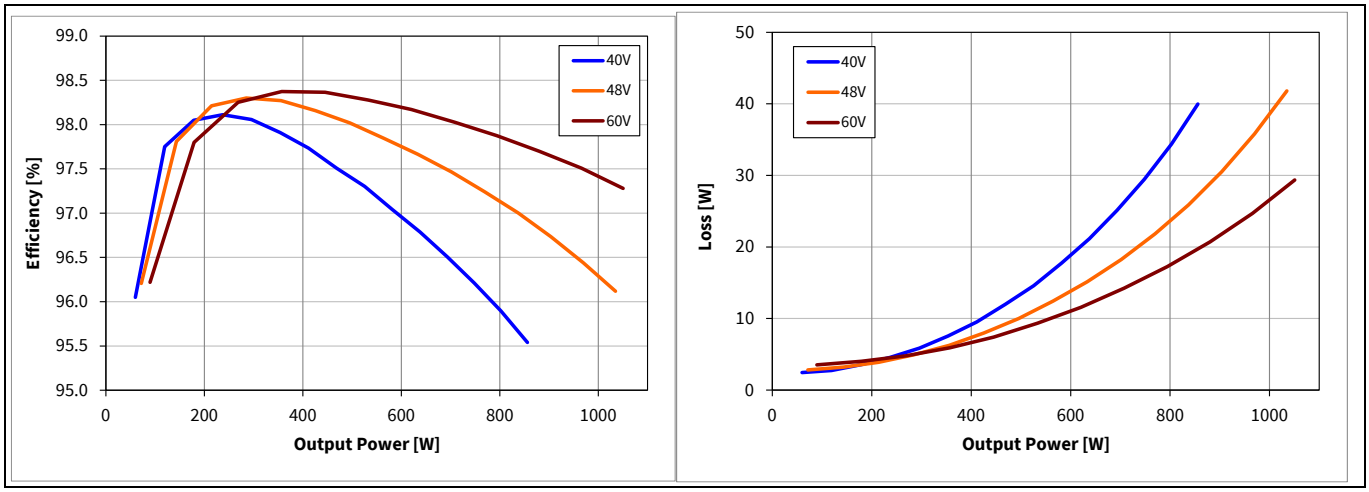

Figure 17 Measured efficiency and loss of the ZSC quarter-brick

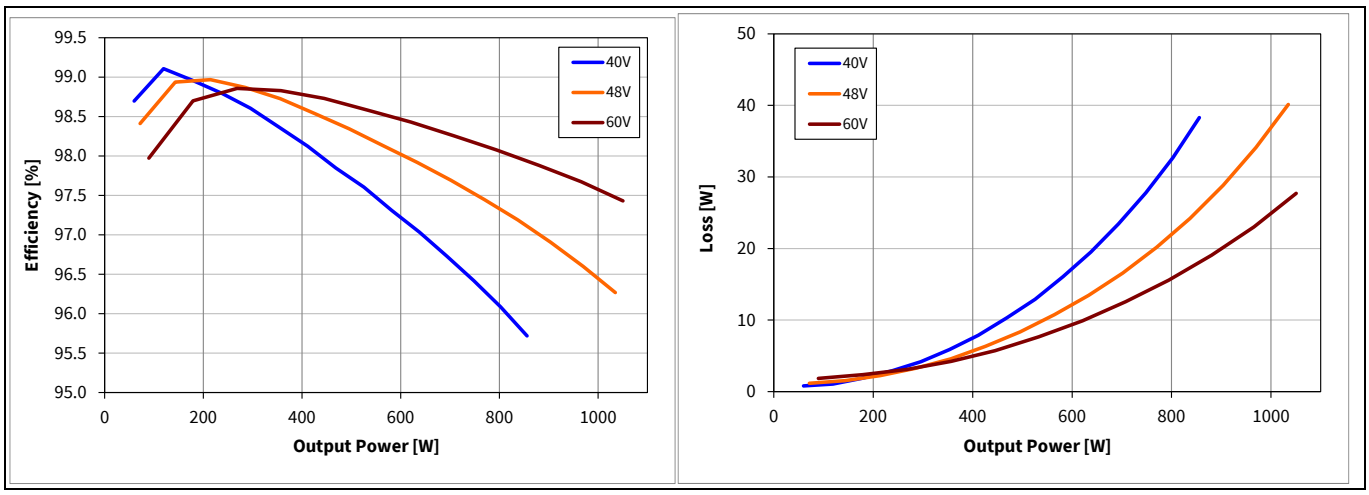

Figure 18 Measured efficiency and loss excluding auxiliary power supply

Note: Measured auxiliary supply power (P_{aux}) is 1.67 W. "Efficiency w/o P_{aux}" in Table 6 through Table 8 is calculated as $P_{OUT}/(P_{IN}-P_{aux})$.

Table 6 Efficiency at 40 V input

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	Efficiency	Efficiency w/o P_{aux}
39.74	22.55	895.99	9.50	90.15	856.02	95.54	95.72
39.79	19.55	777.73	9.58	78.15	748.26	96.21	96.42
39.83	16.55	659.04	9.65	66.11	637.87	96.79	97.03
39.86	13.55	540.07	9.72	54.07	525.50	97.30	97.60
39.89	10.55	420.91	9.79	42.04	411.38	97.73	98.12
39.92	7.55	301.55	9.85	30.02	295.69	98.06	98.60
39.95	4.56	182.03	9.91	18.00	178.48	98.05	98.96
39.98	1.56	62.24	9.98	5.99	59.78	96.05	98.70

Table 7 Efficiency at 48 V input

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	Efficiency	Efficiency w/o P_{aux}
47.74	22.56	1076.73	11.48	90.13	1034.93	96.12	96.27
47.78	19.55	934.32	11.57	78.14	903.80	96.73	96.91
47.82	16.55	791.53	11.64	66.10	769.69	97.24	97.45
47.86	13.55	648.51	11.71	54.07	633.38	97.67	97.92
47.89	10.55	505.32	11.78	42.04	495.32	98.02	98.34
47.92	7.55	361.90	11.85	30.02	355.65	98.27	98.73
47.95	4.55	218.36	11.91	18.00	214.45	98.21	98.97
47.98	1.55	74.59	11.98	5.99	71.76	96.21	98.41

Table 8 Efficiency at 60 V input

V_{IN} [V]	I_{IN} [A]	P_{IN} [W]	V_{OUT} [V]	I_{OUT} [A]	P_{OUT} [W]	Efficiency	Efficiency w/o P_{aux}
59.80	18.06	1079.96	14.58	72.08	1050.59	97.28	97.43
59.82	16.56	990.49	14.62	66.08	965.80	97.51	97.67
59.84	15.06	901.01	14.65	60.07	880.28	97.70	97.88
59.88	12.06	721.87	14.73	48.05	707.63	98.03	98.26
59.91	9.06	542.49	14.80	36.02	533.15	98.28	98.58
59.94	6.05	362.91	14.87	24.01	357.01	98.37	98.83
59.97	3.06	183.26	14.94	11.99	179.23	97.80	98.70
59.98	1.55	93.27	14.98	5.99	89.74	96.22	97.97

6.3 Input overcurrent protection at start-up

Input OCP at start-up is designed to protect the e-fuse at start-up where the inrush current is too high if output loaded at start-up. Referring to the flowchart in Figure 14, after the Ton_delay has elapsed, the IOUT_OC_warn and fault limits are set to MFR_IOUT_OC warn and OC fault limits. These limits are only valid at the start-up of the converter and are lower than the OCP thresholds. Once the converter output voltage goes above MFR_VOUT_TARGET voltage, the IOUT_OC warn and fault limits are set to a regular limit using IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT.

The default IOUT_OC fault (MFR_IOUT_OC_fault) limit is set to 16 A at start-up, which translates to 4 A (4:1 ZSC ratio) of input current, and MFR_VOUT_TARGET is set to 10 V. Tests are performed at three different input voltages (40 V_{IN}, 48 V_{IN} and 60 V_{IN}) to show that input OC limit is not a factor of input voltage.

Test scope channels:

- Channel 1: e-fuse enable (bandwidth 20 Mhz)
- Channel 2: output voltage (V_{OUT}) (BW 20 Mhz)
- Channel 3: input current (I_{IN}) (BW 20 Mhz)
- Channel 4: PWM (TP24) (BW 20 Mhz)

Test condition:

- Current limit of input voltage source is set to 20 A
- Output load is set to 20 A in constant current mode
- Scope is triggered on the falling edge of the e-fuse enable signal at 1.5 V threshold
- Airflow: 1000 LFM

Input voltage applied is 40 V_{IN}.

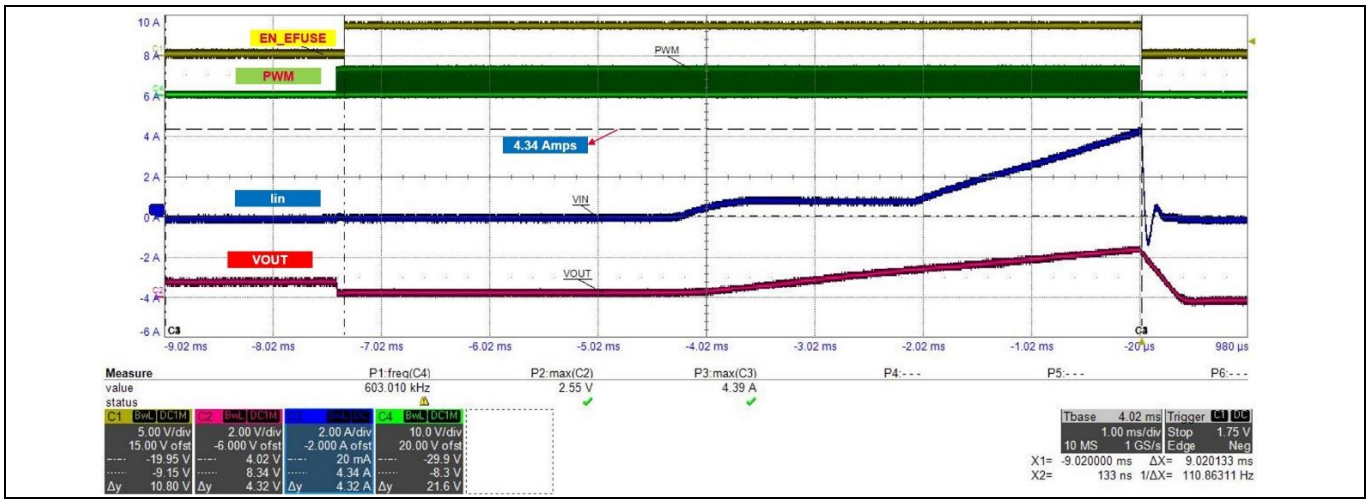

Figure 19 Input OCP at start-up to protect e-fuse at 40 V_{IN}

Input voltage applied is 48 V_{IN}.

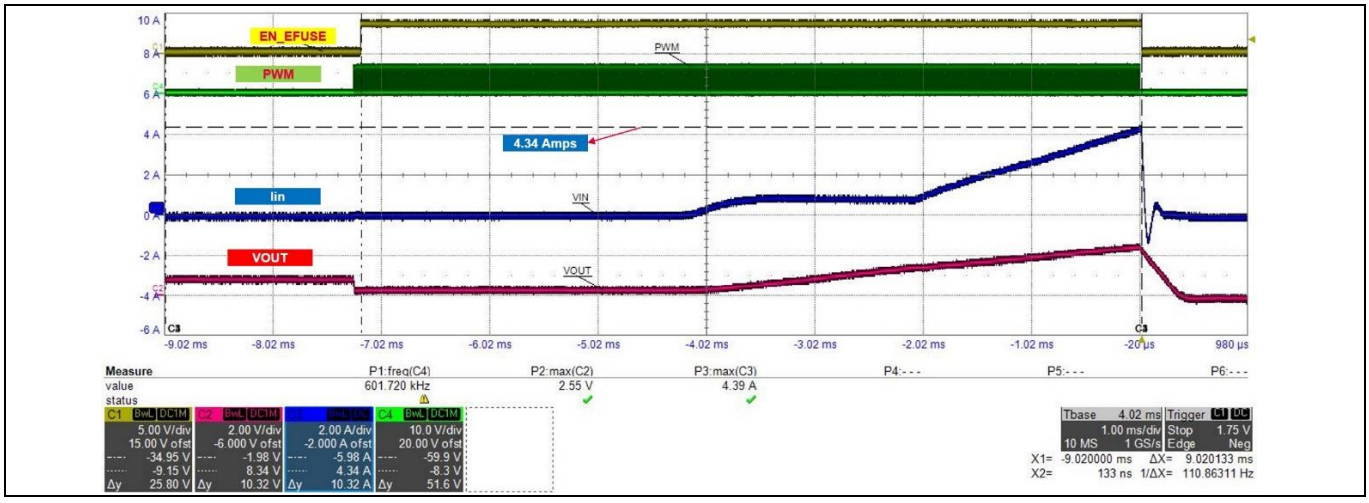

Figure 20 Input OCP at start-up to protect e-fuse at 48 V_{IN}

Input voltage applied is 60 V_{IN}.

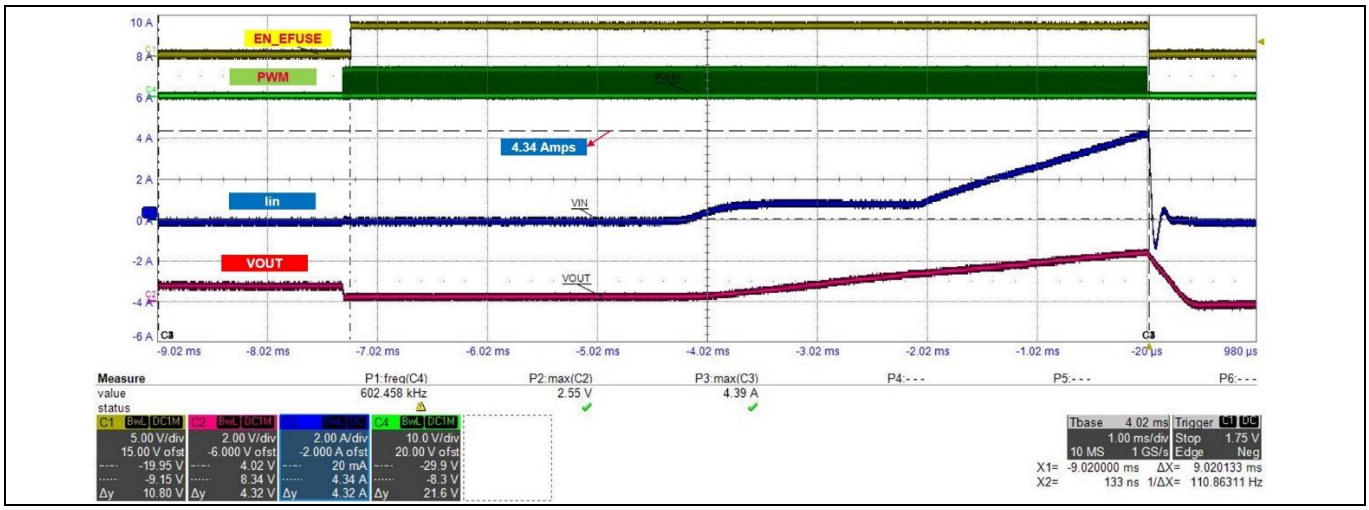

Figure 21 Input OCP at start-up to protect e-fuse at 60 V_{IN}

From Figure 19, Figure 20, and Figure 21, it can be seen that in all three cases, irrespective of input voltage, the start-up input OCP triggers at input current of around 4.34 A, while the output voltage is below the MFR_VOUT_TARGET of 10 V. When OCP triggers, it disables the PWM and the e-fuse enables immediately to protect the e-fuse and latches off.

6.4 Input overvoltage protection

Input OVP has been incorporated to protect input as well as output switches and capacitors from OV stress failures. The default limit of input OVP is set to 65.5 V.

Test scope channels:

- Channel 1: e-fuse enable (BW 20 Mhz)
- Channel 2: output voltage (V_{OUT}) (BW 20 Mhz)
- Channel 3: input current (I_{IN}) (BW 20 Mhz)
- Channel 4: PWM (TP24) (BW 20 Mhz)

Test condition:

- Current limit of input voltage source is set to 20 A
- Input voltage is set to 48 V at turn-on
- No load at the output
- Output OVP has been disabled via PMBus to observe input OVP
- Scope is triggered on the falling edge of the e-fuse enable signal at 1.5 V threshold
- Input voltage is slowly increased to determine the turn-off threshold
- Airflow: 1000 LFM

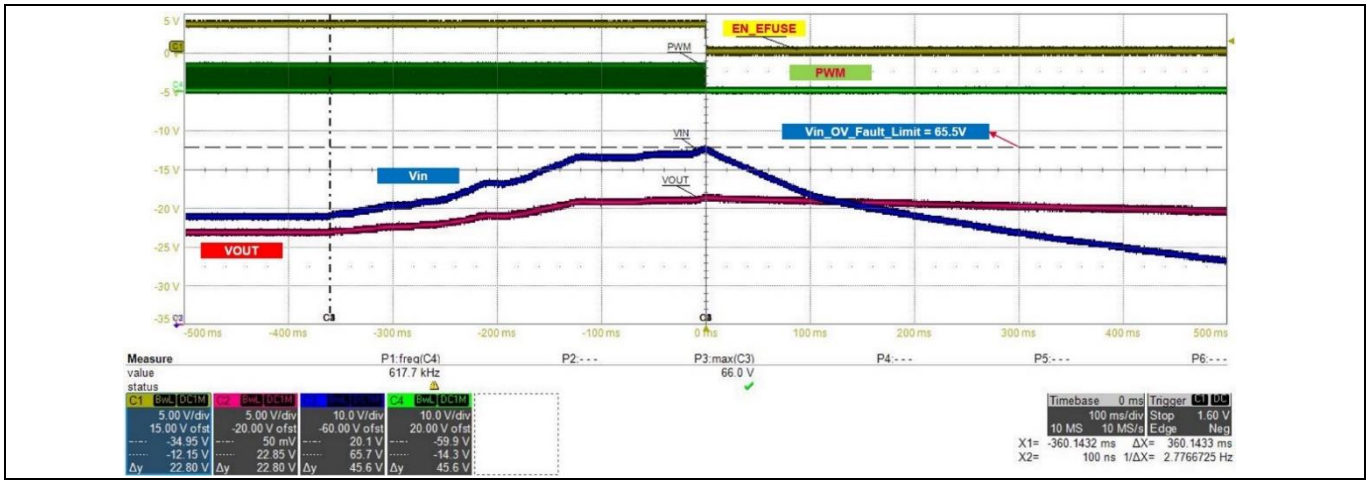

Figure 22 Input OVP trigger

The OVP triggers at an input voltage of V_{IN} = 66 V, as shown in Figure 22. When the input OV fault is detected, the e-fuse enable and PWM signals are disabled and converter is turned off.

6.5 Regular output overcurrent protection

Regular OC fault protection is incorporated to turn off the converter in the event of overload. This detection scheme makes use of a low-pass filter (LPF) before reading samples, which makes it slower compared to the fast OCP discussed in Section 6.6.

Test scope channels:

- Channel 1: e-fuse enable (BW 20 Mhz)
- Channel 2: output voltage (V_{OUT}) (BW 20 Mhz)
- Channel 3: output current (I_{OUT}) (BW 20 Mhz)
- Channel 4: PWM (TP24) (BW 20 Mhz)

Test conditions:

- Current limit of input voltage source set to 30 A
- 48 V of input voltage is applied
- Current limits are modified as follows:
  - IOUT_OC_FAULT_LIMIT = 90 A
  - MFR_IOUT_OC_FAST_FAULT_LIMIT = 95 A
- Output load of 80 A is applied, and then load is increased slowly to trigger OC fault
- Scope is triggered on the falling edge of the e-fuse enable signal at 1.5 V threshold
- Airflow: 1000 LFM

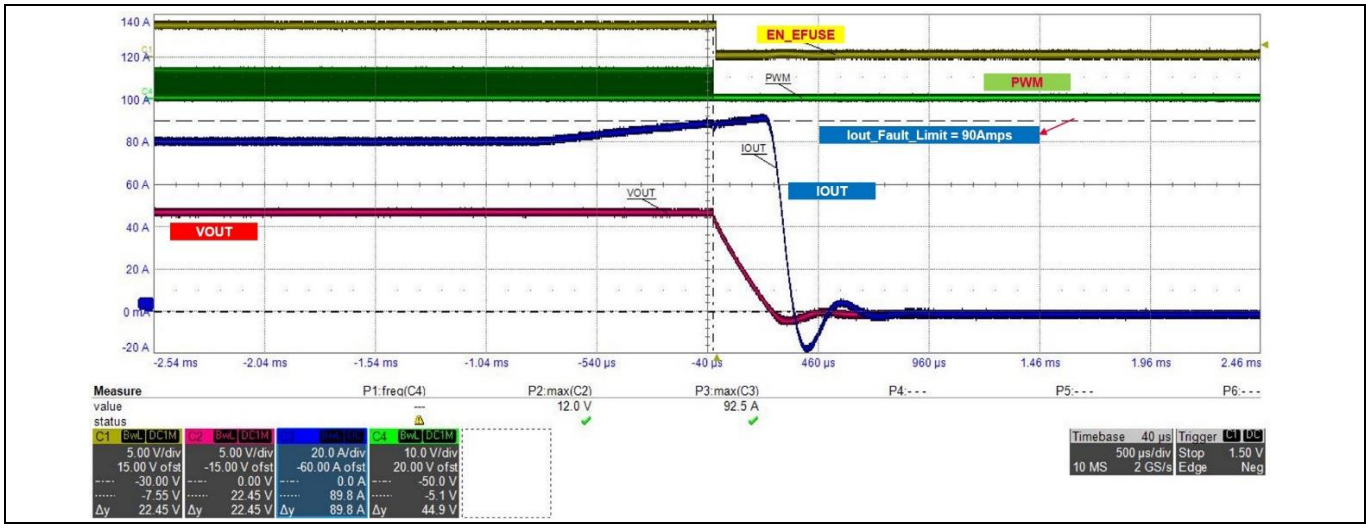

Figure 23 Regular output OCP

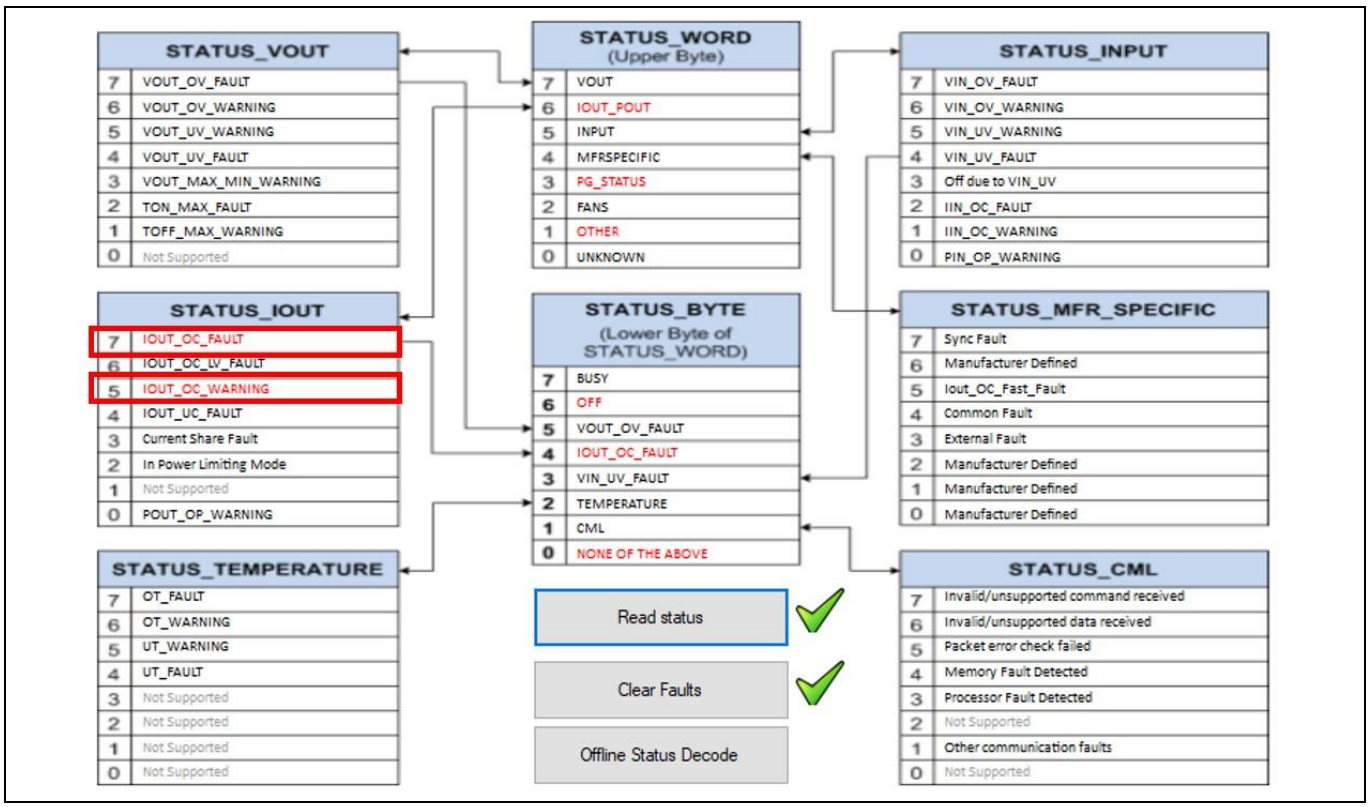

Figure 24 PMBus fault status chart after regular OCP

When the output current crosses the OC threshold of 90 A, the OCP is triggered, which disables the PWM and e-fuse enable signal and raises the IOUT_OC_FAULT fault flag, as shown in Figure 23 and Figure 24.

6.6 Fast output overcurrent protection

Fast output OCP is used for detecting fast faults such as short-circuit. Instead of receiving the samples after the LPF as was the case in regular OCP, the samples come in directly and are averaged out. Thus, more data is read compared to regular OC and the faults are detected more quickly.

Test scope channels:

- Channel 1: e-fuse enable (BW 20 Mhz)
- Channel 2: output current (I_{OUT}) (BW 20 Mhz)
- Channel 3: input current (I_{IN}) (BW 20 Mhz)
- Channel 4: PWM (TP24) (BW 20 Mhz)

Test condition:

- Current limit of input voltage source set to 30 A
- 48 V of input voltage is applied
- Current limits are modified as follows:
  - IOUT_OC_FAULT_LIMIT = 90 A
  - MFR_IOUT_OC_FAST_FAULT_LIMIT = 95 A
- Output load of 75 A is applied, and then the short-circuit fault was initiated on DC load
- Scope is triggered on the falling edge of the e-fuse enable signal at 1.5 V threshold
- Airflow: 1000 LFM

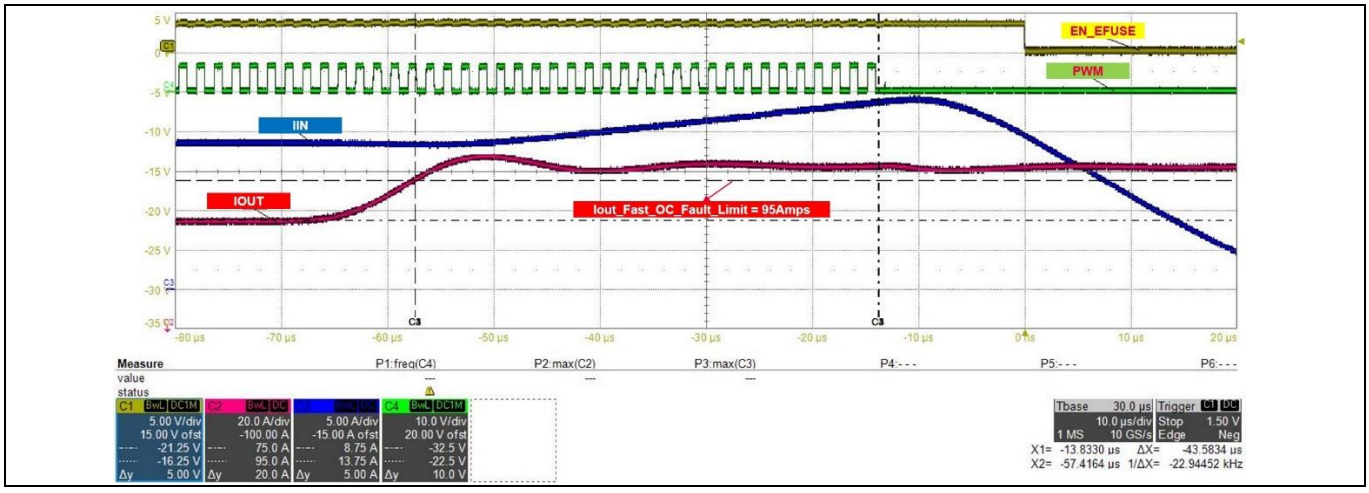

Figure 25 Fast output OCP with output current as y-axis reference

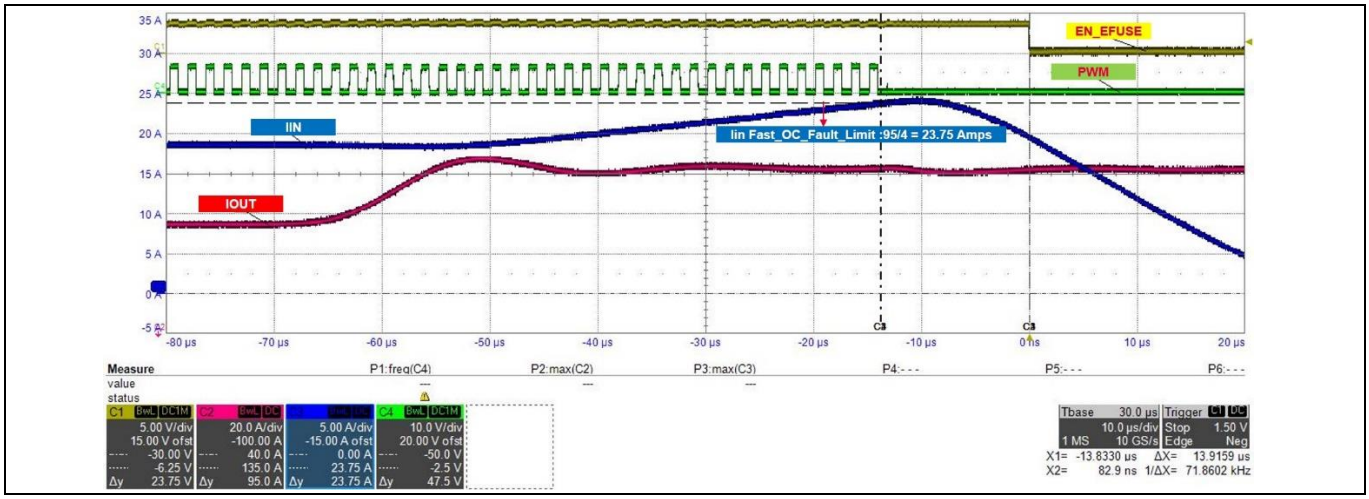

Figure 26 Fast output OCP with input current as y-axis reference

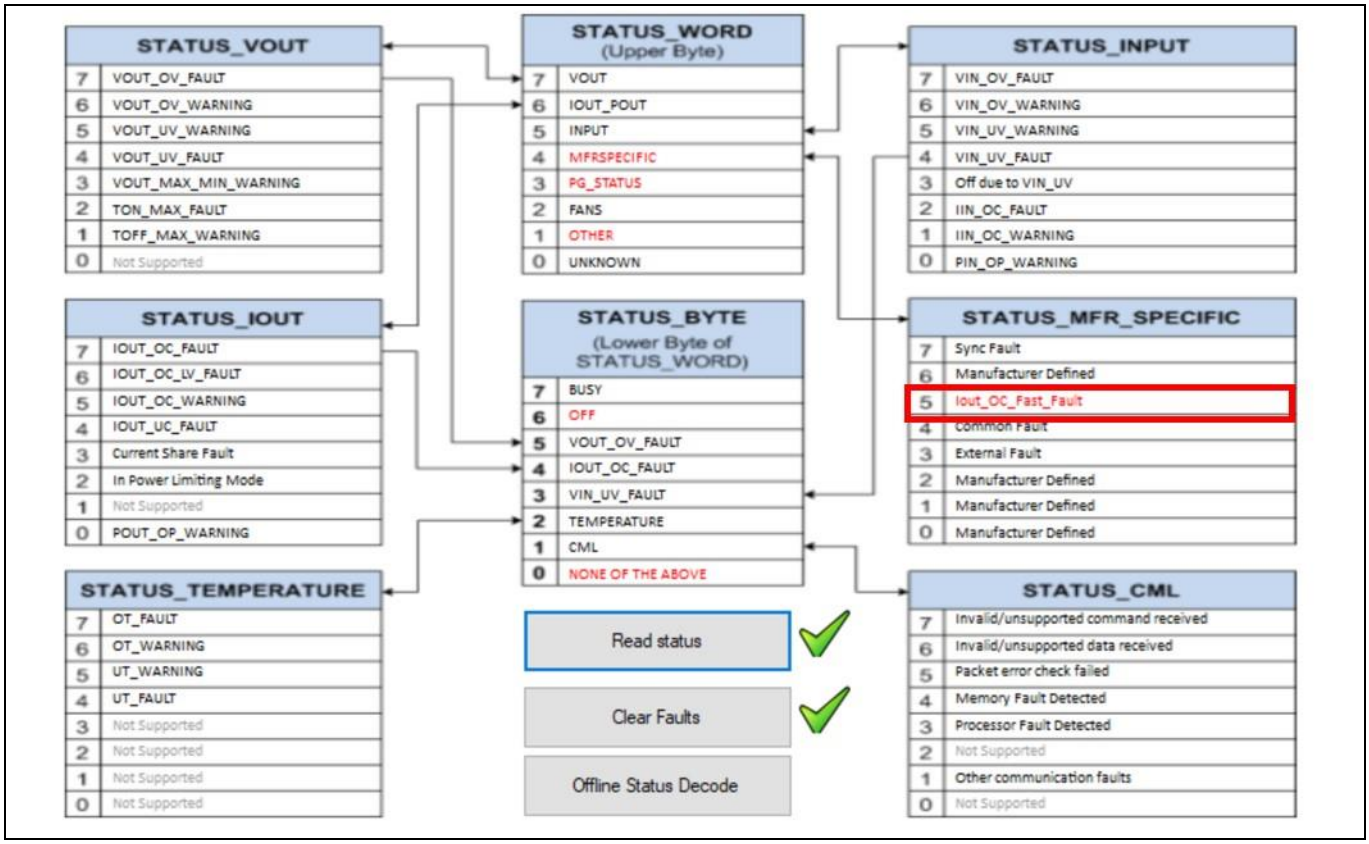

Figure 27 PMBus fault status chart after fast output OCP

Figure 25 is the fast overcurrent protection waveform. It can be seen that there is approximately 44 µs delay between the actual IOUT OC fault and the fault trigger. The XDPP1100 controller measures the input current and translates it to output current by making use of a 4:1 current ratio between output and input of the ZSC. So, the fast fault limit on the input side translates to 95 A/4 = 23.75 A. From Figure 26 it is clear that the fast OCP is triggered instantaneously when the input current exceeds the 23.75 A fault threshold and PWMs are disabled. The 4:1 ratio mismatch between input and output current is because when the short-circuit fault was triggered on the load, the momentary short-circuit current was supplied by the output capacitors instead of being supplied via input source. Analysis of the fault chart in Figure 27 indicates that while the IOUT_OC_FAULT threshold is 90 A the corresponding fault flag is not raised; instead the fast OC fault flag is raised.

6.7 Thermals

Thermal testing was performed on the unit under the following conditions:

- Input voltage: 47.23 V (measured between V_IN_P (TP3) and V_IN_N (TP4))
- Input current: 22.46 A (measured using calibrated current shunt)
- Input power: 1060.86 W
- Output voltage: 11.46 V (measured between V_OUT_P (TP31) and V_OUT_N (TP30))
- Output current: 89.51 A (measured using calibrated current shunt)
- Output power: 1025.93 W
- Efficiency: 96.70 percent (including bias losses)
- Ambient temperature: 25°C
- Airflow: fan operating at 10 V/0.75 A (airflow 1000 LFM)

The unit was put under test for more than 30 minutes under the above-mentioned loading conditions and then the thermal data was recorded using a FLIR camera.

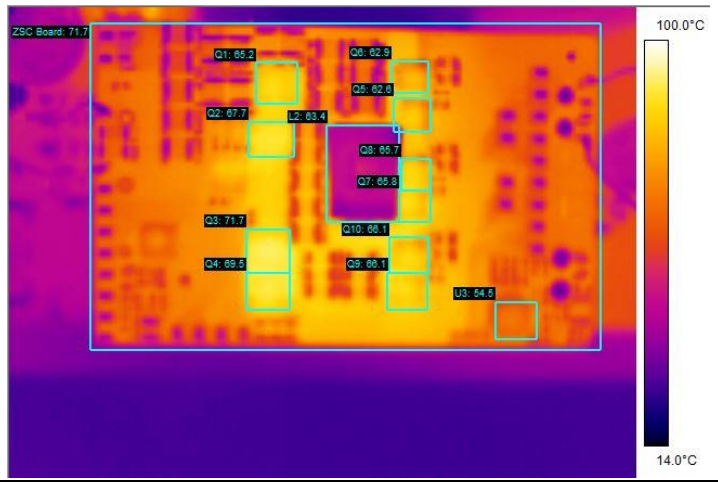

Figure 28 Thermal profile of ZSC (4:1) under full load

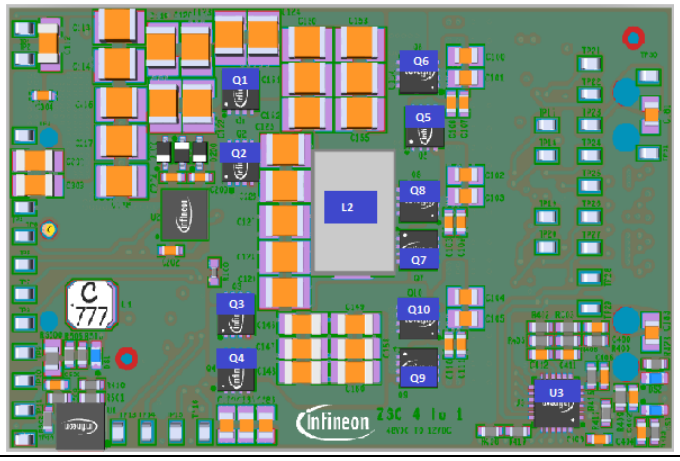

Figure 29 ZSC 4:1 quarter-brick

Table 9 Components' maximum recorded temperature on ZSC 4:1 quarter-brick

Component (reference design)	Component name	Max. temperature recorded
Q1	BSZ011NE2LS5IATMA1	65.2°C
Q2	IQE013N04LM6ATMA1	67.7°C
Q3	IQE013N04LM6ATMA1	71.7°C
Q4	BSZ011NE2LS5IATMA1	69.5°C
Q5	BSZ011NE2LS5IATMA1	62.6°C
Q6	BSZ011NE2LS5IATMA1	62.9°C
Q7	BSZ011NE2LS5IATMA1	65.8°C
Q8	BSZ011NE2LS5IATMA1	65.7°C
Q9	BSZ011NE2LS5IATMA1	66.1°C
Q10	BSZ011NE2LS5IATMA1	66.1°C
L2	SLQ40407A-1R2MHF	63.4°C
U3	XDPP1100-Q024	54.5°C

Figure 28 shows the thermal profile of the ZSC operating under full load. The temperature data is recorded in Table 9. The maximum temperature recorded is 71.7°C on switch Q3 and 69.5°C on Q4, which is below the thermal rating of these switches.

Reference

[1] Infineon Technologies AG: *XDPP1100 datasheet*; Available online

[2] Infineon Technologies AG: *XDPP1100-Q024 product page*; Available online

Glossary

PSU
power supply unit

SCC
switched capacitor converter

ZSC
zero-voltage switching switched capacitor converter

Revision history

Document revision	Date	Description of changes
V 1.0	2023-02-28	Initial release
V1.1	2024-01-24	Updated gate driver part number to 2EDB7259E Updated Figure 9

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