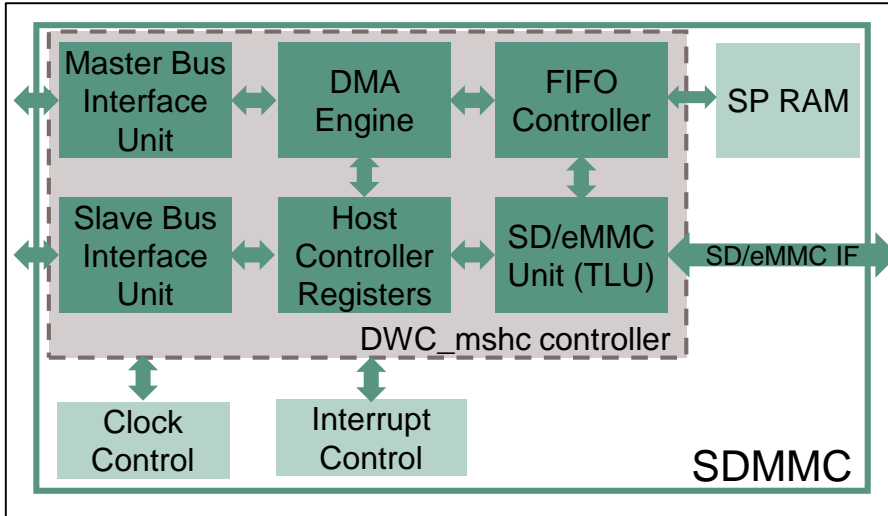


# SDMMC

## SD- and eMMC Interface

AURIX™ TC3xx Microcontroller Training  
V1.0 2020-12





### Highlights

- > The SD- and eMMC Interface (SDMMC) is used to enable communication with a single embedded (eMMC) memory device or a single SD- card
- > Bandwidth up to 400 Mbits/sec for eMMC devices and up to 200 Mbits/sec for SD cards

### Key Features

DMA Engine

Integrated Buffer Memory

Interrupt Support

### Customer Benefits

- > Data transfers without CPU overload
- > 2 x 512 bytes buffer for data transfers between core and cards
- > Status and error signaling

- › The Mobile Storage Host Controller (DWC\_mshc) contains a DMA engine for data transfer to and from the system memory.
- › Multiple modes are supported for different data transfer sizes:
  - Single operation DMA (SDMA) – short data transfer: only a single SD command transaction can be executed for each SDMA operation
  - Advanced DMA-2 (ADMA2) – lengthy data transfers: high data transfer speed is obtained by using the scatter gather DMA algorithm
  - Advanced DMA-3 (ADMA3) – very lengthy data transfers: multiple read/write SD command operations can be performed at a time and high data transfer speed is obtained by using the scatter gather DMA algorithm
- › It supports single and burst transfers

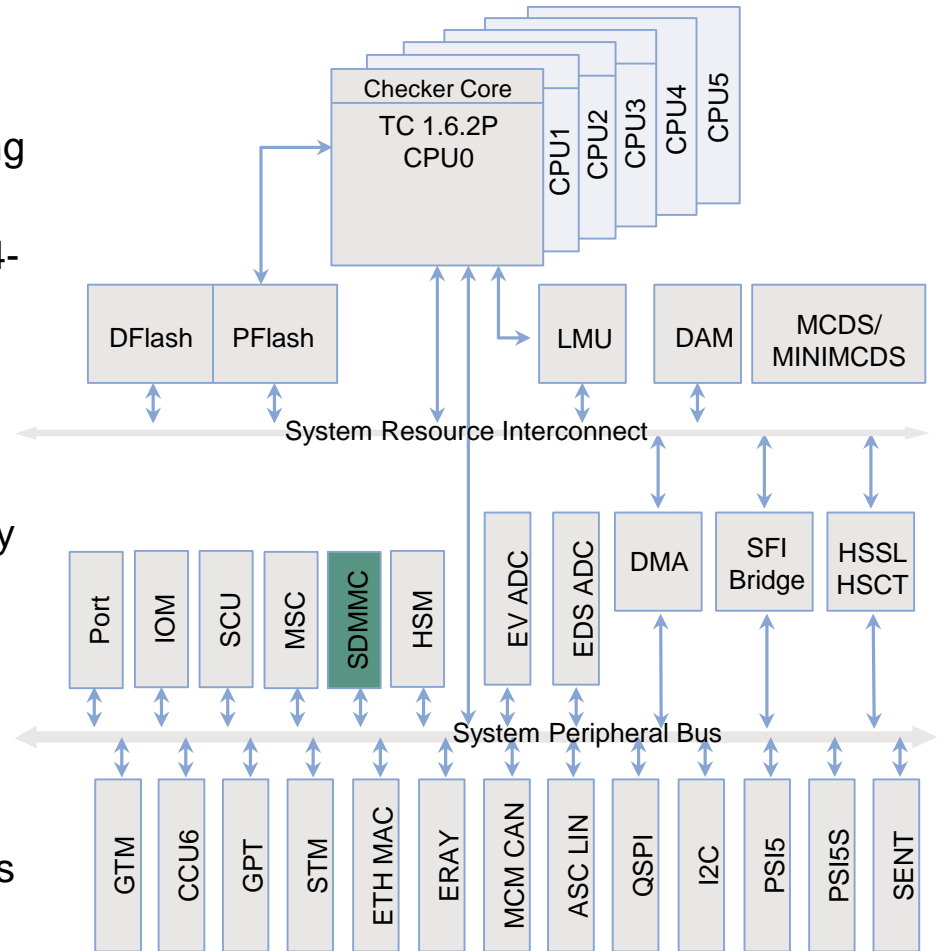
## Integrated Buffer Memory

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- › The internal buffer in the SDMMC is configured as a double buffer (2 x 512 Bytes).
- › Cards with the size less or equal to 256 GB are supported:
  - For card sizes less or equal to 2 GB, the memory addressing is using a byte addressing (32-bit field).
  - For card sizes bigger than 2 GB, the memory addressing is using sector access mode (512 B sector).
- › It can also handle FIFO over and under run conditions.

- › The SDMMC has two types of service requests routed to the interrupt router:
  - Status interrupts (e.g. DMA transfer completed)
  - Error interrupts (e.g. timeouts)
- › Errors in either command or data portion of the transaction can be detected by setting the Error Interrupt flag, for examples:
  - Data errors: Data Timeout Error, Data CRC Error, ADMA Error
  - Command errors: Timeout for CMD\_RES, Framing Error, Header Error
- › The DWC\_mshc supports the Error Interrupt Status register, which captures the interrupt status.

- > SDMMC is the same as most of other components, connected on the System Peripheral Bus (SPB).
- > The SDMMC module conforms to the following standards:
  - JEDEC eMMC 5.1 Specification - JESD84-B51, Feb 2015
  - SD Specifications Part A2 SD Host Controller Standard Specification Version 4.20, August 2015
  - SD Specifications Part 1 Physical Layer Specification Version 5.00, dated February 22, 2016
  - SD Specifications Part E1 SDIO Specification Version 4.10 Sept 2014
- > With the following restrictions:
  - Maximum clock frequency 50 MHz
  - Only standard and high speed grade cards are supported
  - Only 3.3 V supply is supported

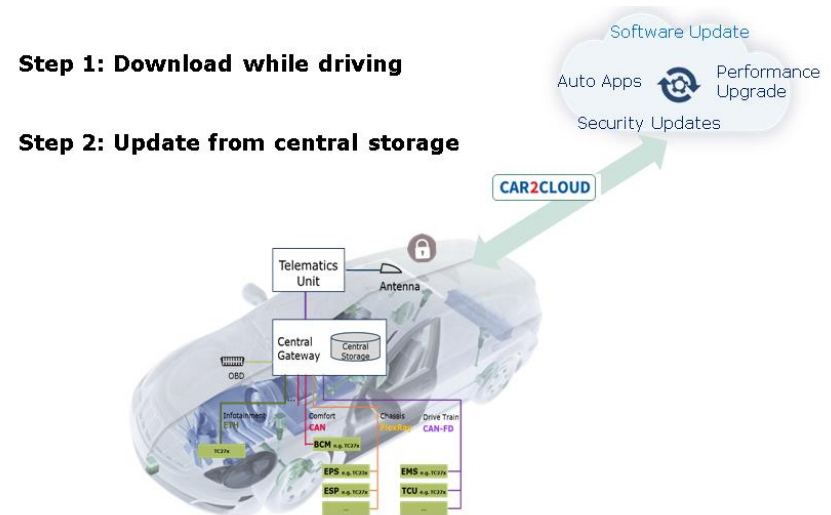


AURIX™ TC39x Block Diagram

# Application example

## Software update Over The Air (SOTA)

- › SDMMC module has many use cases like In-Vehicle infotainment, GPS and telematics, data recorder or Software update Over The Air (SOTA).
- › AURIX™ TC3xx devices besides AURIX™ TC33x have the ability to receive Software updates Over The Air (SOTA).
- › The flash memory is divided in banks and when SOTA is enabled, one of these bank groups can be used to read and execute from, while another group can have new code written to it.



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## Document reference

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