1200-V Gen1p CoolSiC™ MOSFETs in TO263-7 package for automotive applications

About this document

Scope and purpose

This application note describes the family of 1200-V SiC MOSFETs in the TO263-7 package intended primarily for the on-board charger (OBC) systems of battery electric vehicles (BEV), but can also be used in other automotive applications. The purpose of this document is to introduce and explain the specific features of the family products. Important application topics are covered to help design the system for maximum efficiency and reliability.

Intended audience

This document is intended for circuit design engineers developing automotive power electronics systems.

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1 Introduction

The new generation of CoolSiC™ MOSFETs in the TO263-7 pin package is a significant addition to the Infineon automotive SiC MOSFET portfolio offering the best-in-class switching performance, robustness against parasitic turn-ons, as well as improved R_{DSon} and $R_{th(j-c)}$. The features of these new devices address the requests and challenges of the battery electric vehicle (BEV) on-board charger (OBC) application for which this product family was initially optimized. The following details are explained in the subsequent chapters:

- Specific requirements of the target application (OBC) and how this new family addresses them
- Features of the new generation chip technology, including the fast switching and parasitic turn-on robustness
- Advantages and special features of the package
- Topics of device usage, such as gate driving or thermal management

1.1 On-board charger as the target application

With the fast BEV evolution and growing penetration, the charging speed at residential locations depending on the built-in OBC is a very important use topic. Typical OBC consists of a rectifier PFC and high-voltage DC-DC parts. Though OBC parameters vary and different topologies are used for both parts, some of the following general trends can be identified:

- Increasing OBC power to 11–22 kW
- Increasing power density
- The growing interest in bidirectional topologies for supporting V2L (vehicle to load), V2H (vehicle to home) of V2G (vehicle to grid) operation modes and use of controlled switches instead of diodes to enable bidirectional operation
- Battery voltage increase to 800 V

Following these trends and requirements, there is an increasing use of flexible topologies like bidirectional Totem-pole B6 PFC and dual active bridge (DAB) DC-DC for 800 V battery/DC link using 1200 V SiC MOSFETs (Figure 1).

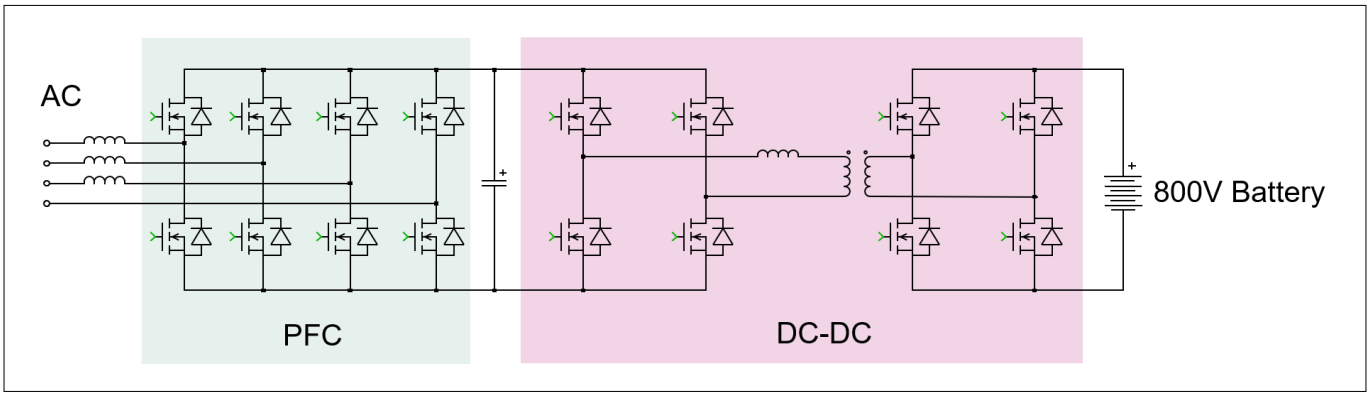

Figure 1 **Illustration of OBC topology: bidirectional Totem-pole B6 PFC (left side) and DAB DC-DC (right side)**

The following OBC trends translate into respective requirements for semiconductor switches as the main building blocks of OBC:

- Low device capacitances, low switching energy, and improved switching control to allow higher frequencies
- 1200 V V_{DS} voltage class and appropriate creepage distance to fit 800 V battery/system voltage
- Surface mount technology (SMT) package preferred for increased power density and automated assembly
- Optimization of all parameters influencing the system cost (including gate driver, cooling system, and passives)

The subsequent chapters provide a detailed explanation on how the new Infineon CoolSiC™ MOSFET family helps to meet these requirements.

1.2 New CoolSiC™ MOSFETs to address OBC application requirements

The new generation of CoolSiC™ MOSFETs in the SMD package code, named “Gen1p”, is based on the first generation (Gen1) of SiC MOSFET chip technology. The new Gen1p SiC MOSFET family in the TO263-7 package brings the following enhancements compared to the Gen1 family in the TO247-3 pin package:

- Compact optimized chip design with improved R_{DSon}* area FOM
- Best-in-class device capacitances and switching energy
- A combination of low C_{rss}/C_{iss} ratio and high V_{GSth} helps avoid parasitic turn-ons
- Reduced total gate charge Q_G for lower driving power/losses
- Increased turn-on voltage (V_{GS} = 20 V) for lower R_{DSon}
- Advanced diffusion soldering chip-mount technology for improved $R_{th(j\text{-}c)}$
- Lower package stray inductance for faster and cleaner switching
- Source sense (Kelvin) pin for a better gate control and reduced switching losses
- Increased creepage distance to fit 800 V DC applications without the need for coating
- Choice of R_{DSon} options for an optimal fit for application requirements, including the only 9 mΩ device in the TO263-7 package currently available on the market

These features provide the following benefits to the application:

- Smaller inductors and capacitors due to higher switching frequency
- Lower cooling effort and smaller heat sinks due to lower switching losses
- Higher power density and lower system costs because of the SMD package
- Simplified unipolar gate driver enabled by 0 V turn-off with reduced driving power due to low Q_G

1.3 Device portfolio in the TO263-7-12 package

The AIMBG120RxxxM1 family consists of eight devices with different R_{DSon} ratings, including the only 9 mΩ 1200 V SiC MOSFET in the TO263-7 package currently available on the market. This choice makes it possible to always find the optimal fit for any combination of conduction/switching losses in a particular OBC application (Figure 2). The key advantages of the Gen1p chip technology are explained in Chapter 2, followed by the package benefits discussed in Chapter 3.

Portfolio overview

$R_{DS(on)\ typ}$ [mΩ]	TO-263-7 pin
9 mΩ	AIMBG120R010M1
20 mΩ	AIMBG120R020M1
30 mΩ	AIMBG120R030M1
40 mΩ	AIMBG120R040M1
60 mΩ	AIMBG120R060M1
80 mΩ	AIMBG120R080M1
120 mΩ	AIMBG120R0120M1
160 mΩ	AIMBG120R0160M1

Figure 2 Family of Infineon 1200 V CoolSiC™ MOSFETs based on Gen1p chip technology in TO263-7-12 package

2 New chip technology Gen1p

Gen1p is the evolution of the first CoolSiC™ MOSFET generation Gen1. It was optimized for the OBC application profile to provide a cost-effective solution while maintaining the reliability and the optimal balance of the key parameters.

The following are the advantages of the Gen1p technology:

- Best-in-class switching performance: low switching losses and device capacitances
- Robustness against parasitic turn-ons due to high V_{GSth} and low C_{rss}/C_{iss}
- Optimized chip technology for reduced R_{DSon}* area
- $V_{GS(on)}$ = 20 V for lower R_{DSon} for the same chip size
- Advanced diffusion soldering die attach for reduced R_{th}

2.1 Switching performance

Switching performance is one of the key optimization factors of Gen1p chip technology. Due to the reduced chip area (for the same R_{DSon}), the device capacitances reduced significantly as shown in Figure 3 for the 80 mΩ parts. Both switch-on and switch-off energy values of Gen1p 80 mΩ device reduced more than 2 times compared to Gen1. This allows for a much higher switching frequency (and therefore smaller inductors) for the same switching losses, or much lower switching losses (and lower cooling effort) for the same switching frequency. The same implies to the output capacitance C_{oss} improved by a factor of 2. The 49% reduction in input capacitance C_{iss} means that lesser gate driving power is required to control the MOSFET, resulting in a cheaper gate driver and reduced driving losses. The reduced C_{rss} and C_{rss}/C_{iss} ratio help against parasitic turn-ons by minimizing the parasitic transients on the gate caused by high output dv/dt (more details on this topic is discussed in Chapter 2.2).

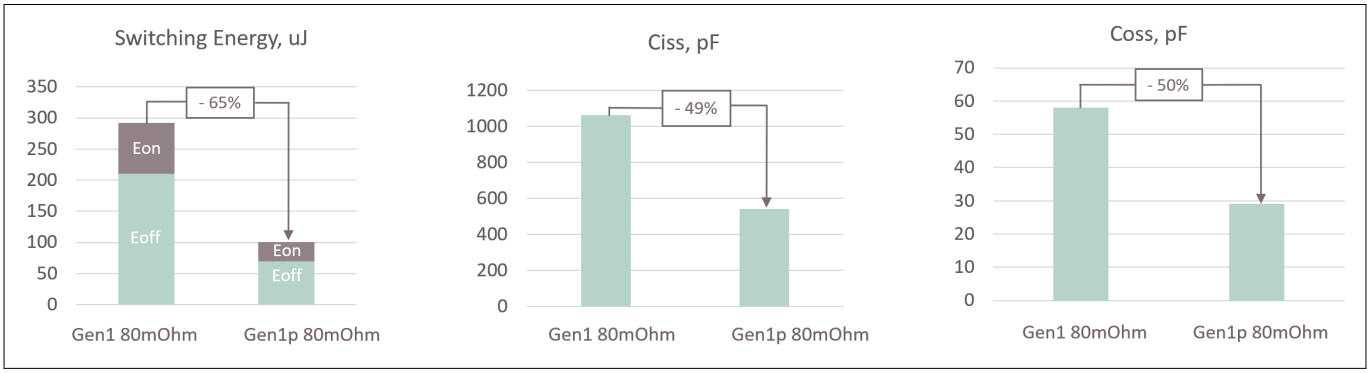

Figure 3 Improvements in Gen1p switching parameters over the first generation

2.2 Avoiding parasitic turn-on

The parasitic turn-on phenomenon is illustrated in Figure 4.

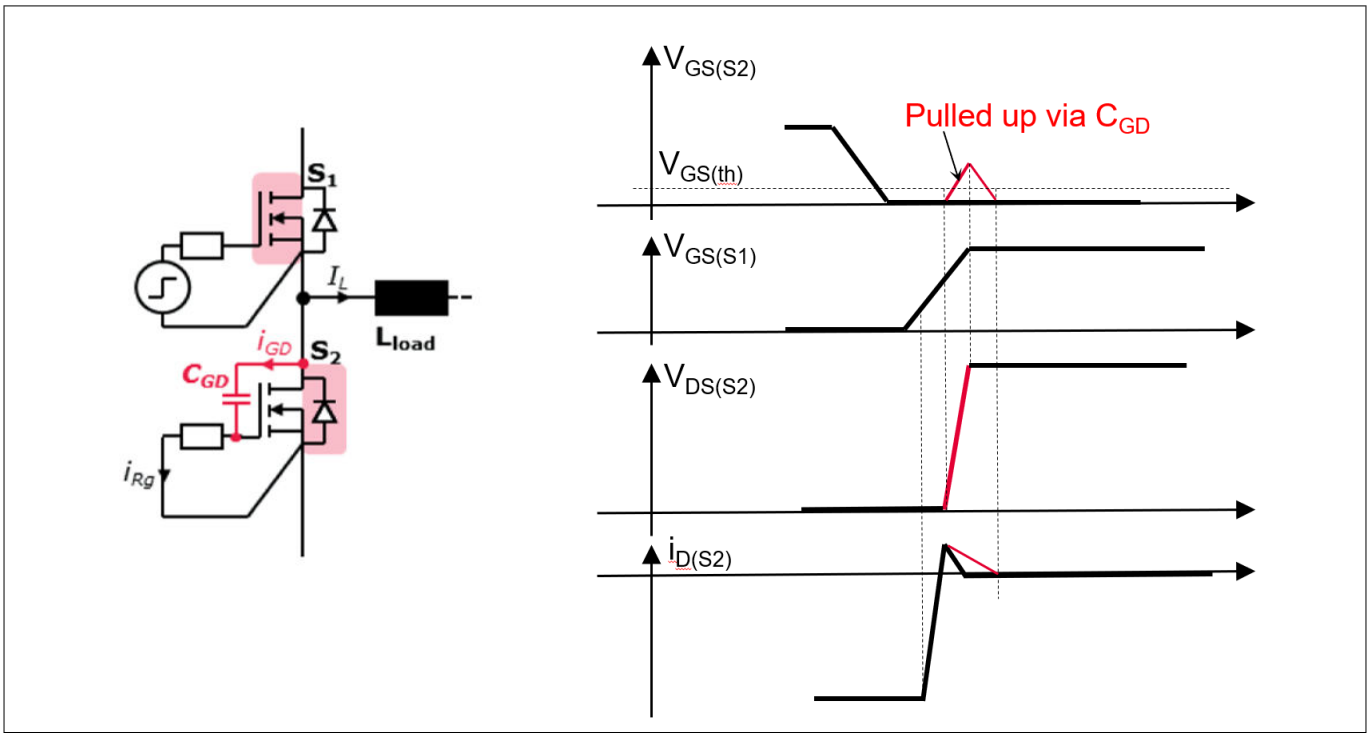

Figure 4 Parasitic turn-on illustration

In a half-bridge circuit (left side), S2 has just turned off (the body diode is freewheeling the load current) and then S1 turns on. The parasitic surge is induced at S2 gate by the S2 drain voltage transient via the parasitic capacitance C_{GD} (C_{rss}). If the surge level exceeds $V_{GS(th)}$, then S2 reopens. This leads to an extended tail of the reverse recovery current of the diode $i_{D(S2)}$ and an increase in Q_{rr}.

The detailed analysis and measurements presented in reference [1] provide an important guideline for choosing the R_{Goff} values to avoid parasitic turn-on at $V_{GS(off)}$ = 0 V. Figure 5 shows the test setup to characterize the critical value of R_{Goff} where S2 still faces no parasitic turn-on while S1 turns on. The R_{Gon} value sets the dv/dt generated by S1 turn-on.

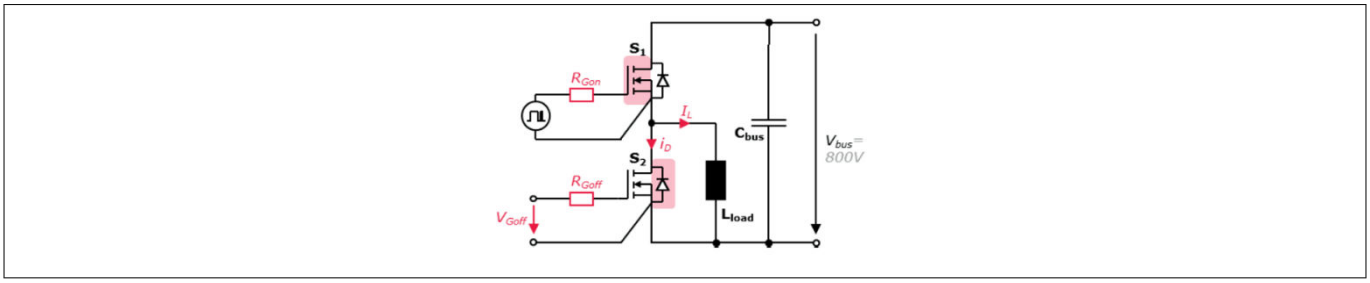

Figure 5 Test setup for characterizing the critical gate resistance R_{Goff}

S2 is turned off by R_{Goff} and then S1 is turned on. R_{Gon} sets the dv/dt of the transition.

The criterion of the parasitic turn-on in this measurement is the 10% increase in Q_{rr} (illustrated by a orange curve in Figure 6 at left side). It was investigated at which maximum value of R_{Goff} no parasitic turn-on was observed (this value of R_{Goff} is called “critical” and is shown on the Y-axis in Figure 6 at right side). Critical values were evaluated for different R_{Gon} values (X-axis) at different junction temperatures (25°C, 100°C, and 175°C) and load conditions (0 A or 40 A).

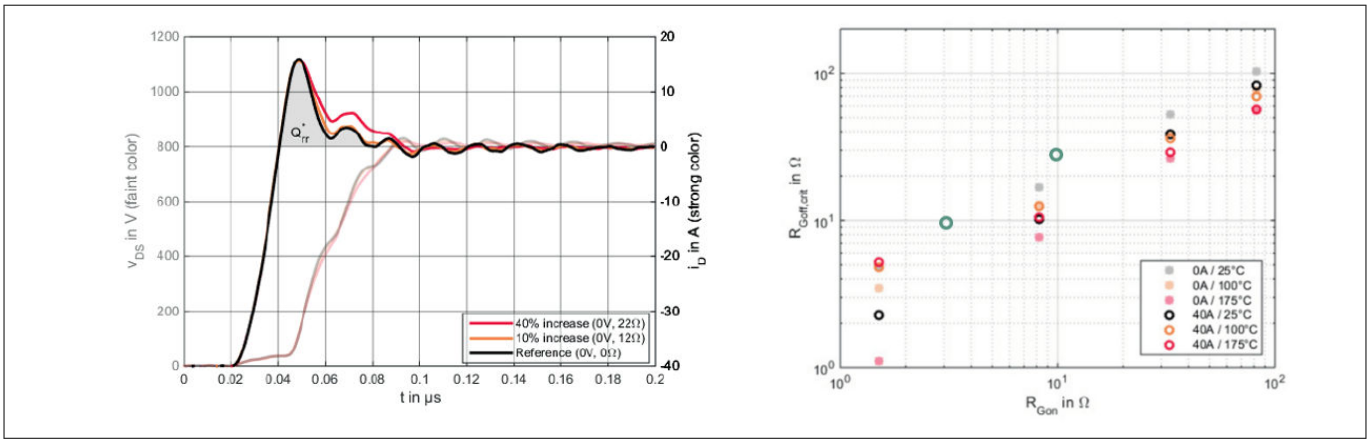

Figure 6 Illustration for a parasitic turn-on criterion and critical R_{Goff}

Left side: The criterion of a parasitic turn-on is defined as "Q_{rr} increase by 10%" (solid orange waveform) relative to the reference waveform at R_{Goff} = 0 Ω (black waveform). Right side: Critical (maximum) values of R_{Goff} at which no parasitic turn-on occurs (Y-axis). The X-axis represents the values of R_{Gon} setting the transition dv/dt. Green dots are the results of the AIMBG120R080M1 measurement at 175°C and 10 A.

The following two key parameters define how much MOSFET is susceptible to parasitic turn-on conditions:

- C_{GD}/C_{GS} (also referred to as C_{rss}/C_{iss}) ratio defines the level of parasitic V_{GS} surge induced by V_{DS} transient, and C_{GD}/C_{GS} is significantly enhanced in Gen1p (Figure 7)
- V_{GSth} (higher V_{GSth} means lesser chance for V_{GS} surge to turn on the MOSFET)

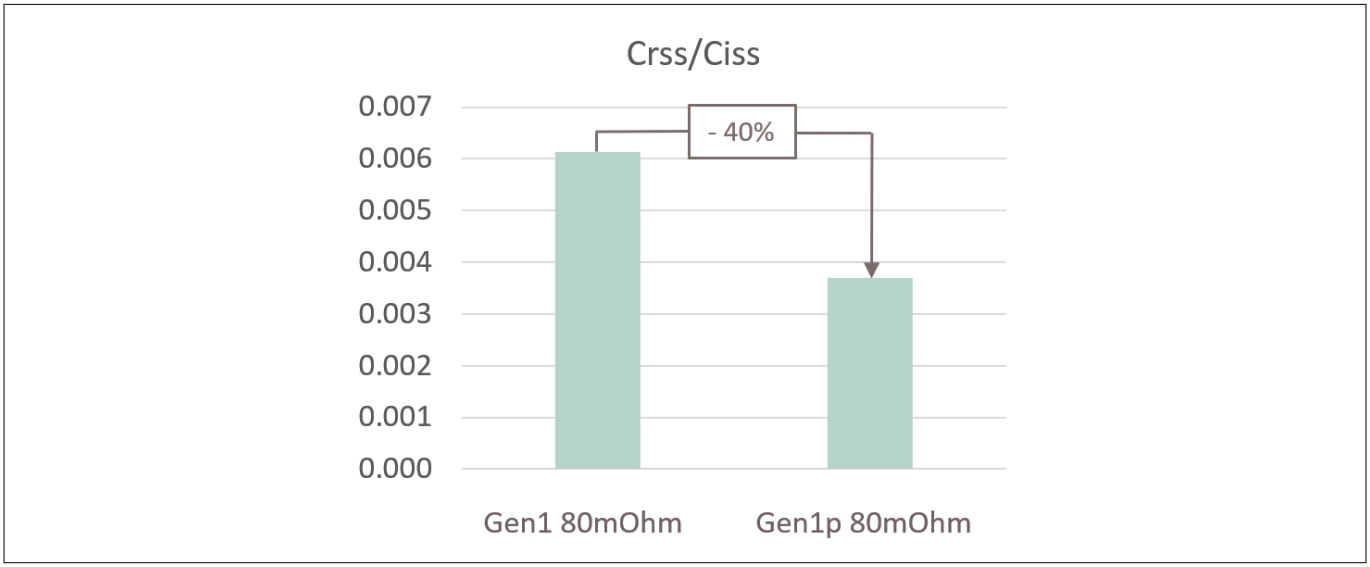

Figure 7 Parasitic turn-on conditions

The C_{rss}/C_{iss} ratio of Gen1p was improved by 40% compared to Gen1. This reduced the parasitic transition of V_{DS} voltage to the gate.

The combination of high V_{GSth} and reduced C_{GD}/C_{GS} (or C_{rss}/C_{iss}) ratio of Infineon's Gen1p chip technology results in higher critical gate resistance values (green dots in Figure 6). This gives more flexibility to the R_{Goff} selection, allowing wider control over commutation speed while maintaining the reliable switch-off with 0 V $V_{GS(off)}$. Zero gate voltage turn-off makes simpler unipolar gate driving possible, as described in Chapter 4.3.

3 Package information

Offering the new Gen1p in a SMT package addressed the demand for higher system power density and a simpler PCB assembly process. In this chapter, the specific features of the TO263-7-12 package used for this product family are discussed, such as sense (Kelvin) source pin, increased creepage distance, and improved $R_{th(j-c)}$ due to chip diffusion soldering, significant thermal considerations, and assembly recommendations.

3.1 Sense (Kelvin) source pin

The additional sense source pin (pin 2 in Figure 8) provides a dedicated connection between the negative terminal of the gate driver and the chip's source potential.

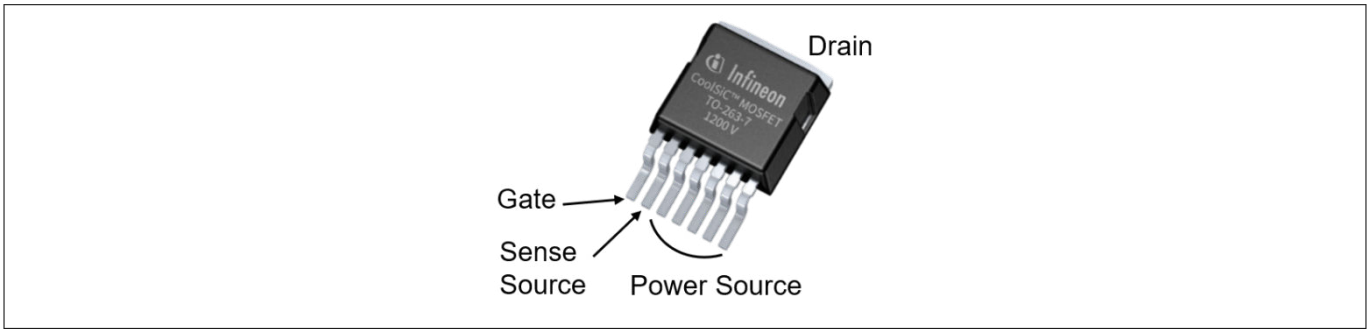

Figure 8 Pin designation of TO263-7-12 package

This avoids distortion of the gate control voltage ($V_{GS,\,chip}$ in Figure 9) caused by a voltage drop across the inductance and resistance of the internal power source bond wire ($V_{L,S}$ and $V_{R,S}$ in Figure 9) at high i_{DS} currents.

Attention**: **Driving the gate with reference to sense source is the only recommended option.

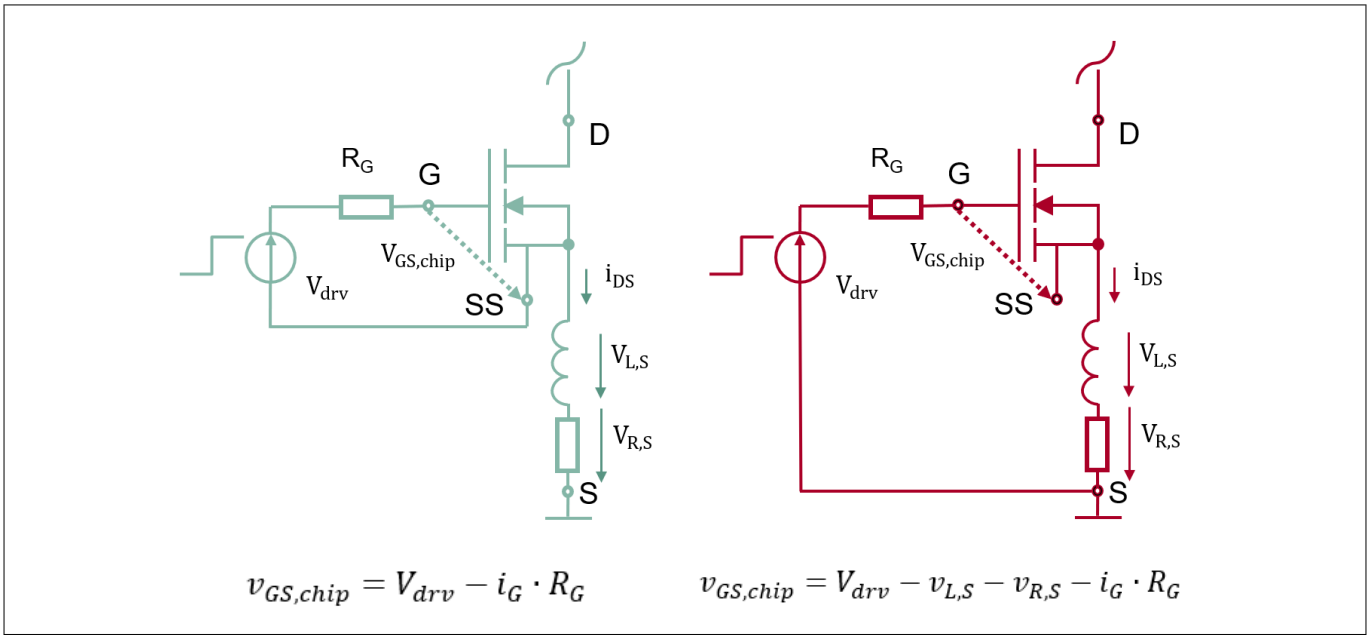

Figure 9 Gate drive connection options referenced to the sense source pin SS (left side, recommended) and power source S (right side, not recommended)

The simulated switching curves in Figure 10 show the significant difference between switching behavior and switching losses for these driver connection options. Slower I_D increase and delayed V_{DS} drop lead to significantly higher switching losses.

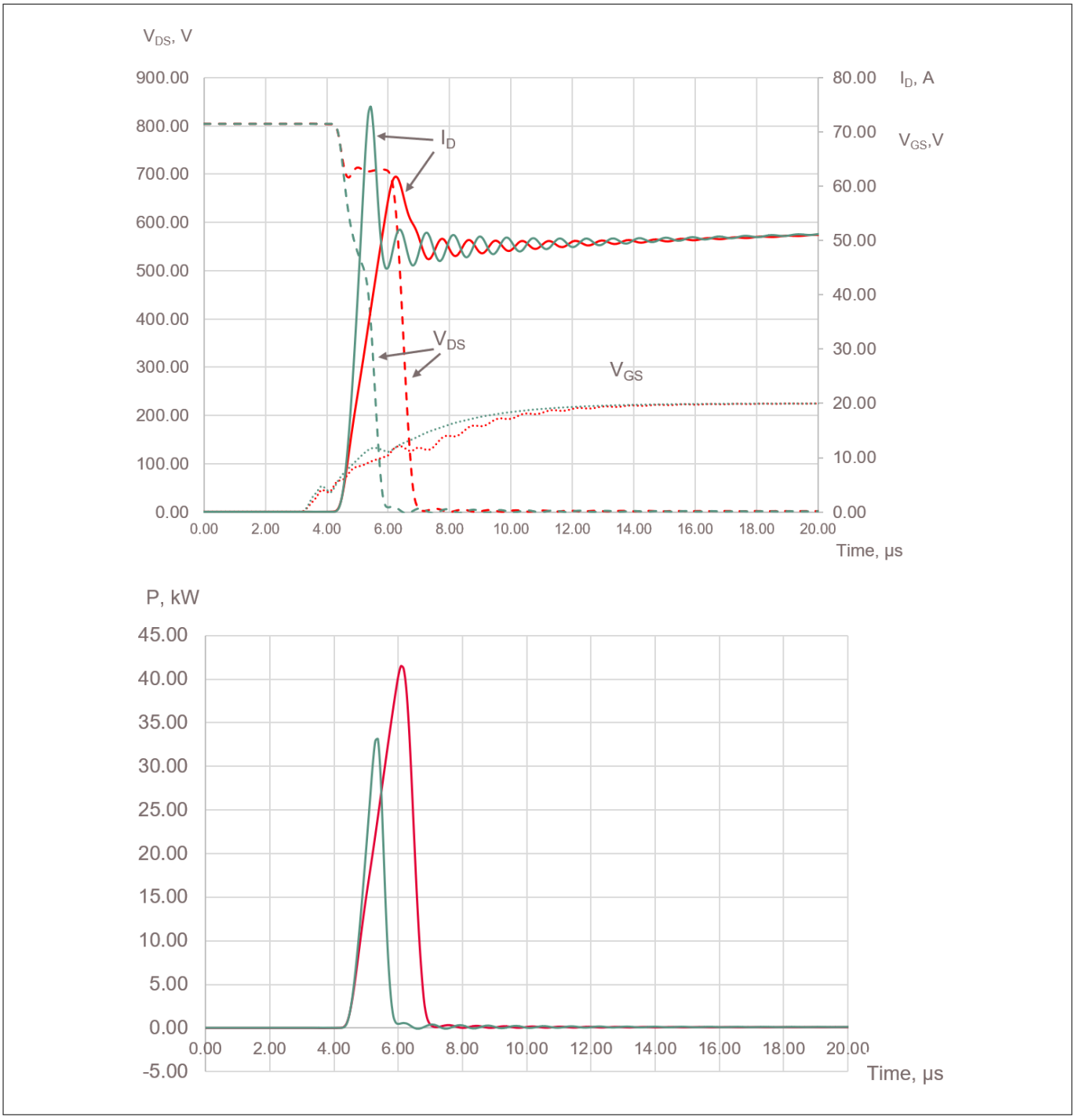

Figure 10 **Simulated switching curves and losses with the gate driver referenced to the sense source (green, recommended) versus power source (red, not recommended)**

3.2 Creepage distance

In the design of the TO263-7-12 package, the optimal balance is found between the thermal performance set by the exposed pad area of the lead frame and the creepage distance along the package surface from the source leads to the drain pad. As a result, high creepage distance value of 5.89 mm is achieved. The shortest creepage paths along the package are shown in Figure 11. This distance value helps meet the creepage requirements of the 800 V system without the need for a PCB coating (according to IEC 60664-1, material group II, only 5.6 mm creepage is required for the 800 V system).

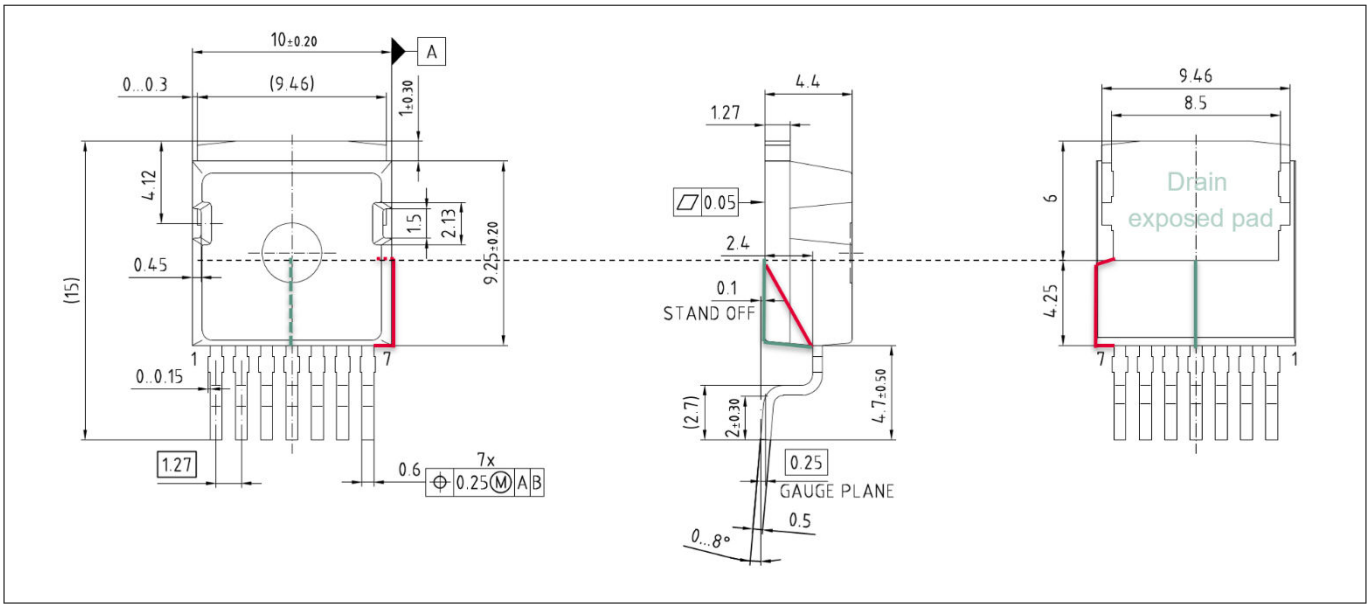

Figure 11 Shortest creepage paths on TO263-7-12 package surface

3.3 Improved $R_{th(j-c)}$

While reducing the chip size helps improve the switching performance, it also increases the challenge of dissipating power from the chip. To compensate for the reduction in power dissipating area and maintain $R_{th(j-c)}$ at a minimum level, the diffusion soldering die attach technology was implemented. This helped maintaining the same $R_{th(j-c)}$ for the shrinked chip with the same R_{DSon} or reducing $R_{th(j-c)}$ by 25% for the same chip size (Figure 12).

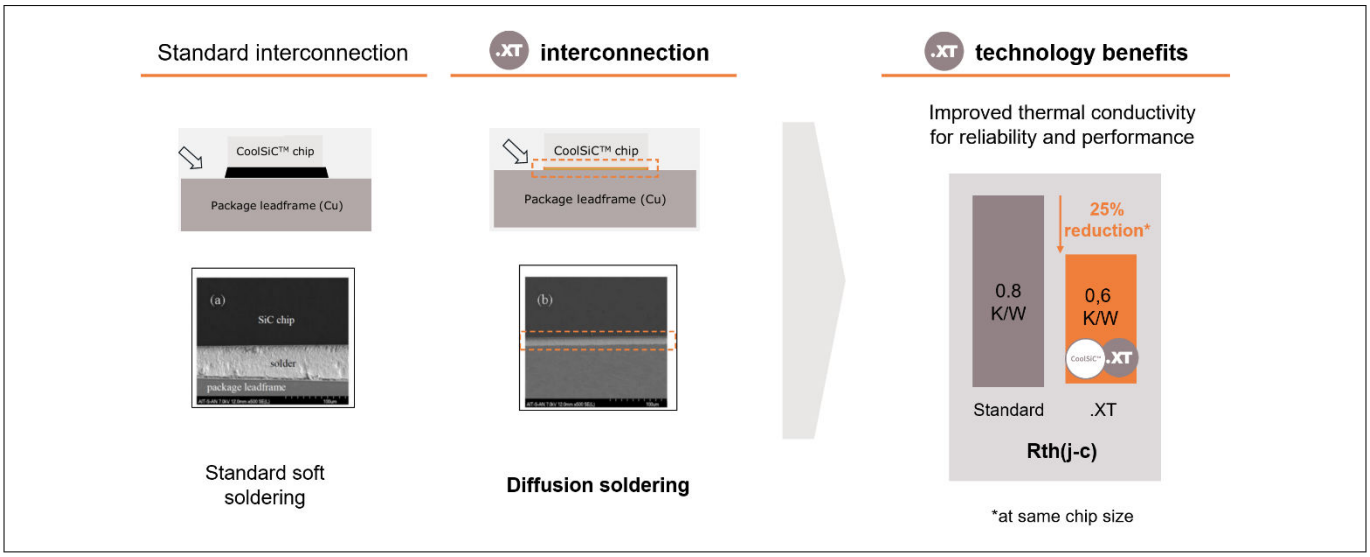

Figure 12 Diffusion soldering technology and its impact on $R_{th(j-c)}$

Since heat dissipation from the package to the heatsink via PCB remains the challenge for all bottom-side-cooled (BSC) SMD packages, this topic requires special attention and is further discussed in Chapter 3.4.

3.4 Thermal considerations

Note: The maximum junction temperature must never be exceeded, even under the worst operating conditions (maximum losses at highest ambient temperature). Since both R_{DSon} and switching energy E_{tot} increase with T_{vj}, the correct values of "hot" (at maximum target T_{vj}) R_{DSon} and E_{tot} should be used for the calculations.

The use of insulated metal substrate (IMS) board is highly recommended for optimal thermal management and to maintain the junction temperature below the designated level. The results of the thermal simulations with the 9 mΩ part AIMBG120R010M1 (largest chip size) and the 80 mΩ AIMBG120R080M1 show the thermal performance that can be achieved for these types with different PCB types (Figure 13). The simulation is performed with a power loss of 20 W, an ambient temperature of 25°C, and a solder void rate of 10%. The resulting thermal resistance values from the junction to the heatsink via the PCB show that using an IMS board offers a significant advantage in $R_{th(j\text{-}hs)}$ reduction.

Board	Cu Thickness	Solder Voids Rate (Board Solder)	Rth(j-hs) [K/W]	
			AIMBG120R010M1	AIMBG120R080M1
IMS 1Layer	70µm	10%	1.31	2.41
IMS 1Layer	100µm	10%	1.29	2.39
IMS 2Layer	70µm	10%	1.76	3.01
JEDEC FR4 2s2p	70µm	10%	5.92	7.23

Figure 13 Comparison of thermal resistance junction to heatsink $R_{th(j\text{-}hs)}$ for AIMBG120R010M1 and AIMBG120R080M1 mounted on IMS and FR4 PCBs

If an FR4 PCB is used, the thermal connection from the device package to the bottom copper plane becomes the key to thermal performance. This is usually performed by plated through-hole vias in the board. Thermal and electrical analysis and/or testing along with a proper board assembly design procedure are recommended to determine the optimal PCB parameters and the number of vias required. The application note "Thermal Measurement for D2PAK on PCB" [4] provides the detailed analysis of the measurements carried out on a real prototype board with different combinations of PCB types (2 or 4 layers, copper thickness), footprint area as well as via matrix setups (example of PCB part and the corresponding measurement results in Figure 14).

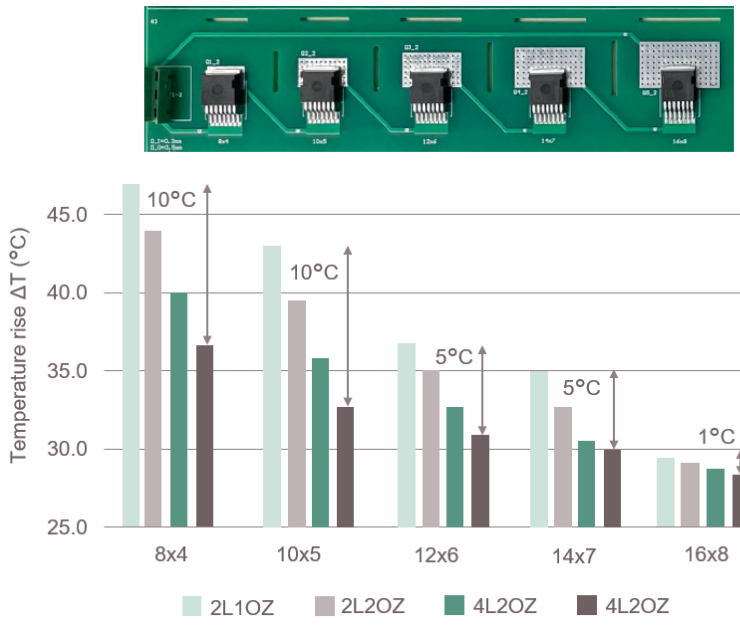

Figure 14 Evaluation board for comparing TO263-7 footprints on FR4 PCB with different layer configurations, copper thickness, and a via matrix setup (PCB on top)

The graph depicts the respective values of the temperature increase. The results show the impact of thermal vias (8×4 to 16×8 matrix), copper layers (2L or 4L), and copper layer thickness (1OZ or 2OZ) on thermal performance.

3.5 Assembly recommendations

The detailed information about the TO263-7-12 package is available on the https://www.infineon.com/cms/en/product/packages/PG-TO263/PG-TO263-7-12/ page. It includes the package drawings, soldering PCB footprint, 3D model and references to useful materials. The application note “Recommendations for board assembly of Infineon transistor outline type packages” [3] covers topics, such as recommended reflow process parameters, moisture sensitivity level (MSL) considerations, and other helpful recommendations.

4 Gate drive

4.1 Gate driver considerations

Controlling the SiC power MOSFET gate voltage is one of the most important application topics because of its direct influence on both the system performance as well as MOSFET lifetime and reliability. In this chapter, the following topics are discussed:

- Selection of gate turn-on and turn-off voltages
- Taking advantage of 0 V switching
- Gate charge Q_G and required gate driver output power

4.2 Gate drive voltage

Choosing the correct V_{GSon} and V_{GSoff} voltages has a significant impact on the system performance and device reliability. The recommended V_{GSon} and V_{GSoff} levels for Gen1p chips are 20 V and 0 V, respectively. An increase in V_{GSon} from 15 V to 18 V gives an 18% reduction in R_{DSon} and a value of 20 V provides the lowest R_{DSon} with an additional 5% improvement as shown in Figure 15. Note that most of the datasheet parameters for the Gen1p family are provided at $V_{GS(on)}$ = 20 V, while driving the gate at $V_{GS(on)}$ = 18 V, would require a corresponding parameter derating.

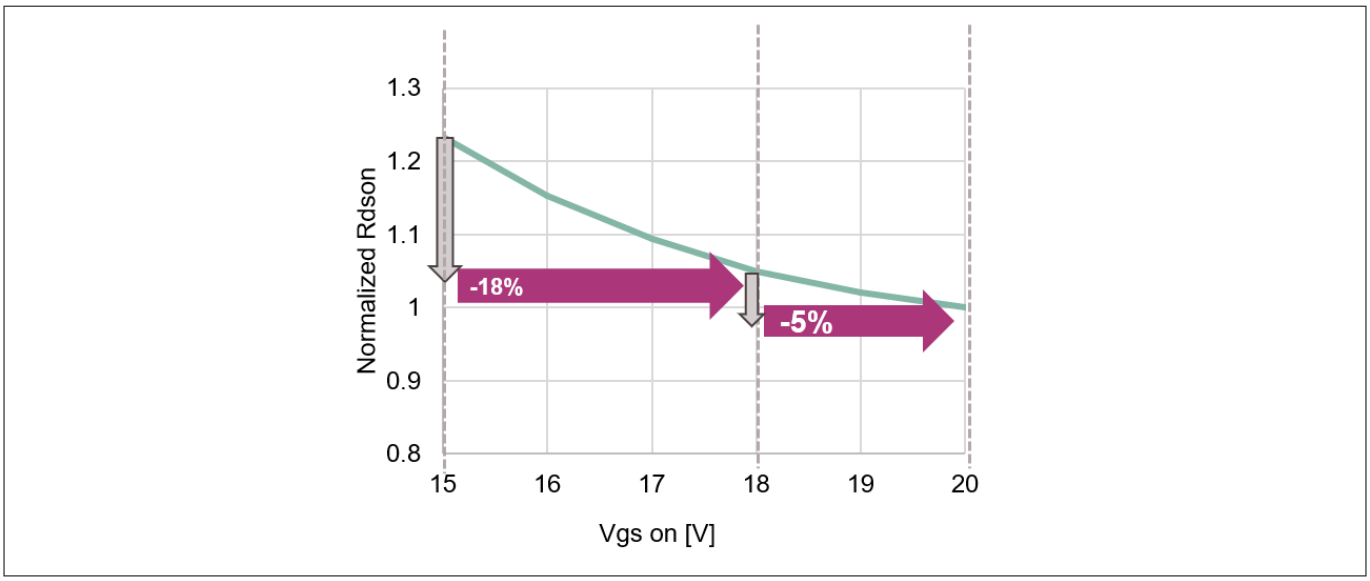

Figure 15 Graph illustrates the $R_{ds(on)}$ reduction with increased $V_{gs(on)}$ value

Reduced by 18% with $V_{gs(on)}$ changing from 15 V to 18 V and an additional 5% from 18 V to 20 V.

The $V_{GS(off)}$ value of 0 V is recommended as discussed in Chapter 2.2. With the recommended gate driving voltages, one can achieve the highest efficiency and reliability. The customer can choose also different V_{GS} voltages according to their needs in the range from -5 V to 0 V for turn off and 15 V to 20 V for turn on. Having additionally a broad transient gate driving window from -10 V to +25 V makes the design of these devices very convenient.

Note: The choice of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in the application note 2018-09 "Infineon guidelines for CoolSiC™ MOSFET gate drive voltage window" [2] must be considered to ensure the reliable operation of the device over the expected lifetime.

4.3 Unipolar gate driving

The use of MOSFETs, which are susceptible to parasitic turn-on, typically required negative biasing of the gate voltage to ensure a reliable turn-off state without the risk of parasitic turn-on gate voltage induced by Miller capacitance. From the gate driver's perspective, this means that a negative voltage source is needed, which requires several additional components (Figure 16, left side).

As discussed earlier in Chapter 2.1, Infineon's Gen1p technology facilitates reliable zero gate voltage turn-off without the risk of parasitic turn-on. This eliminates the need for a negative gate drive voltage and can significantly simplify the gate driver power supply by saving a Schottky diode, two capacitors, a Zener diode, and simplifying the transformer (Figure 16, right side).

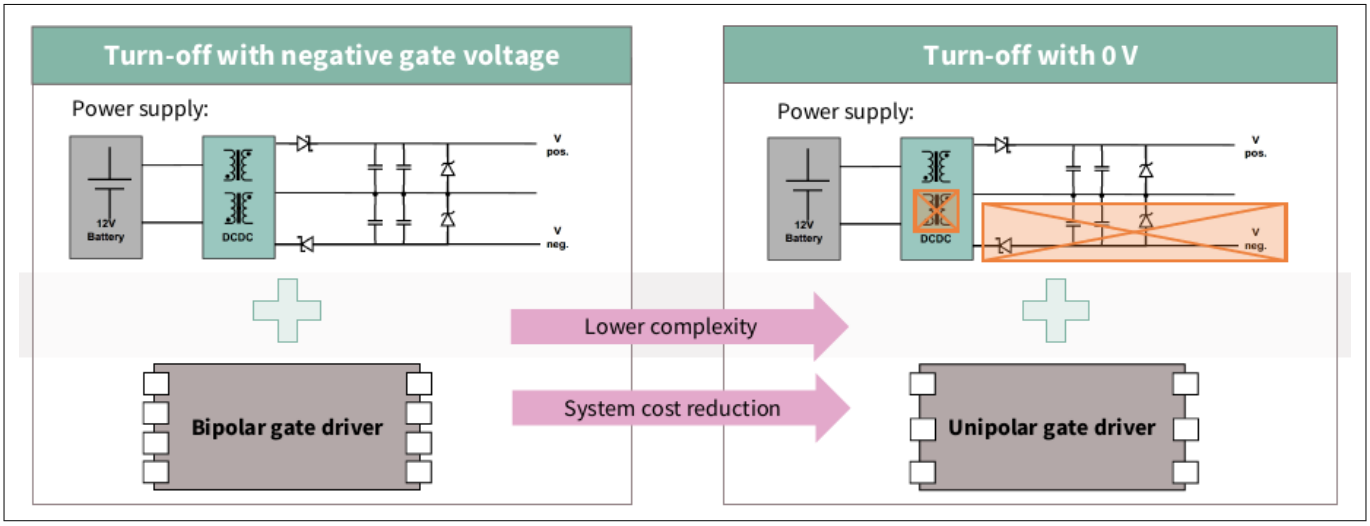

Figure 16 Unipolar gate drive possibility with reliable 0 V turn-off helps simplify the gate driver, reduce component count and cost

As explained in [1], even devices less susceptible to parasitic turn-on, such as Gen1p MOSFETs, in unipolar gate drive mode require careful consideration of the $R_{G(off)}$ value and PCB layout of critical gate traces to ensure no drain-gate capacitance is added externally. Sometimes the use of the driver with Miller clamp functionality can still be considered to provide an additional margin of safety.

4.4 Gate charge and driver output power

The gate charge Q_G value has been improved in Gen1p technology, as shown in Figure 17.

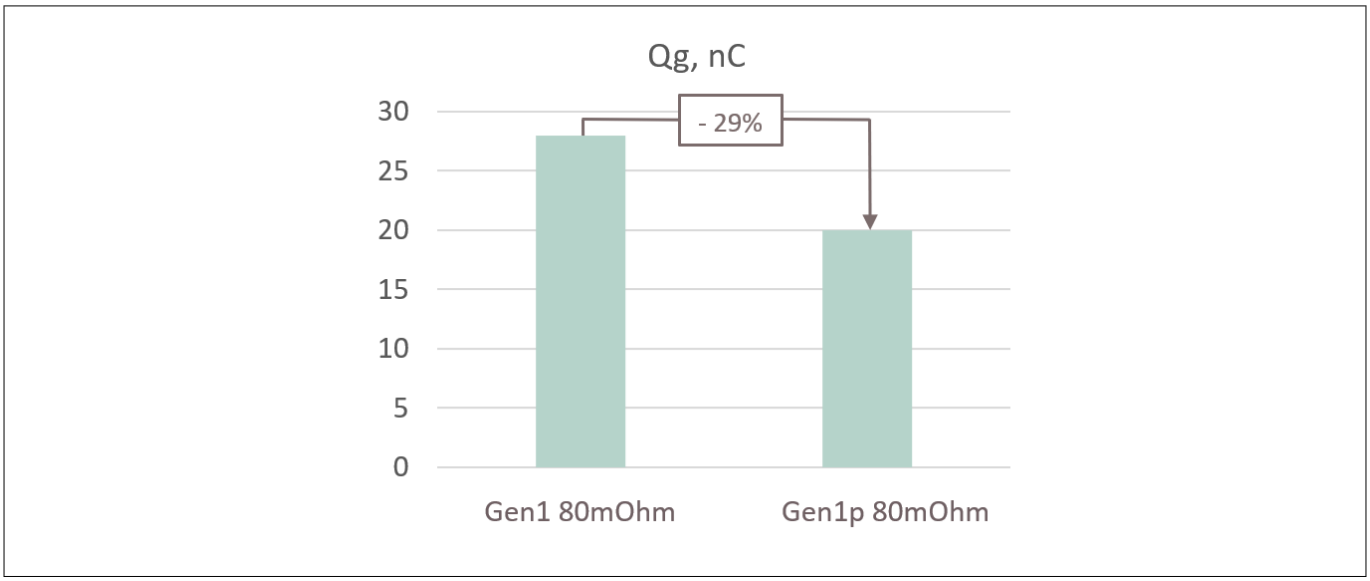

Figure 17 Gen1p technology gate charge reduction

Q_G is calculated for V_{GS} swing from 0 to 18 V for Gen1 and from 0 V to 20 V for Gen1p.

Therefore, the required output power of the gate driver, estimated as $P_{drv} = Q_G * F_{SW} * \Delta V_{GS}$, is reduced proportionally to Q_G. This helps reducing the cost of the gate driver and power loss as well as improving system efficiency, especially important with a light load operation.

4.5 ESD sensitivity

The ESD sensitivity of high-impedance MOSFET gate terminal is well known. Any external charge Q connected to the gate generates a gate voltage Q/C_{iss} that can easily exceed the maximum V_{GS} value and lead to electrical failure in a catastrophic (gate oxide breakdown) of latent (gate oxide degradation) form. SiC MOSFETs optimized for faster switching and having lower C_{iss} develop even higher Q/C_{iss} voltage values. Special measures need to be taken throughout the logistics and manufacturing process to ensure that the gate terminal is never accidentally connected to potentially dangerous ESD sources. Some useful recommendations can be found in [5].

References

[1] K. Sobe, T. Basler and B. Klobucar: *Characterization of the parasitic turn-on behavior of discrete CoolSiC™ MOSFETs*; PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; 2019, pp. 1–7, ISBN: 978-3-8007-4938-6; https://ieeexplore.ieee.org/document/8767479

[2] Infineon: *Application Note AN2018-09 "Guidelines for CoolSiC™ MOSFET gate drive voltage window"*; https://www.infineon.com/dgdl/Infineon-Guidelines_for_CoolSiC_MOSFET_gate_drive_voltage_window-ApplicationNotes-v01_20-EN.pdf?fileId=5546d4626e8d4b8f016e9385274a66df

[3] Infineon: *Application Note "Recommendations for board assembly of Infineon transistor outline type packages"*; https://www.infineon.com/dgdl/Infineon-Recommendations_for_Board_Assembly_TO-P-v03_00-EN.pdf?fileId=5546d462580663ef0158069840880338

[4] Infineon: *Application Note AN_2112_PL18 "Thermal Measurement of D2PAK on PCB"*; https://www.infineon.com/dgdl/Infineon-AN-2021-02_Thermal_measurement_for_D2PAK_on_PCB-ApplicationNotes-v02_00-EN.pdf?fileId=5546d4627956d53f0179a29c13950aa6

[5] Infineon: *Application Note AN_2112_PL18_2112_024619 "Designing with power MOSFETs. How to avoid common issues and failure modes"*; https://www.infineon.com/dgdl/Infineon-Designing_with_power_MOSFETs-ApplicationNotes-v01_02-EN.pdf?fileId=8ac78c8c7ddc01d7017e6c619a490f47

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Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.