Application Note AN 2013-03
V1.0 March 2013

ZVS Phase Shift Full Bridge

CFD2 Optimized Design

IFAT PMM APS SE SL
Di Domenico Francesco
Mente René

Edition 2013-03-14
Published by
Infineon Technologies Austria AG
9500 Villach, Austria

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AN 2013-03
Revision History: date (13-03-14) , V1.0
Previous Version: none
Subjects: none

Authors: IFAT PMM APS SE SL
Di Domenico Francesco
Mente René

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1 Introduction

In modern power electronics applications, there is a growing need for high efficiency combined with high power density. This combination is not easy to achieve and this definitely represents the most important trade-off challenge for power converter design. In fact, the simplest way to reduce the size especially of magnetic components is to increase the switching frequency, but unfortunately this normally involves an increase of switching losses, and so worse efficiency. One way to improve the trade-off relation is to use soft switching topologies. The main benefit of these topologies is to minimize the losses generated by the power devices during switching transitions. The ZVS(1) phase shift full bridge used in IFX(2) board achieves this reduction of losses due to a zero voltage turn-on of the MOSFET(3)s. In this design the ZVS operation is maintained from full load down to very light load.

This paper is going to show in a “step by step approach” how to achieve highest efficiency in a ZVS topology (IFX board) using the new CoolMOS™ IPW65R080CFD. The main features and benefits of this new Superjunction MOSFET are documented in the application note “650V CoolMOS™ CFD2” released by Infineon in February 2011. All possible adjustments like delay times, dimensioning of the resonant inductance, variances of $R_{G,ext}$(4), optimization of primary-secondary MOSFETs delays are going to be explained in detail in the present paper.

The purpose of this paper is to give electrical design engineers with fundamental knowledge of the ZVS phase shift principle of operation the general guidelines to optimize the design of this topology using the new IFX CoolMOS™ CFD2 series. For these reasons the mathematical content and all the design calculation details will be intentionally not analyzed in this document, whose main focus is on the waveforms analysis in a “real” application board.

Before starting with the measurements and optimization for the IPW65R080CFD on a given setup the following chapter is going to illustrate the IFX board and the main components.

2 IFX board and main components

The following figure represents the new developed ZVS DC(5)/DC converter for telecom rectifiers with an output voltage from 45VDC to 56VDC and an output power of 2kW. This converter works with an input voltage between 300VDC and 420VDC (typical 385VDC) and a switching frequency of 100kHz on the primary side.

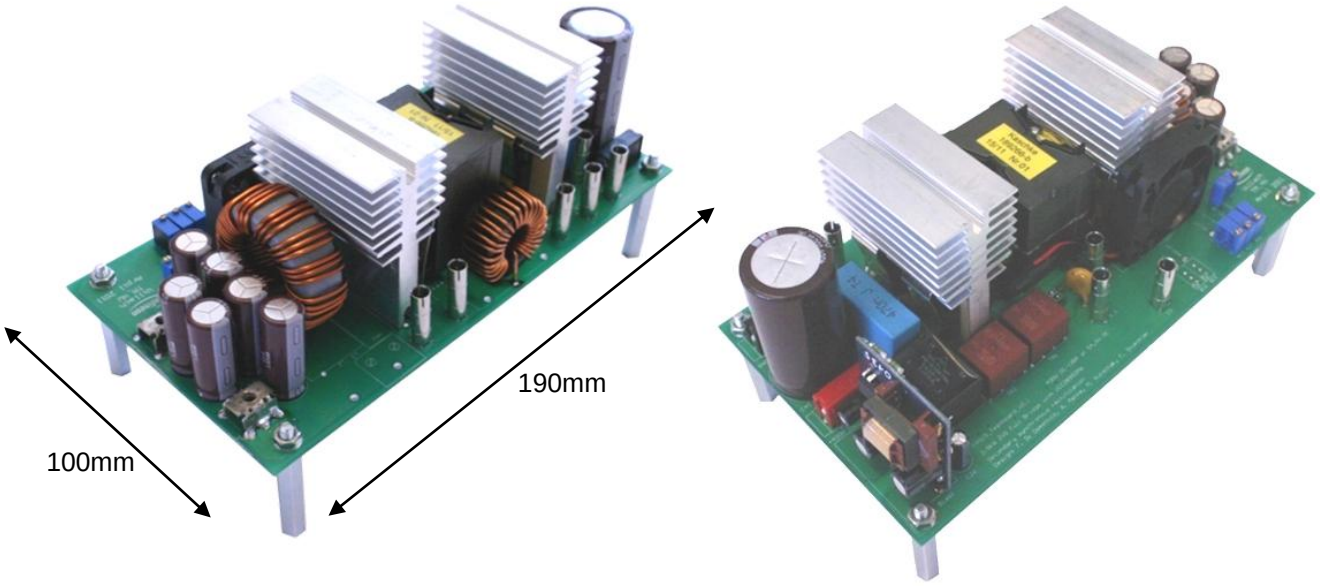

Figure 1: IFX ZVS phase shift full bridge

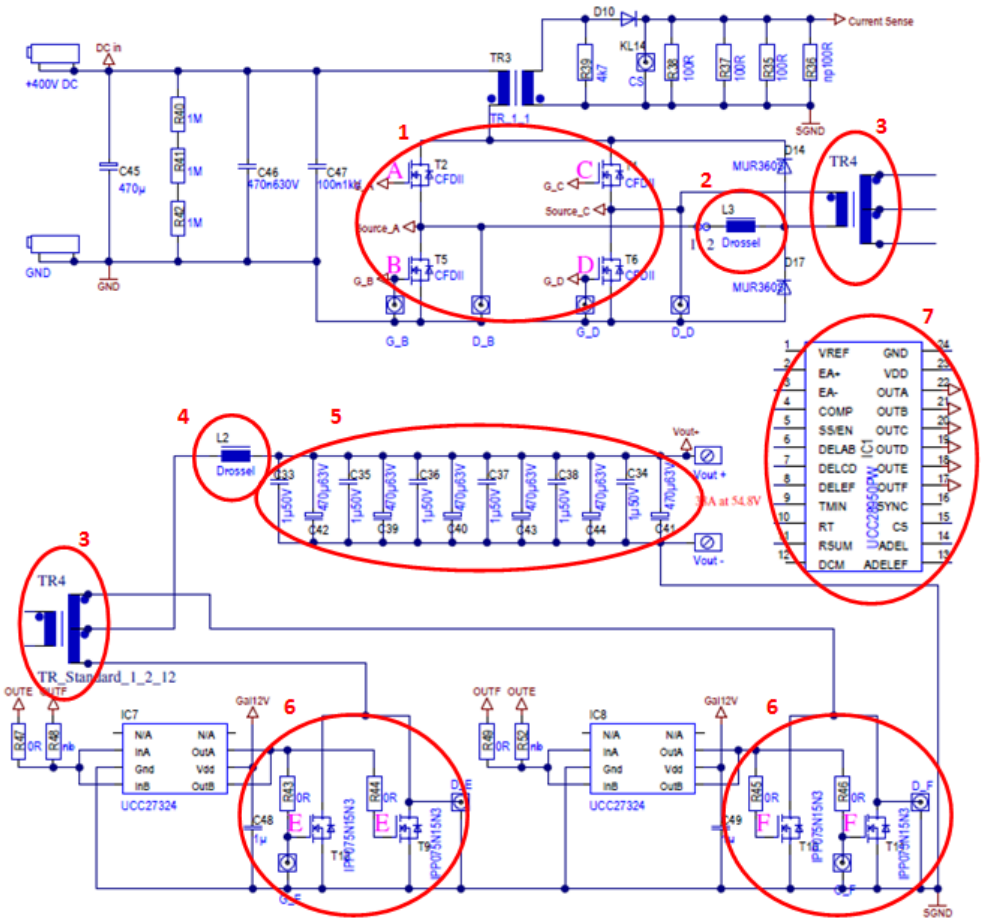

Figure 2: schematic of the IFX board (primary side, secondary side)

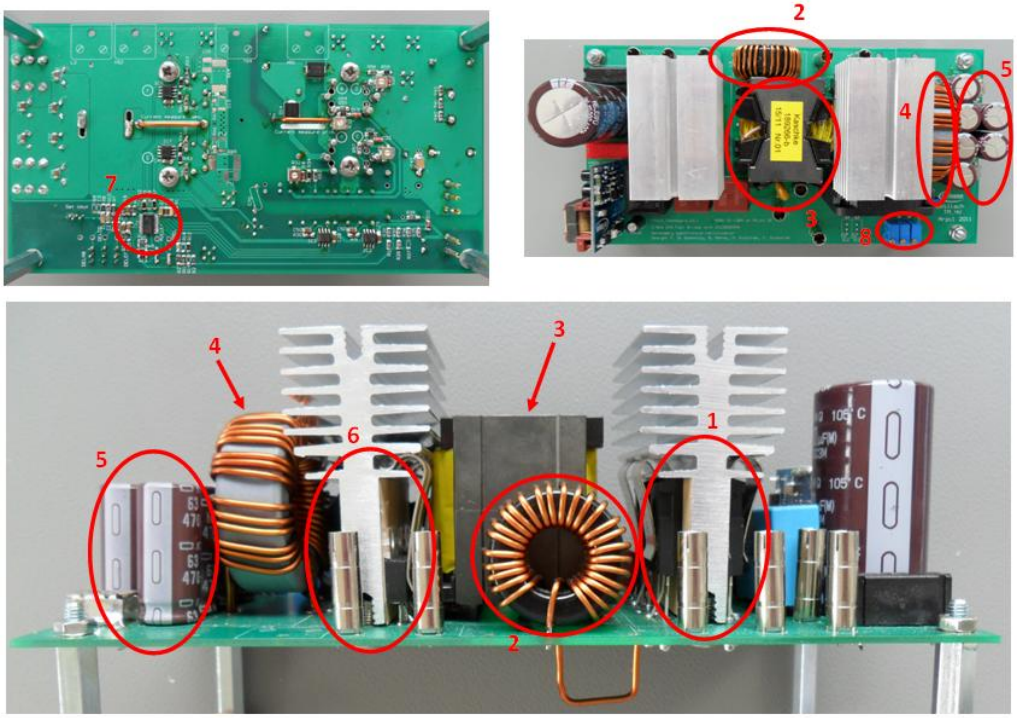

Figure 3: main parts on the IFX board

Figure 2 and Figure 3 illustrate the placement of the main parts in a schematic representation and on the assembled PCB[6].

(1) Primary MOSFETs IPW65R080CFD:

The used switches in the full bridge on the primary side are the new IPW65R080CFD which are most suitable for resonant topologies due to their ease of use behavior, low $R_{DS(on)}$[7] and their integrated fast body diode. This fast body diode is an important feature to prevent failures in the used topology during short circuit, line cycle drop out or burst mode. (MOSFET A, B, C, D)

(2) Resonant inductance:

This resonant inductance is realized using a 77894-A7 Magnetics Inc. Kool-Mμ material. This document is also going to illustrate that it is very important to have a correct dimensioning of this inductance.

(3) Main transformer:

The used main transformer is a PQ40/40 ferrite core, 3C96 material with a winding partitioning of 20 turns on the primary side and 4 plus 4 turns on the secondary side in a center tapped configuration.

(4) Output inductance:

In order to have a low current ripple on the output inductance and taking into account the actual maximum duty cycle available, a value of 18μH has been designed. The used core is a 55083-A2 Magnetics Inc. Molypermalloy material.

(5) Output capacitance:

Low ESR[8] capacitances needed for high efficiency applications (Nippon-Chemicon miniature ultra low impedance LXV series).

(6) Synchronous rectification MOSFETs:
The IFX ZVS phase shift full bridge uses two paralleled OptiMOS™ IPP110N20N3 (200V $V_{(BR)DSS}$[9] with 11mΩ $R_{DS(on)}$). (MOSFET E, F)

(7) Controller for primary and secondary: Texas Instruments UCC28950

(8) Trim potentiometers for adjusting the delay times on the primary and secondary side

After the short explanation of the main parts of the IFX board the next chapter is going to describe the principle of operation of this topology.

3 Principle of operation

This chapter introduces the principle of operation by describing the different phases of the current flow through the circuit on a simplified schematic.

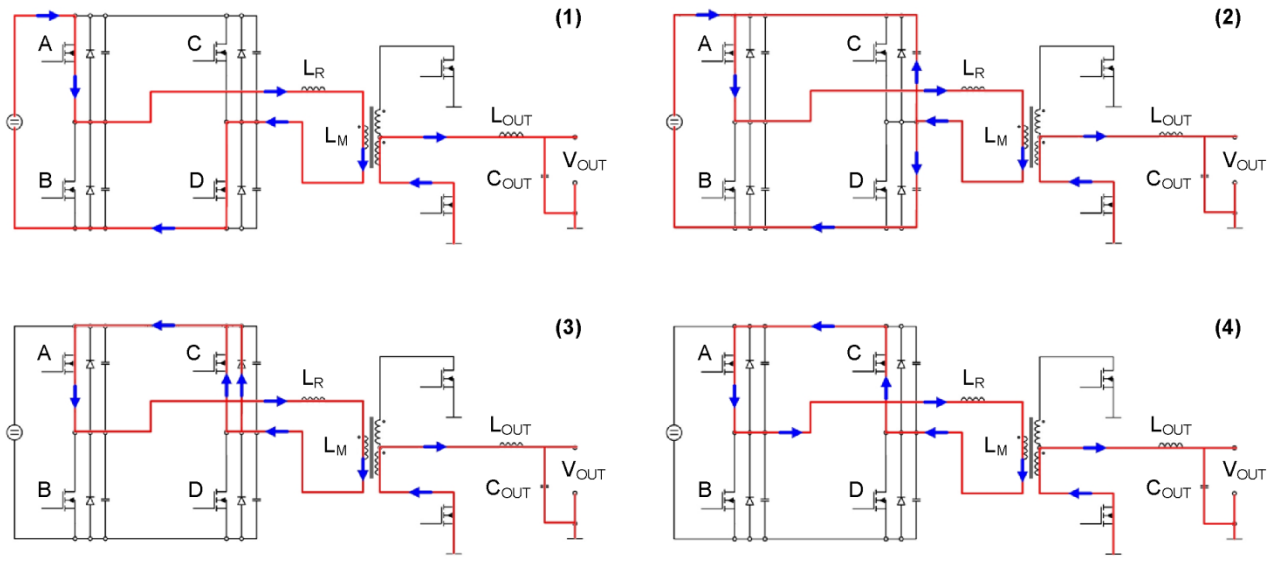

Figure 4: ZVS phase shift full bridge principle of operation phase 1 - 4

(1) Power transfer phase:
MOSFET A and D are turned on and the current is flow looks like in the figure. During this phase the primary current is rising accordingly to the value of the total primary inductance

(2) The second phase is responsible for the zero voltage switching of MOSFET C. In order to reach a zero voltage turn-on the energy stored in the resonant inductance is used to discharge the output capacitance of MOSFET C and charge the output capacitance of MOSFET D.

(3) After the output capacitance of MOSFET C is discharged the current is commutating to the body diode of the MOSFET C. This body diode conduction time should be minimized in order to reduce additional losses.

(4) In phase 4 MOSFET C is actively turned on and the current is flowing through the channel and not through the body diode anymore. This phase is the so called freewheeling phase

(5) In order to start a new power transfer phase MOSFET B is turned ON. This phase is done in the same way as phase 2 by turning off MOSFET A. The output capacitance of MOSFET A is charged and the output capacitance of MOSFET B is discharged before actively switching on the MOSFET.

(6) The body diode conduction time of MOSFET B, which is visible in this phase, should also be reduced to a minimum as in phase 3.

(7) MOSFET B is actively turned on, the current changes its direction and the next power transfer phase starts.

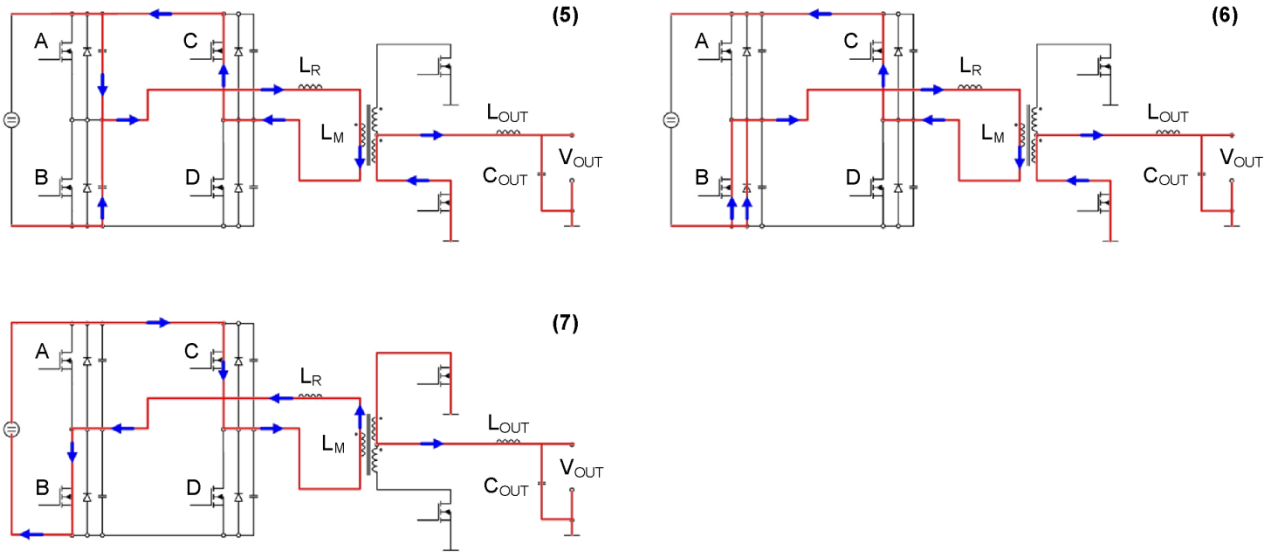

Figure 5: ZVS phase shift full bridge principle of operation phase 5 - 7

The following figure represents the idealized control signals for the primary full bridge, which correspond to the different phases.

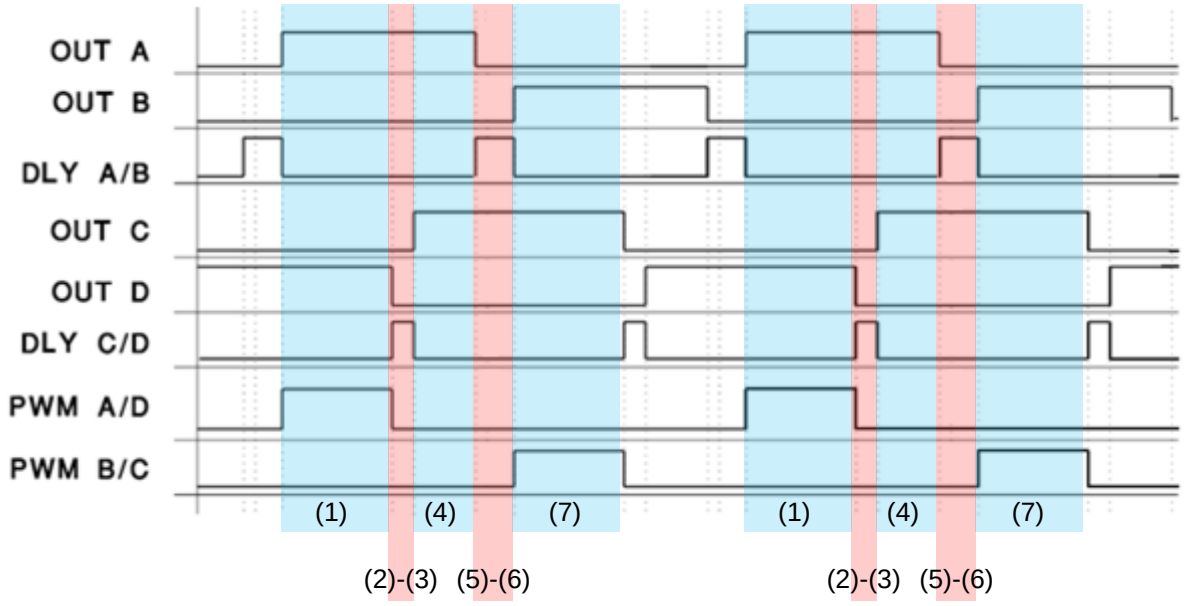

Figure 6: control signals for primary full bridge

Furthermore, figure 6 shows that phase (2)-(3) is much faster than phase (5)-(6). This behavior comes from the available energy which is stored in the resonant inductance to discharge the output capacitance of the MOSFETs. It is easier to achieve ZVS for MOSFETs C and D, since they switch on after a power transfer phase where more energy is stored in the L_R[(10)].

Now that the principle of operation is well known this paper continues with the main part of this document with the design procedure to optimize the board for CFD2.

4 Design procedure

4.1 General design overview

Key points in a ZVS FS FB design are:

- dimensioning of the resonant inductance with reference to the minimum load at which ZVS is required and the output capacitance of the used MOSFETs
- setting of delay or “dead” time between the conduction of the switches on the same leg.
- dimensioning of proper external R_G[(11)] for each switch, taking into account its impact on the commutation behavior
- setting of delay between primary and synchronous rectification MOSFETs conduction, in order to minimize body diode conduction on secondary side
- dimensioning the main transformer in order to guarantee duty cycle availability at any load and input voltage condition, taking into account the actual duty cycle window determined by the combination of the total primary inductance (and so the slope of primary current) with the chosen values of delay times and $R_{G,ext}$[(12)]
- setting the transformer turn ratio in a way to minimize the reverse voltage peak on synchronous rectification MOSFETs, which allows to use the lowest possible V_{DS}[(13)] range and so the lowest possible $R_{DS(on)}$

The main goal of this document is to find the best compromise among these key points based on the characteristics of the used MOSFETs, the new IFX CFD2 series.

Considering the requirements of all recent worldwide standards in matter of light load efficiency, typically the first decision is related to the minimum load where full ZVS is achieved. This mainly involves the resonant inductance design, in combination with delay time and external gate resistances setting.

In order to achieve full ZVS at least at 20% maximum load, the calculated starting values are the following:

$L_R = 52\mu H$	(L_R … resonant inductance)
$R_{G,on}{}^{(14)} = R_{G,off}{}^{(15)} = 5\Omega$	($R_{G,on}$ … external gate resistor at turn-on; $R_{G,off}$ … external gate resistor at turn-off)

This paper is going to show how these settings, needed for ZVS, impact on the actual duty cycle available for the output regulation at any V_{IN}[16] and load condition and how it is eventually possible to find the best compromise for the CFD2 devices.

An important role in high efficiency target achievement is played by the secondary synchronous rectification. In the first design step the synchronous rectification on the secondary side has been disabled, and the rectification is done by using the body diodes of the MOSFETs. The reason for this is to be initially focused only on the primary settings by being independent from the secondary side.

4.2 ZVS behavior: right and left leg

As well known, the two legs of the full bridge behave differently with reference to the ZVS. The right leg starts its transition at the end of a power transfer phase. This means that there is more energy stored in L_R and therefore more energy available to discharge the MOSFETs output capacitance. The left leg starts the transition at the end of a free-wheeling phase, which results in less available energy.

There are two ways to identify each of the two legs. The main indicator whether there is a zero voltage switching or not is the presence of a Miller-plateau on the V_{GS}[17] waveform. The following figure represents a non ZVS behavior of leg A/B clearly visible due to the Miller-plateau.

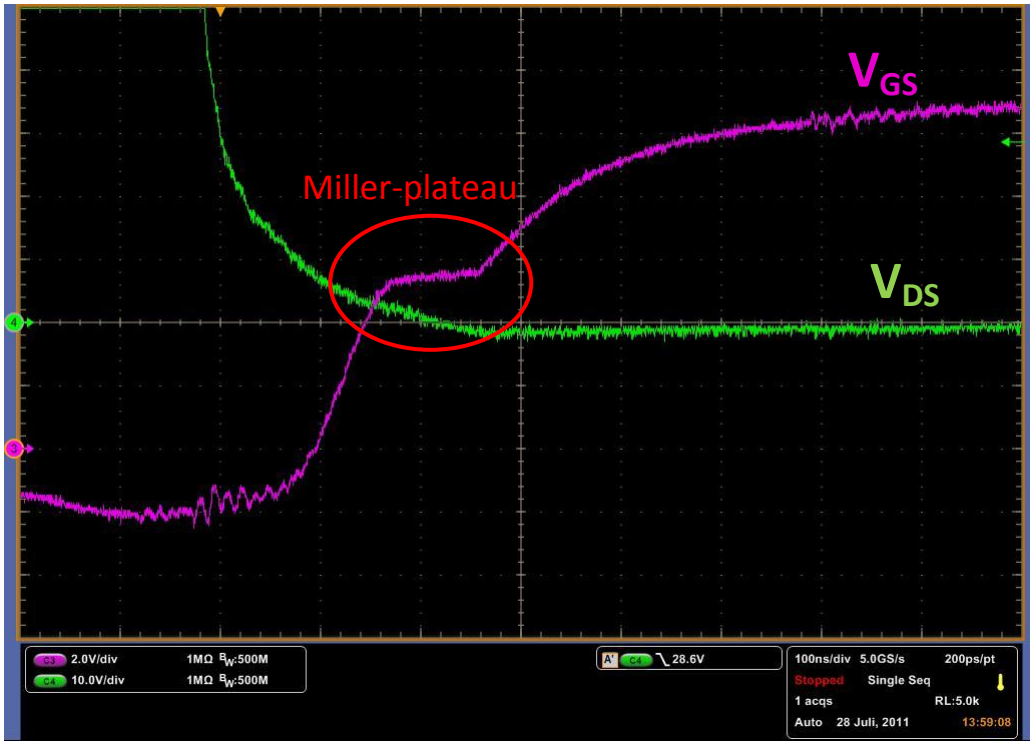

Figure 7: non ZVS behavior of leg A/B

Now it is possible to increase the delay time between MOSFET A and B which results in a shift of the gate signal to the right direction. If it is not possible to remove the Miller-plateau even with the highest delay time, then there is not enough energy stored in the resonant inductance to completely discharge the output capacitance of the MOSFET. In this case it is needed to increase the output load in order to increase this amount of energy: in fact the energy stored in the resonant inductance is depending on the primary current which is also dependent on the output current based on the main transformer turn ratio. After some measurements it was possible to reach a ZVS at P_{OUT}[(18)]=450W with a delay time $t_{del\_A/B}$[(19)]≈520ns. The next figure shows this approach.

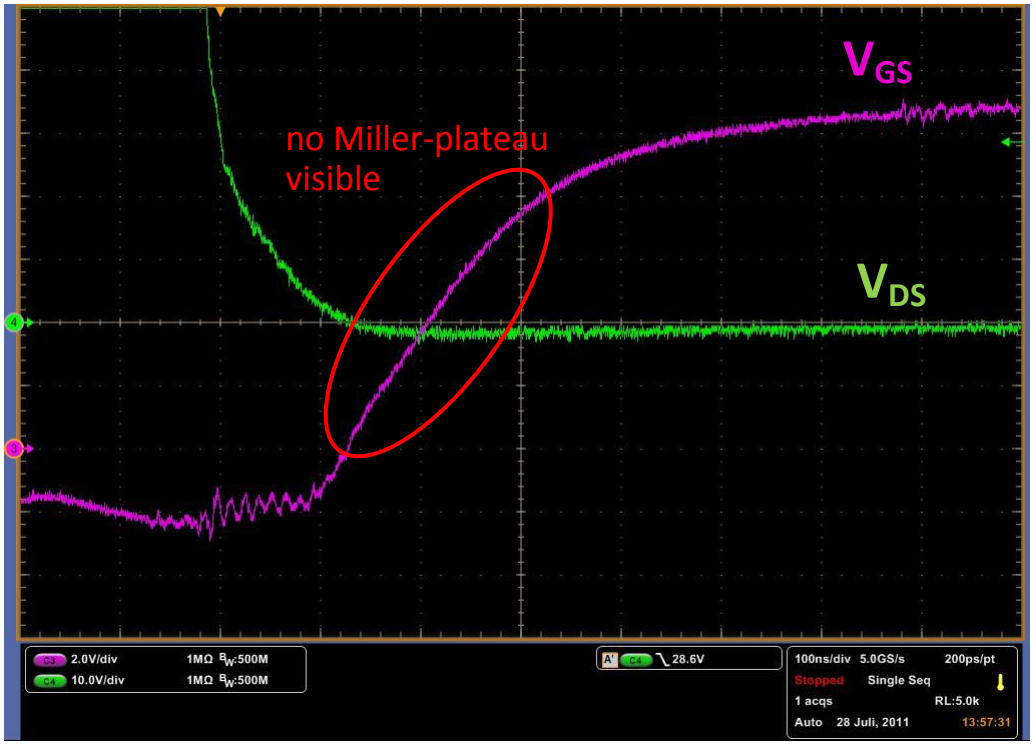

Figure 8: ZVS of leg A/B at 450W output power

Now it is possible to do the same measurement on the second leg C/D. The result of this analysis shows that it is possible to reach ZVS at 320W, so at lower load compared to A/B, because there is more energy stored in L_R.

The second way to analyze the different behavior of the two legs is by looking at the waveforms of the V_{DS} of MOSFET B, MOSFET D and the voltage drop over the main transformer on the primary side. For this analysis it is needed to completely understand the principle of ZVS phase shift full bridge operation. The following figure represents this investigation.

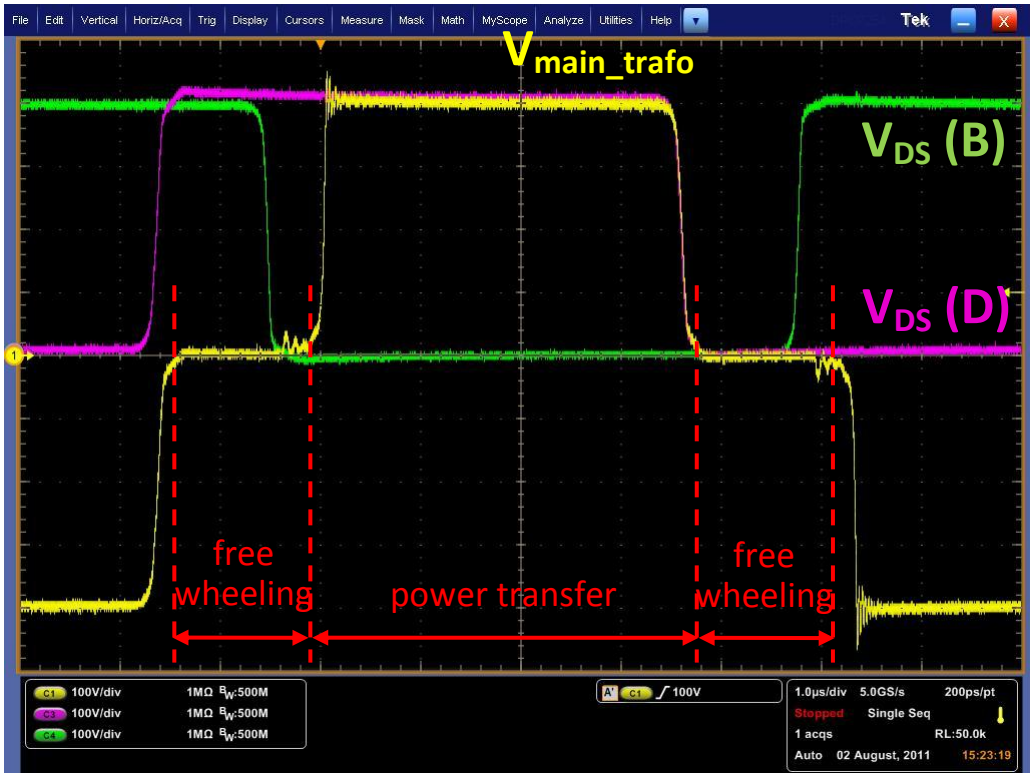

Figure 9: C/D leading leg confirmation

Figure 6 illustrates that a power transfer phase starts with C and B simultaneously ON: the bulk voltage (400V) is applied on the primary side of the main transformer. At the end of this power transfer phase, in sequence MOSFET C switches OFF and then the discharge of the output capacitance of MOSFET D starts by using the energy stored in the total primary inductance: this energy is the maximum possible, because I_{prim}[20] is at its maximum value. It has been demonstrated that the right leg C/D transition starts after a power transfer phase.

After the V_{DS} of MOSFET D is zero, the ZVS turn-on of MOSFET D will take place. At this point a free-wheeling phase starts, where the primary of the main transformer is short circuited, then the MOSFET A turn-on command arrives. In other words, the A/B leg transition starts after a free-wheeling phase, so with lower value of I_{prim} and therefore less available energy to discharge the output capacitance.

Finally, it is possible to say, that this stage has full ZVS at a minimum of 450W on both legs, which corresponds to about 22% of maximum output power. So the first goal regarding the minimum ZVS load is achieved, as per calculation.

The next step is the verification that it is possible to regulate the output voltage at 54VDC up to an output power of 2kW in the assigned range of V_{IN}.

4.3 Output voltage regulation at 54VDC up to 2kW

To ensure that this stage is able to regulate the output voltage V_{OUT}[21] at 54VDC up to 2kW it is necessary to check if there is enough duty cycle available. It is possible to predict the available actual duty cycle by mathematical calculations, but this evaluation is done by the measurement of primary waveforms. In fact, the available duty cycle can be analyzed by measuring the primary current (I_{prim}) and the voltage drop over the main transformer (V_{main_trafo}[22]) on the primary side.

The following figure represents the duty cycle margin available for the regulation at an output load of 8.22A (P_{OUT}≈443W).

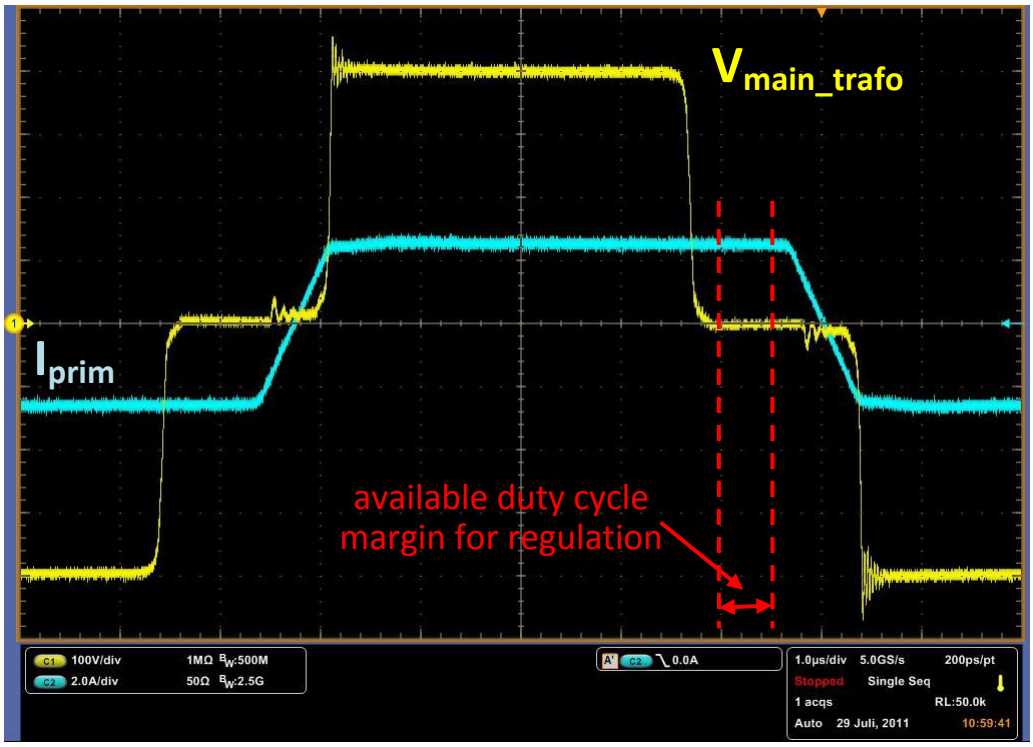

Figure 10: available duty cycle at 443W

The result of an increasing output load is a reduction of the available duty cycle margin which is illustrated in figure 8.

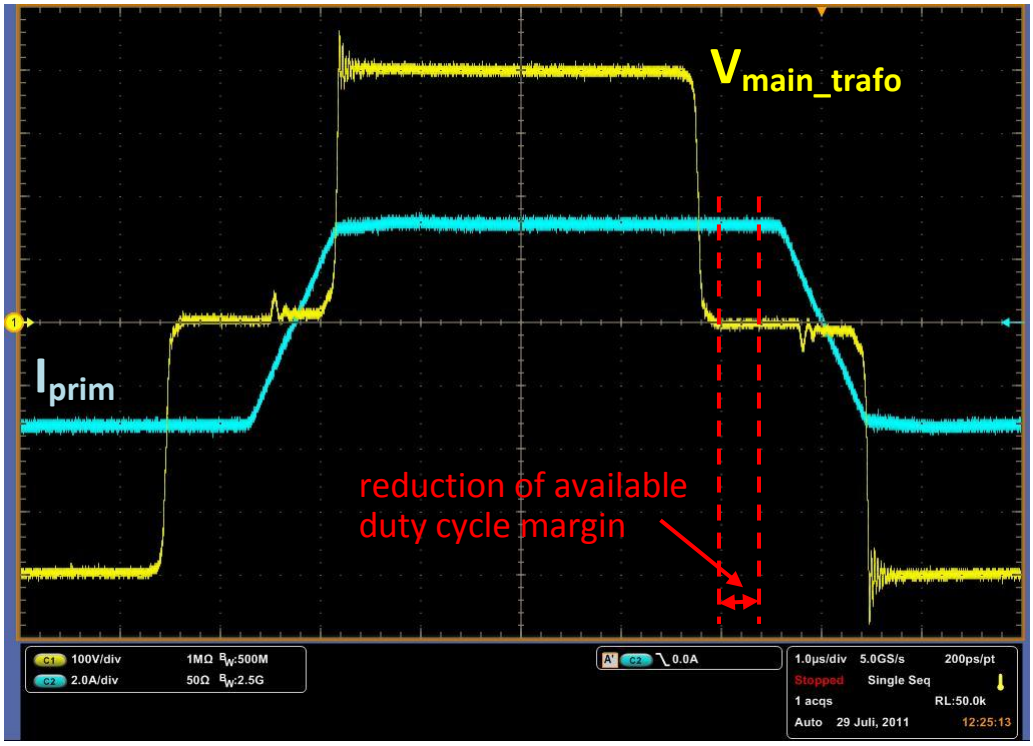

Figure 11: reduction of duty cycle margin at 650W

The next step is to increase the output power up to 2kW. When P_{OUT} reaches about 1183W V_{OUT} begins to decrease, because the max actual duty cycle has been reached: this means that the regulation of the output voltage over 1183W is not possible anymore. The following figure shows the reason for this behavior.

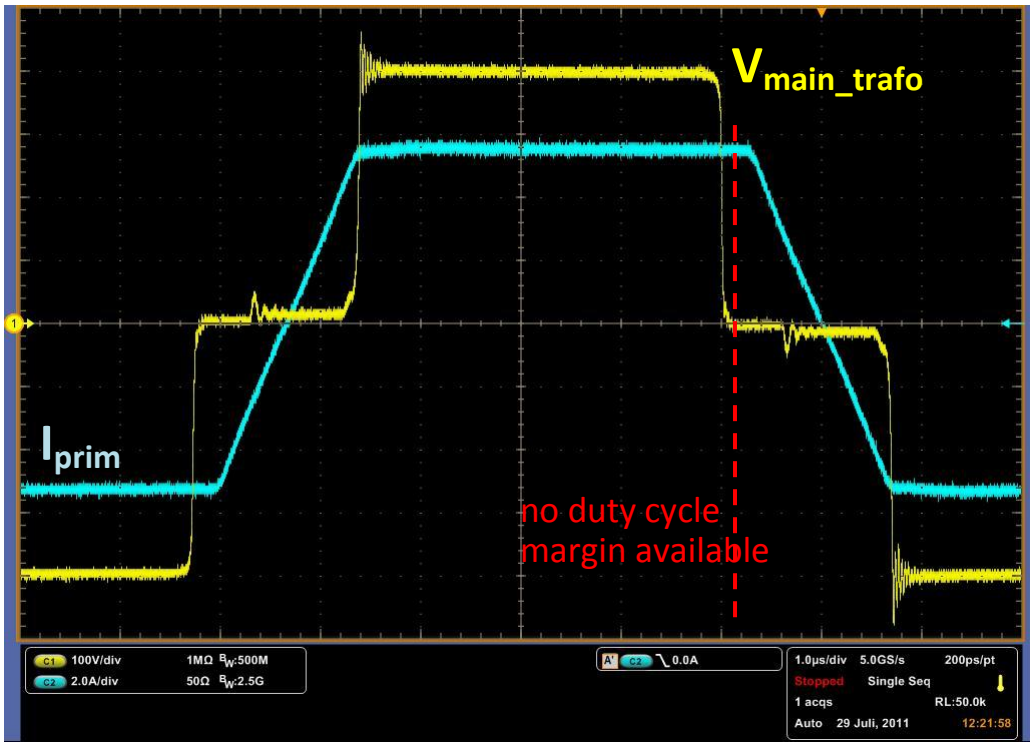

Figure 12: no duty cycle margin available at 1183W

It is clearly visible that the regulation of V_{OUT} is not possible due to the duty cycle limiting. A possible way to recover duty cycle is by reducing the turn-on and turn-off delay times. This reduction can be done by reducing the external $R_{G,on}$ and $R_{G,off}$.

4.3.1 Reduction of external R_G

The ZVS phase shift full bridge has a hard switching turn-off so it is only reasonable to change the external $R_{G,off}$ to 0Ω. $R_{G,on}$ is changed to 2.7Ω and not 0Ω in order to guarantee good commutation behavior.

Due to the change of the external R_G we are able to reduce the total transition time and so extend the available duty cycle window of about 100ns: which leads, after adjusting the delay times, into a regulated load increase of about 100W: this is also not enough for the 2kW stage.

Now the question arises: what else has an influence on the duty cycle?

By analyzing figure 9 there can be only one answer. The best way to gain duty cycle is by increasing the slope of the primary current when changing direction.

4.3.2 Increasing the slope of the primary current I_{prim}

The increase of the slope of the primary current during change of direction can be done by decreasing the inductance in the current path on the primary side This can be realized by declining the amount of primary turns of the main transformer, but this leads also to some drawbacks like increasing the peak voltage on the rectification MOSFETs and an increase of magnetizing current. For this reason this is not an option because it would be necessary to use 250V OptiMOS™ parts for the rectification. These implementation would double the $R_{DS(on)}$ which results in a reduction of efficiency at heavier loads. Another possibility, currently implemented, is to reduce the resonant inductance, in this case from 52uH to 30uH. This change brings a drawback in reaching the ZVS at light load because there would be less energy stored in L_R. After readjustment of the delay times the stage achieves full ZVS on both primary legs at 487W which corresponds to about 24.4% of maximum load. This value can be considered still acceptable.

The following figure shows the slope difference between a L_R=52µH and L_R=30µH at 1283W.

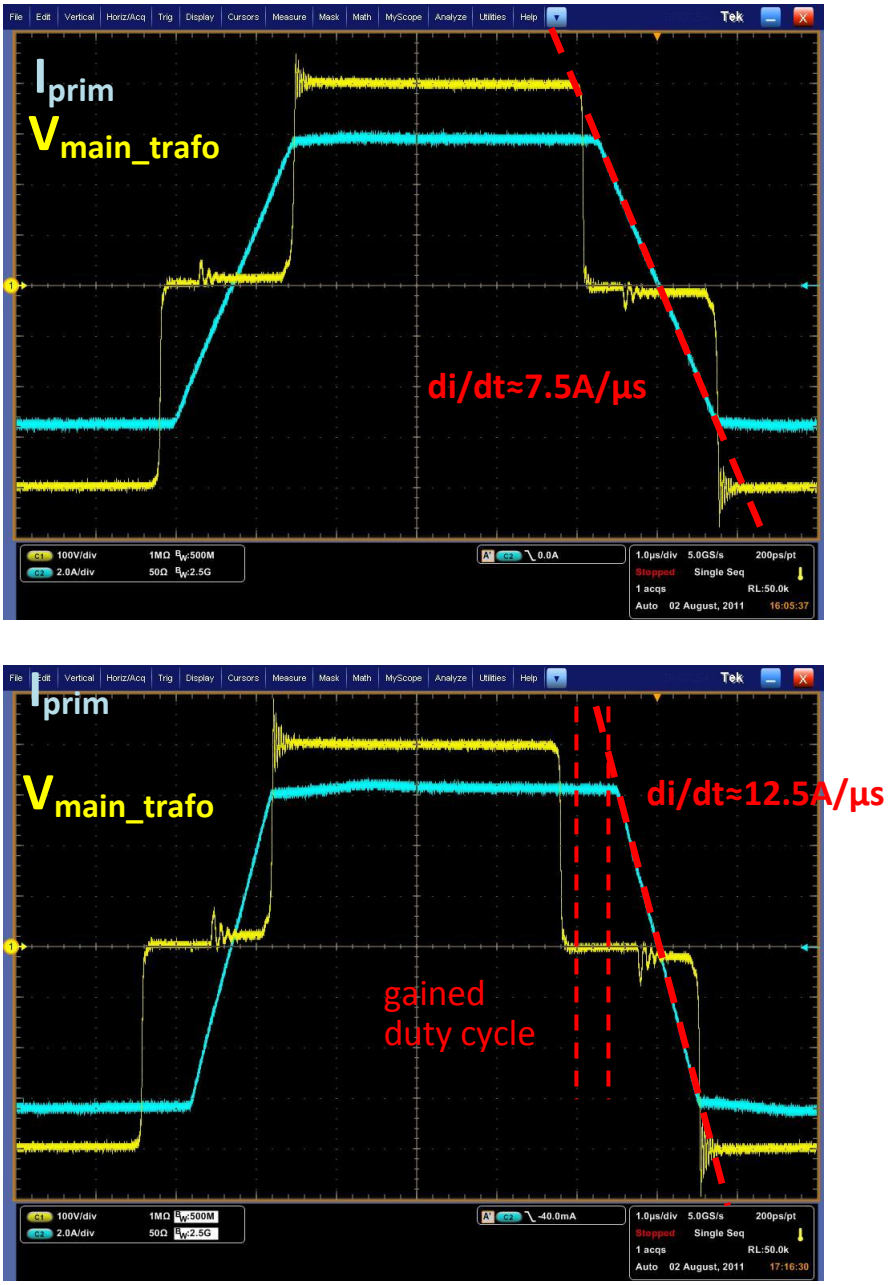

Figure 13: I_{prim} comparison with L_R=52µH (upper) and 30µH (lower)

It is clearly visible that with 52µH there is a di/dt of about 7.5A/µs in comparison to 30µH with a di/dt of about 12.5A/µs. This gives enough duty cycle margin for reaching 2kW output power.

Figure 11 represents the primary current and the voltage drop over the main transformer when the converter is running at 2kW with 54VDC output voltage.

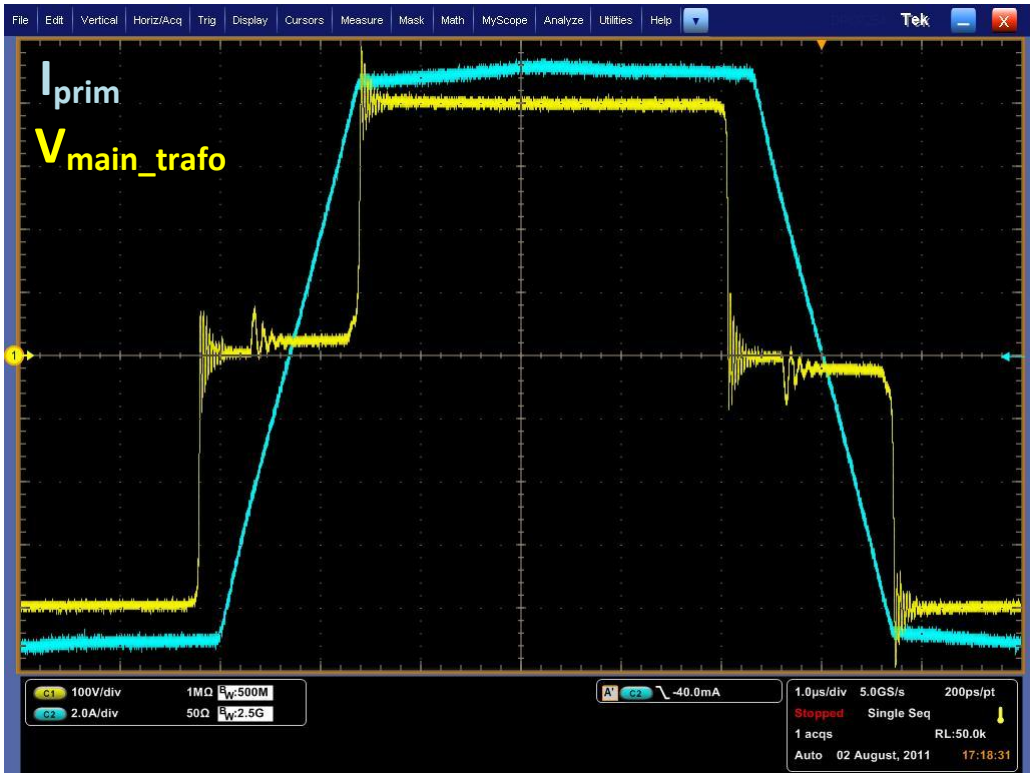

Figure 14: IFX ZVS phase shift full bridge running at 2kW with 54VDC output voltage

All these measurements were done using diode rectification in order to be firstly focused on primary settings, without influence from the secondary stage. Now the synchronous rectification is going to be activated.

The next chapter is going to explain how it is possible to optimize the delay times for the synchronous rectification and by the end the efficiency curve over the whole load range will be represented.

4.4 Synchronous rectification

In order to optimize the delay time for the synchronous rectification (SR[23]) MOSFETs, with the goal to finally get the best possible efficiency, it is necessary to actively switch the MOSFETs on and off so that the current is flowing as long as possible through the channel and not through the body diode. For safety reasons the delay time must be adjusted at the minimum load at which the synchronous rectification is activated. Otherwise there is a risk of destruction of the parts when decreasing the load due to an overlap of V_{GS} and V_{DS}.

Figure 12 shows an example where the delay time is not optimized.

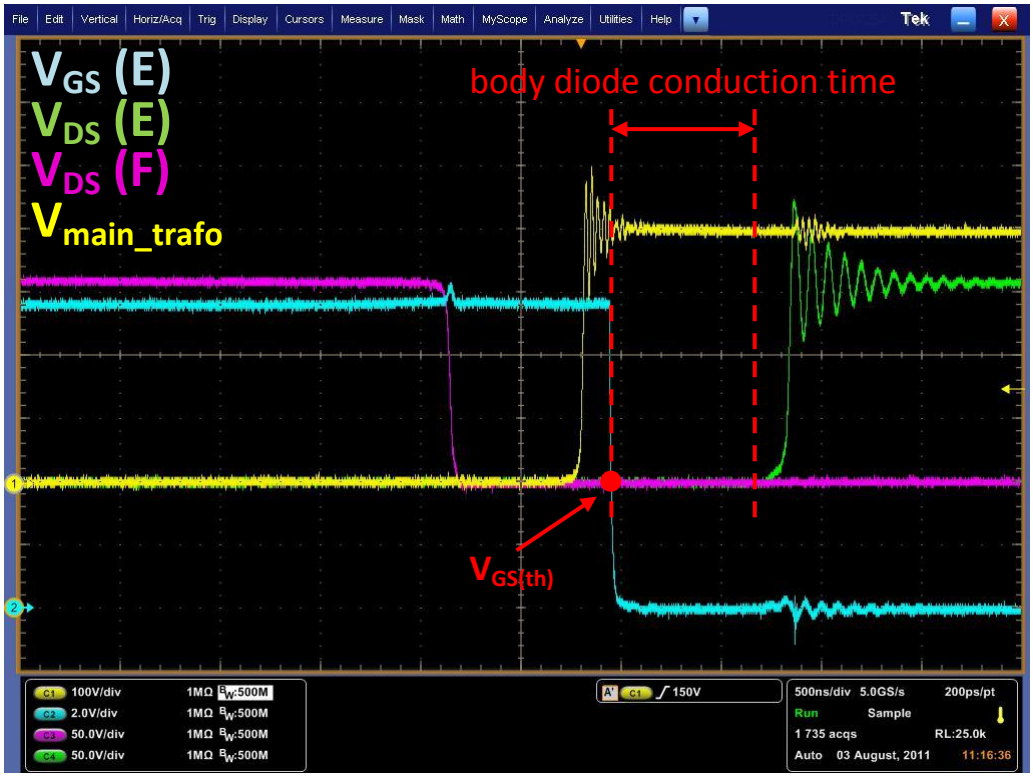

Figure 15: delay on SR not optimized

As mentioned before, to optimize the delay of the synchronous rectification it is necessary to reduce the body diode conduction time. To do this we can adjust the delay time in order to shift the turn off of the MOSFET E as close as possible to the point when the V_{DS} of MOSFET E starts to increase (figure 16).

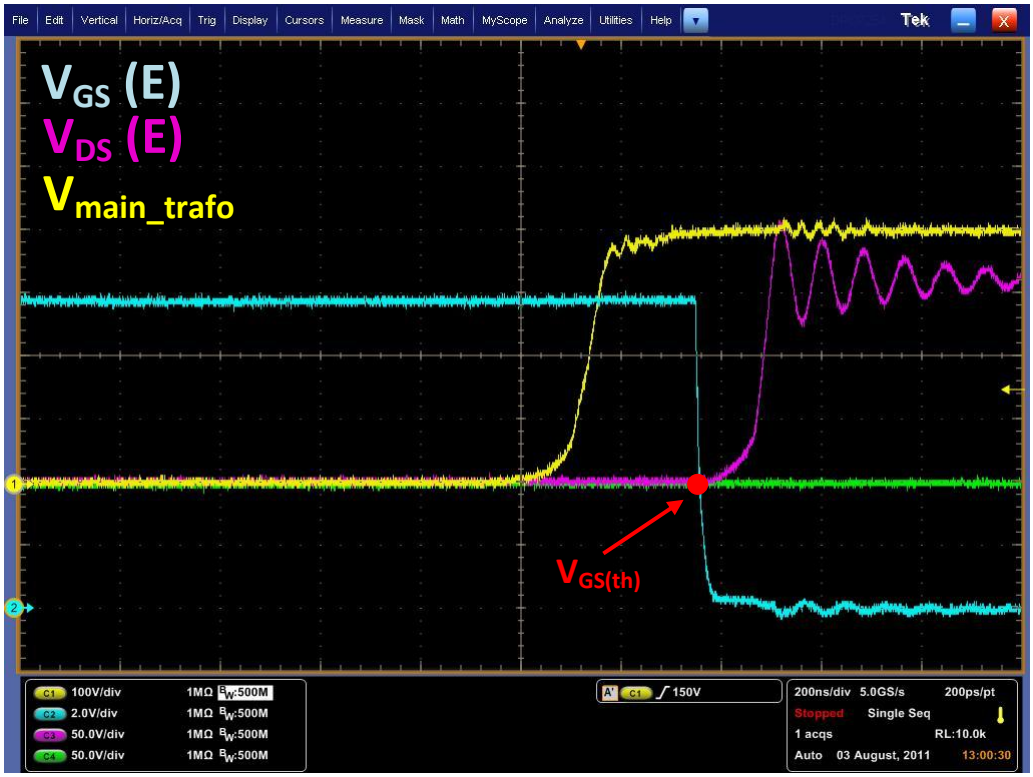

Figure 16: delay on SR optimized

Why is it necessary to do this measurement at the minimum load when the synchronous rectification starts to operate? At heavier loads the front of V_{DS} of MOSFET E is shifting in the right direction. By adjusting the delay time at heavier loads and then decreasing the load leads to a shift of V_{DS} in the left direction which results in a V_{GS} and V_{DS} overlap. This can destroy the part because the channel is still on when the V_{DS} is ramping up

The last figure of this application note illustrates the efficiency curve after optimization of the synchronous rectification.

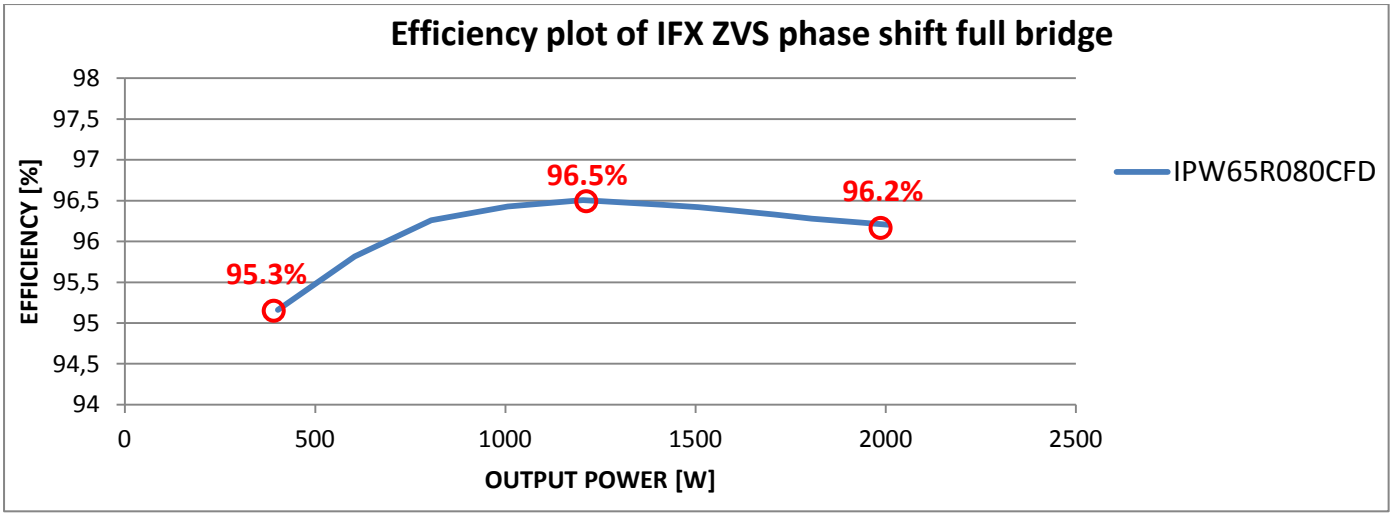

Figure 17: efficiency of IFX ZVS phase shift full bridge with IPW65R080CFD

4.5 Benefits given by CFD2 technology in ZVS board design

As mentioned in the introduction, the main benefits of CFD2 technology have been already described in details in the application note "650V CoolMOS™ CFD2" released by Infineon in February 2011. In this paragraph the special features making CFD2 attractive for ZVS phase shift full bridge are highlighted.

First of all, CFD2 has been introduced with the goal to reduce the typical $Q_g^{(25)}$ by 30% over the whole $R_{DS(on)}$ range compared with previous CFD (see figure 18).

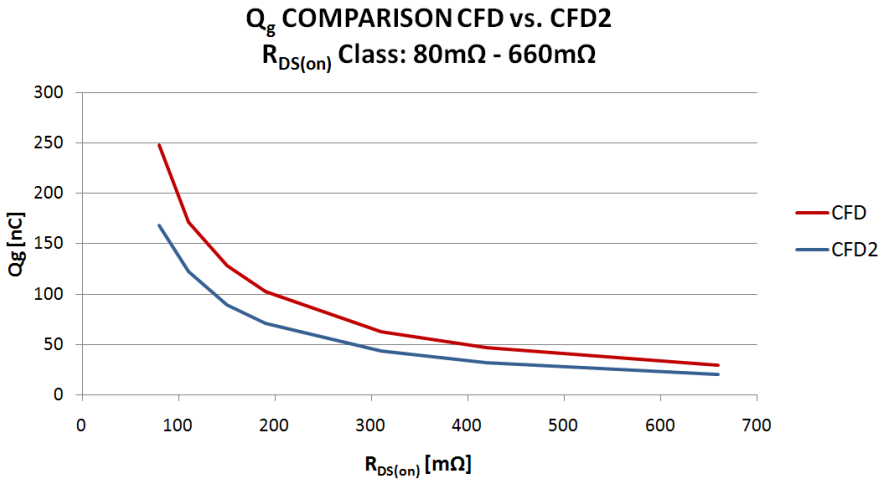

Figure 18: Q_g comparison CFD2 vs. CFD

The graph below (figure 19) shows the impact of Q_g by the increase on the ZVS window.

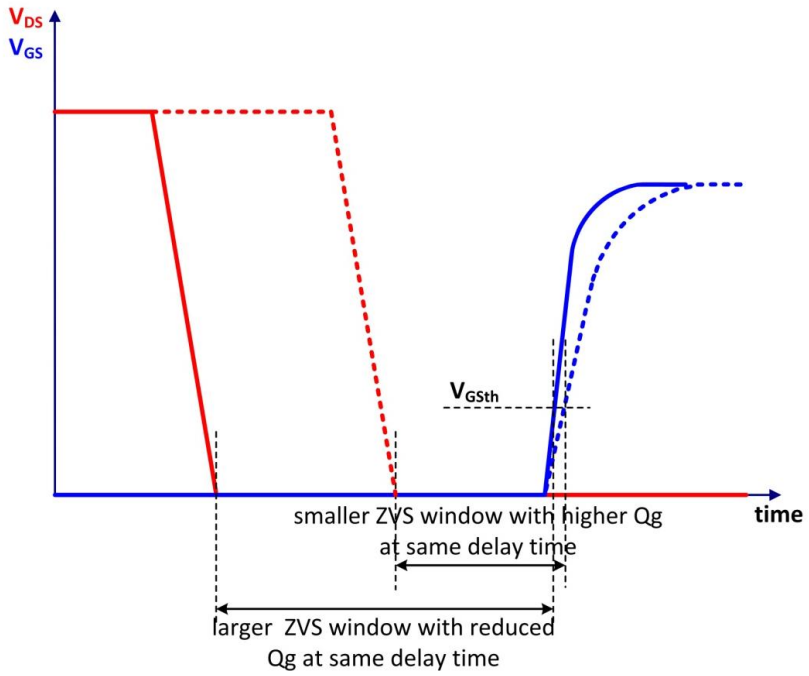

Figure 19: simplified ZVS window depending on Q_g at same delay time

The figure illustrates that with a lower Q_g a larger ZVS window is given with the same delay time at turning OFF. On the other way around, it allows to decrease the delay time keeping the same ZVS window, which also gives the benefit to increase the actual duty cycle and to shorten the conduction time of the body diode.

It is possible to demonstrate by calculation that, in IFX ZVS Board, by using $R_{G,off}$=0Ω. $R_{G,on}$=2.7Ω the reduction of 30% of Q_g leads to a reduction of the total transition time by around 50nsec, which means around 1% of increase of actual maximum duty cycle. This means also more margin in available regulation window and lower $I_{prim(rms)}$, which results in a reduction of conduction losses and increase in efficiency especially at maximum load where conduction losses are the most important part, as showed in the figure below:

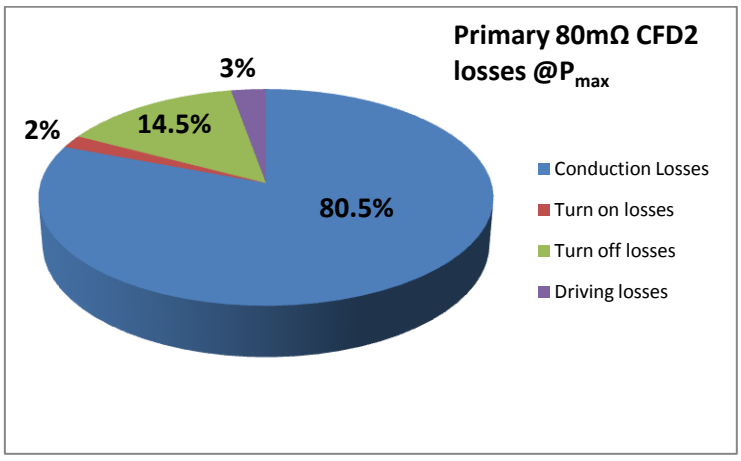

Figure 20: losses spread of the primary MOSFETs at P_{max} [26]

Moreover, in the following figure, it is possible to see the losses spread on each full bridge MOSFET at 10% of maximum load:

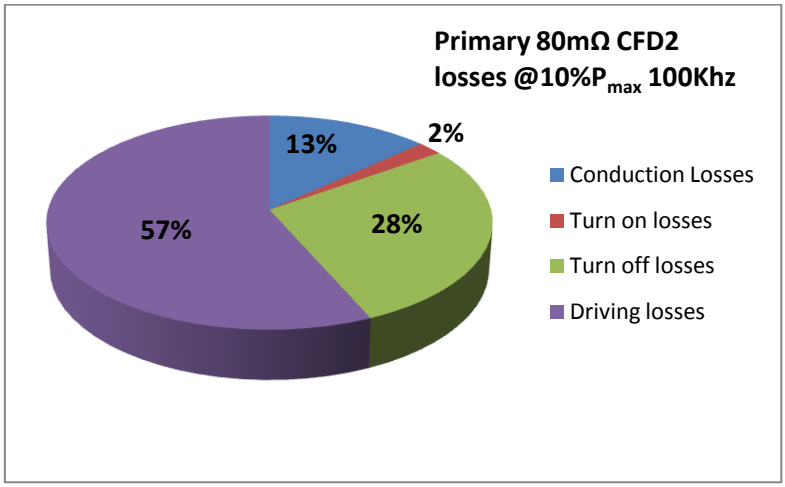

Figure 21: losses spread of the primary MOSFETs at 10% of P_{max}

So at 10% of maximum load the driving losses are most important and Q_g is the key parameter in the driving losses: in IFX board specific application, it has been calculated that a reduction of Q_g by 30% leads to an increase of efficiency by 0.3% at 10% P_{max}.

The same benefit at light load comes from the reduced E_{OSS}, parameter more related the V_{DS} transition time, which contributes together with the turn-off delay time (Q_g related) to the total transition time (so called "ZVS window").On the other way around, having assigned the minimum load for the ZVS (in our case 24%P_{max}), using devices with bigger E_{OSS}[27] involves the use of higher value of L_R.

The second important benefit given by CFD2 technology is the reduction of the typical t_{rr}[28] of the body diode.

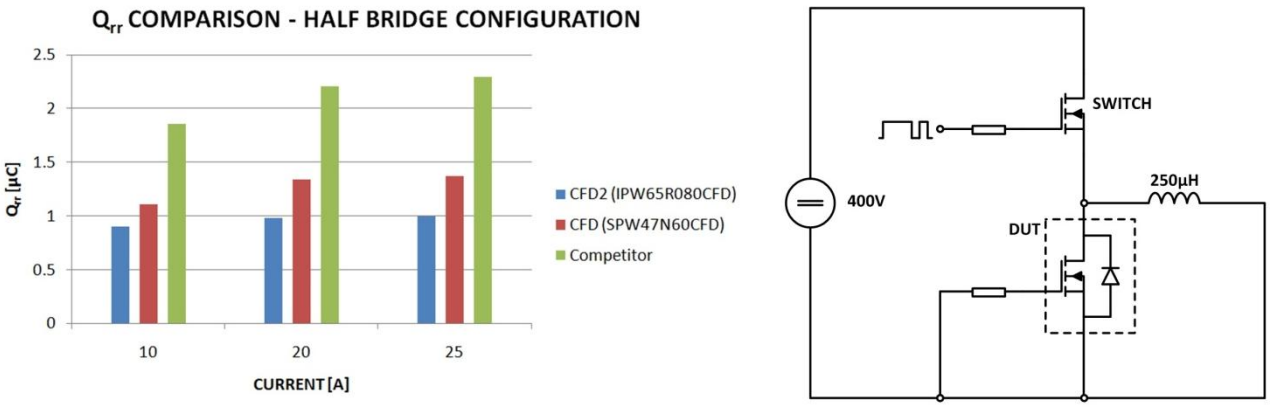

Figure 22: Q_{rr} comparison of low side MOSFET in a half bridge configuration

The diagram in figure 22 illustrates the Q_{rr}[29] value of CFD2 in comparison to CFD and a competitor technology by showing the example of 80mΩ product. It is visible that CFD2 has the lowest Q_{rr} values from 10A to 25A in a half bridge configuration with a supply voltage of 400V. The high side switch is used to load the inductance to the specified current. After switching OFF the high side MOSFET the current is commutating to the body diode of the low side MOSFET which corresponds to the device under test.

This second feature brings benefits in efficiency by reducing the losses due to body diode conduction, but also improves the reliability of this device under critical working conditions, like start-up, overload or short circuit protection, burst mode operation, in which the body diode is heavily involved. It has been demonstrated, that in these conditions a key parameter to guarantee safe operation is the t_{rr} of the body diode, which must be as low as possible. This topic has been widely described by the technical literature and is out of the scope of this paper.

4.6 Further improvement: adaptive delays setting

By using special features available in standard controllers (like the UCC28950 from TI) or DSPs it is possible to adapt the primary and secondary delay times in function of the output load. In particular, as the load increases, the $t_{del\_A/B}$ and $t_{del\_C/D}$[30] will be accordingly decreased on the primary side while the delay time on the synchronous rectification MOSFETs will be increased. This will allow reducing the body diode conduction time to a minimum, both on the full bridge and the synchronous rectification MOSFETs, helping to further optimize the efficiency under any load condition. In fact, this “adaptive delay” has been only simulated in our investigations by optimizing by trimmer the SR delay time only at the load corresponding to the maximum efficiency area (800W), which resulted in further ~0.2% increase of efficiency.

The second advantage of the adaptive delay is that it allows gaining additional duty cycle portions, useful for the regulation at maximum load, therefore increasing the design margin room versus the possible tolerances in the main transformer construction and coupling.

5 Summary

In the present paper the performance of the new CFD2 CoolMOS™ MOSFET (IPW65R080CFD) in a 2kW ZVS phase shift full bridge converter (IFX board) has been analyzed.

General guidelines about the design optimization have been given with the purpose to get the maximum possible benefit out of this new device’s usage. In fact this document has to be considered as natural extension of the “Application Note - 650V CoolMOS™ CFD2” released by Infineon in February 2011.

By using fixed delay times both on primary and secondary sides a peak efficiency of 96.42% has been achieved. It can be increased up to 96.6% using adaptive delay setting. Moreover full ZVS has been guaranteed down to around 24% of maximum load.

6 List of Abbreviations

(1)	ZVS	…	zero voltage switching
(2)	IFX	…	Infineon Technologies AG
(3)	MOSFET	…	metal oxide semiconductor field effect transistor
(4)	$R_{G,ext}$	…	external gate resistor
(5)	DC	…	direct current
(6)	PCB	…	printed circuit board
(7)	$R_{DS(on)}$	…	drain-source on-state resistance
(8)	ESR	…	equivalent series resistance
(9)	$V_{(BR)DSS}$	…	drain-source-substrate breakdown voltage
(10)	L_R	…	resonant inductance
(11)	R_G	…	gate resistor
(12)	$R_{G,ext}$	…	external gate resistor
(13)	V_{DS}	…	drain-source voltage
(14)	$R_{G,on}$	…	external turn-on gate resistor
(15)	$R_{G,off}$	…	external turn-off gate resistor
(16)	V_{IN}	…	input voltage
(17)	V_{GS}	…	gate-source voltage
(18)	P_{OUT}	…	output power
(19)	$t_{del\_A/B}$	…	delay time between MOSFET A and B
(20)	I_{prim}	…	primary current
(21)	V_{OUT}	…	output voltage
(22)	V_{main_trafo}	…	voltage drop over main transformer on primary side
(23)	SR	…	synchronous rectification
(24)	$V_{GS(th)}$	…	gate-source threshold voltage
(25)	Q_g	…	gate charge
(26)	P_{max}	…	maximum load
(27)	E_{oss}	…	energy stored in output capacitance of the MOSFET
(28)	t_{rr}	…	reverse recovery time
(29)	Q_{rr}	…	reverse recovery charge
(30)	$t_{del\_C/D}$	…	Delay time between MOSFET C and D