100 W (19 V/5.26 A) TV adapter demonstrator with IDP2303A

About this document

Scope and purpose

This document describes the 100 W (19 V/5.26 A) 90 V_{AC} ~ 265 V_{ac} input off-line PFC - LLC converter demoboard featuring Infineon's digital PFC - LLC combi controller IDP2303A and MOSFETs IPA60R230P6, IPD50R380CE and BSC067N06LS3G.

Intended audience

This document is intended for users of the IDP2303A who wish to design a PFC plus LLC converter with a non-auxiliary power supply for TV adapter applications .

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Abstract

1 Abstract

The demoboard described in this document is a 100 W TV adapter using a digital PFC-LLC combi controller (the IDP2303A), which is the second generation of digital combi controller with a 16-pin package developed by Infineon Technologies. The IDP2303A is specially designed for TV adapter switch mode power supply applications.

The IDP2303A is a highly integrated multi-mode power factor correction (PFC) and half bridge LLC (HB LLC) controller. Multi-mode operation of the PFC controller and zero voltage switching of the LLC MOSFETs can significantly increase the power conversion efficiency, especially light load efficiency, while the system costs are minimized by the integrated high-voltage start-up cell, regulator for the PFC converter, MOSFET drivers and internal communication between the PFC and LLC controllers. The auxiliary power supply can be eliminated by the integrated high-voltage start-up cell and advanced burst mode control. With an active X-CAP discharge function, low stand-by power consumption during burst mode is supported. A comprehensive set of built-in protection features can greatly enhance the system operation and safety. Up to 40 different parameters ensure flexibility during system design and achieve optimal performance. All of these features make the IDP2303A a very competitive AC-DC controller for PFC-HB LLC resonant converters.

For TV adapters, high power density with high effiency is the market trend and Infineon CoolMOS™/OptiMOS™ is used to minimize power loss. The IPA60R230P6 is used in the PFC stage for its low switching and driving losses. DPAK Power MOSFETs are used in the LLC stage of this reference design for the advantage of component thickness and also the ease of the assembly process. Meanwhile, two BSC067N06LS3G are used for the synchronous rectifier due to their compact dimensions.

2 Demonstrator board

This document contains a list of features, the power supply specification, schematic, bill of material and the transformer construction documentation. Typical operating characteristics such as performance curves and oscilloscope waveforms are shown at the end of the document.

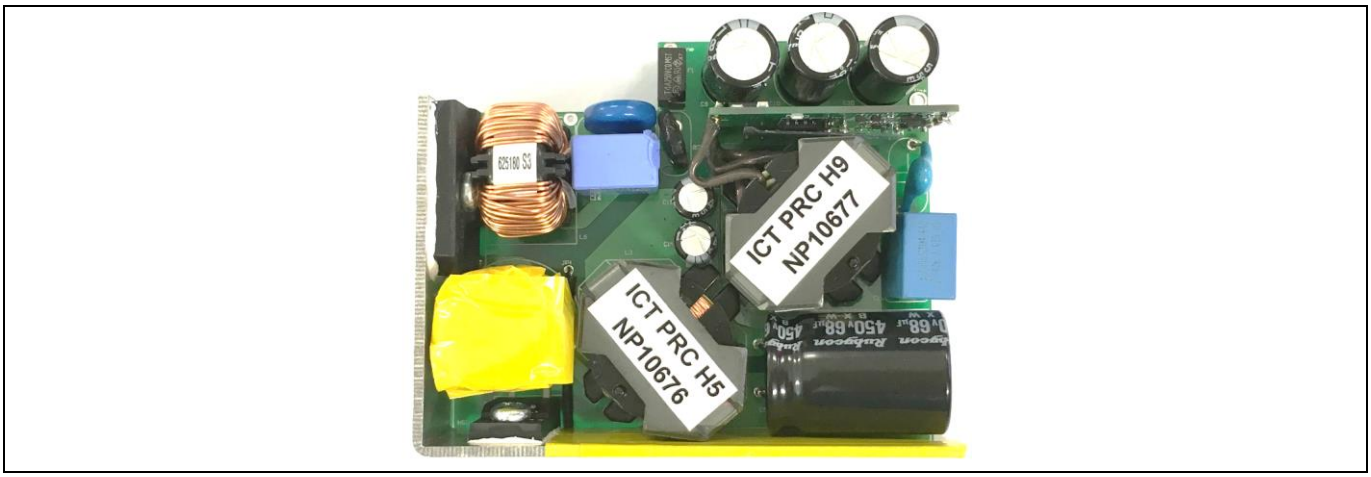


Figure 1 DEMO-IDP2303A-100W PFC+LLC converter (top view)

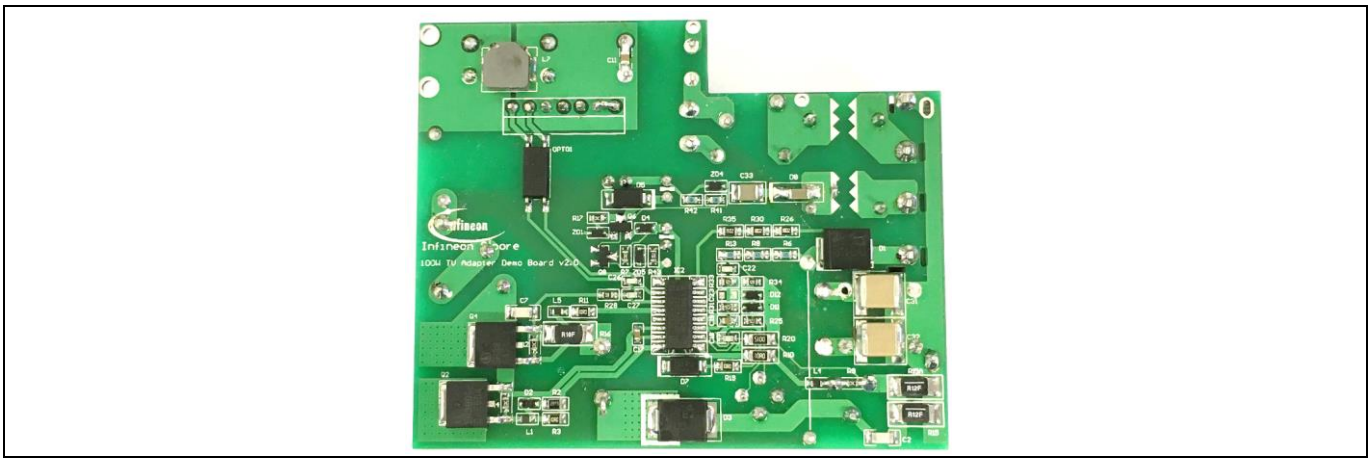


Figure 2 DEMO-IDP2303A-100W PFC+LLC converter (bottom view)

3 Specifications of demonstrator board

Table 1 Specifications of DEMO-IDP2303A-100W

Input voltage	90 V_{AC} ~ 265 V_{AC}
Input frequency	50 / 60 Hz
Output load	Full load : 19 V 5.26 A; Min load : 19 V 0.1 A Stand by load : 19 V/8 mA
Power efficiency	>88.3% @115/230 V_{AC}
Power factor	>0.95 (230 V_{AC})
Controller IC	IDP2303A
PFC / LLC MOSFET	IPA60R230P6, IPD50R380CE & BSC067N06LS3G
Form factor (L x W x H)	77 mm x 63 mm x 28 mm

4 Features of IDP2303A

Table 2 Features of IDP2303A

Integrated 600 V start-up cell
Integrated floating driver for HB high-side MOSFET
Multi-mode operation of PFC
Integrated PIT regulator for PFC controller
Active X-CAP discharge function supports low stand-by power consumption
Comprehensive set of PFC/LLC protection features
Internal communication between PFC and LLC controller
Plenty of configurable parameters and failure protection modes
UART interface for communication and in-circuit configuration
Adaptive burst mode
Low ripple during standby
Low standby power
Parameter patching during DV/PV/production

5 Circuit description

5.1 Introduction

The circuit consists of two power stages; a front-end PFC pre-regulator and a half bridge LLC resonant converter based on the IDP2303A controller.

5.2 Mains input and rectification

The AC line input side comprises the input fuse F1 as an over current protection device. The X capacitor (C16), choke (L6), and Y capacitor (C24) form a mains filter to minimize the feedback of RFI into the main supply. An NTC thermistor (R21) is placed in series with the input to limit the initial peak inrush current.

5.3 Multi-mode PFC converter

After the bridge rectifier, there is a boost type PFC converter consisting of Q3, D3, L3 and C5. A CoolMOS™ IPA60R230P6 is used as the power switch Q3. Due to its low R_{dson} and low output capacitance, the MOSFET conduction and switching loss can be effectively reduced. Output capacitor C5 provides energy buffering to reduce the PFC output voltage ripple.

The PFC choke current is sensed by the external shunt resistors R15 and R15A. The sense voltage is fed into the CS0 pin and compared to the internal voltage level for current limiting.

Multi-mode operation is implemented by the IDP2303A. Based on constant on time control, it does not require a direct sine wave reference signal. At heavy loads, it is beneficial for the PFC to work in CrCM mode. However, with CrCM operation, the PFC switching frequency may increase to quite a high value at light load, which leads to high switching losses. In this controller, the PFC can lower the switching frequency by adding an additional delay into each switching cycle through selecting further PFC MOSFET drain-source voltage valleys to achieve QR2, QR3 and up to QR10 operation. In this way, the switching frequency is limited between a minimum and maximum value.

The IDP2303A provides enhanced PFC output overvoltage protection with two different levels. Thus, it can effectively monitor and protect the PFC bus voltage against any overshoot in the case of abrupt load or input voltage variations.

The IDP2303A features VS pin open loop protection, which can effectively protect the whole system in the case of the VS pin external high side resistor becoming open circuit.

Brown-in and brown-out protections are provided with the integrated startup cell via the HV pin to avoid the system working at extremely low AC input.

In order to meet the increasingly stringent system safety requirements, the IDP2303A also features VS pin open circuit protection and VS pin short to adjacent pin protection.

In addition, the IDP2303A features long term continuous conduction mode protection, which can help to protect the whole system in the case of a shorted PFC bypass diode or heavy load condition.

5.4 Half bridge LLC resonant converter

The second stage is a half bridge LLC resonant converter, operating with zero-voltage switching. The PFC-LLC combi controller (IDP2303A) incorporates the necessary functions to drive the half bridge's high side and low side MOSFETs (Q2 and Q4) with a 50% duty cycle including a configurable dead time. The switching frequency can be changed by the IDP2303A to regulate the output voltage against the load and input voltage variations.

During operation, the primary MOSFETs Q2 and Q4 are turned-on under a ZVS condition and the secondary rectified MOSFETs, Q1 and Q5, are turned-on and turned-off under a ZCS condition. Hence, high power conversion efficiency is achieved.

As the IDP2303A has the half bridge high side MOSFET driver built-in, based on Infineon's coreless transformer technology, there is no requirement to add an external driver module, such as a pulse transformer or driver IC to drive the high side MOSFET. Hence, the system BOM cost and design effort is greatly reduced.

The mains transformer (TR1) uses a magnetic integration approach, incorporating the resonant series and shunt inductances. Thus, no additional external coils are required for resonance. The transformer configuration for the secondary winding is center-tapped, and the output rectified MOSFETs, Q1 and Q5, are OptiMOS™, in order to reduce the power loss.

The voltage across the half bridge shunt resistor (R16) is fed into the CS1 pin of the IDP2303A. Thus, the current flowing through the primary winding is strictly controlled to ensure the system max power limitation and over current protection.

Since the IDP2303A has an internal voltage reference and pull-up resistor for the HBFB pin, the feedback signal from the opto-coupler (OPTO1) can be directly fed into this pin, which also minimizes the BOM cost and design effort. Thus, with the feedback information, the IDP2303A is able to regulate the LLC frequency to achieve the LLC load regulation and line regulation.

In the case of an overload condition, the HBFB pin voltage will rise and may reach $V_{\_OlpHB}$, which will trigger the overload protection. As a result, the LLC will stop switching after a blanking time and enter the auto-restart mode, with a configurable break time to protect the whole power supply system.

In the case of an extremely light load condition, the voltage on the HBFB pin may drop and reach another threshold ($V_{\_burst\_enter}$), which will cause the LLC to stop switching and enter the burst mode after a blanking time. When the voltage on the HBFB pin increases to reach the threshold $V_{\_burst\_on}$, the LLC will resume switching. Thus, at extremely light load conditions, with this burst mode feature, the LLC output will still be under regulation. When a heavy load is applied, the HBFB pin voltage exceeds $V_{\_burst\_exit}$ or the burst off time reaches its minimum setting $t_{\_burst\_off\_min}$, the LLC will leave burst mode and resume normal operation.

To achieve good cross regulation and dynamic load response, type III compensation is adopted. R23 and R36 form a voltage divider network that senses the output voltage. Output voltage regulation is controlled through the shunt regulator TL431 (IC3) and the optocoupler (OPTO1) provides electrical isolation between the primary and secondary sides. Resistor R27 provides the bias current required by IC3 and is placed in parallel to OPTO1 to ensure that the bias current to TL431 does not become a part of the feedback current. Resistor R22 sets the overall DC loop gain and limits the current through OPTO1 during transient conditions. R29, C29, R32, C20 and C21 set the frequency response for the feedback circuit.

Output overvoltage is protected by ZD2, D10 and Q7. Once Vout is over 25 V, ZD2 conducts to turn on Q7 and the TL431 output is pulled down. Consequently, the primary HBFB pin will be pulled down below 0.3 V and the LLC enters burst off stage. Afterwards, the output voltage will drop below 25 V and HBFB recovers to a level above 1.75 V where the LLC will resume switching again.

5.5 AC detection

The IDP2303A's AC detection algorithm monitors the AC waveform with a signal conditioning circuit formed by C33, R7, Q8, R41, R42, R43, R44, ZD4 and ZD5 to perform AC detection for Xcap discharge via the UART pin.

An AC detection algorithm checks if there is an alternating voltage at the converter input. As soon as the voltage stops alternating an AC unplug event is detected and the input capacitors (XCAPs) are discharged via the depletion cell of the IDP2303A between the HV pin and GND.

5.6 Vcc regulator

To limit the operating temperature of the IDP2303A, a Vcc regulator circuit formed by auxiliary winding of transformer TR1, D4, D5, Q6, R17, ZD1, C14 and C15 is incorporated into the design. This circuit limits the Vcc voltage to the IDP2303A to 14 V.

6 Circuit diagram

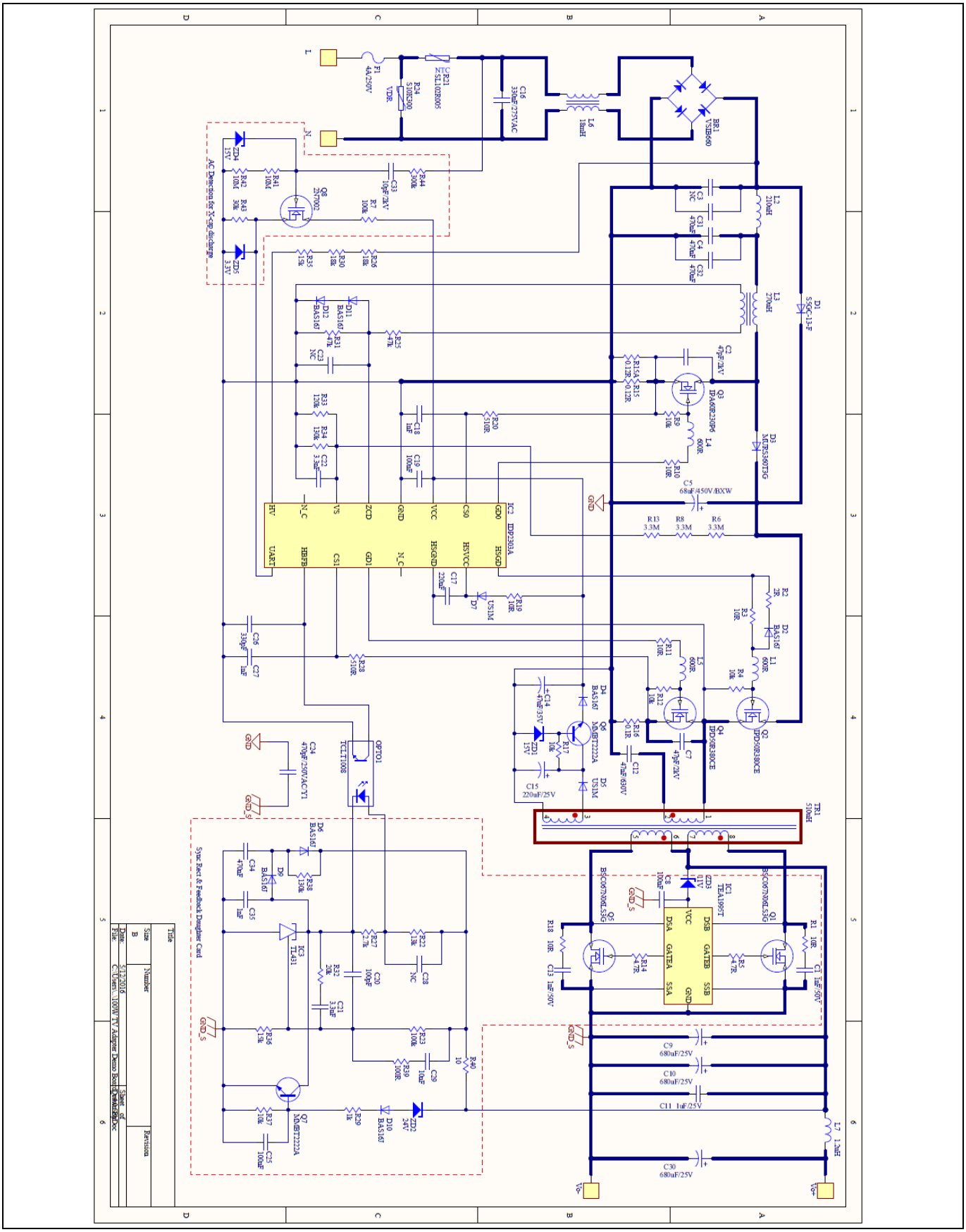


Figure 3 Schematics of 100 W PFC + LLC adapter

7 PCB layout

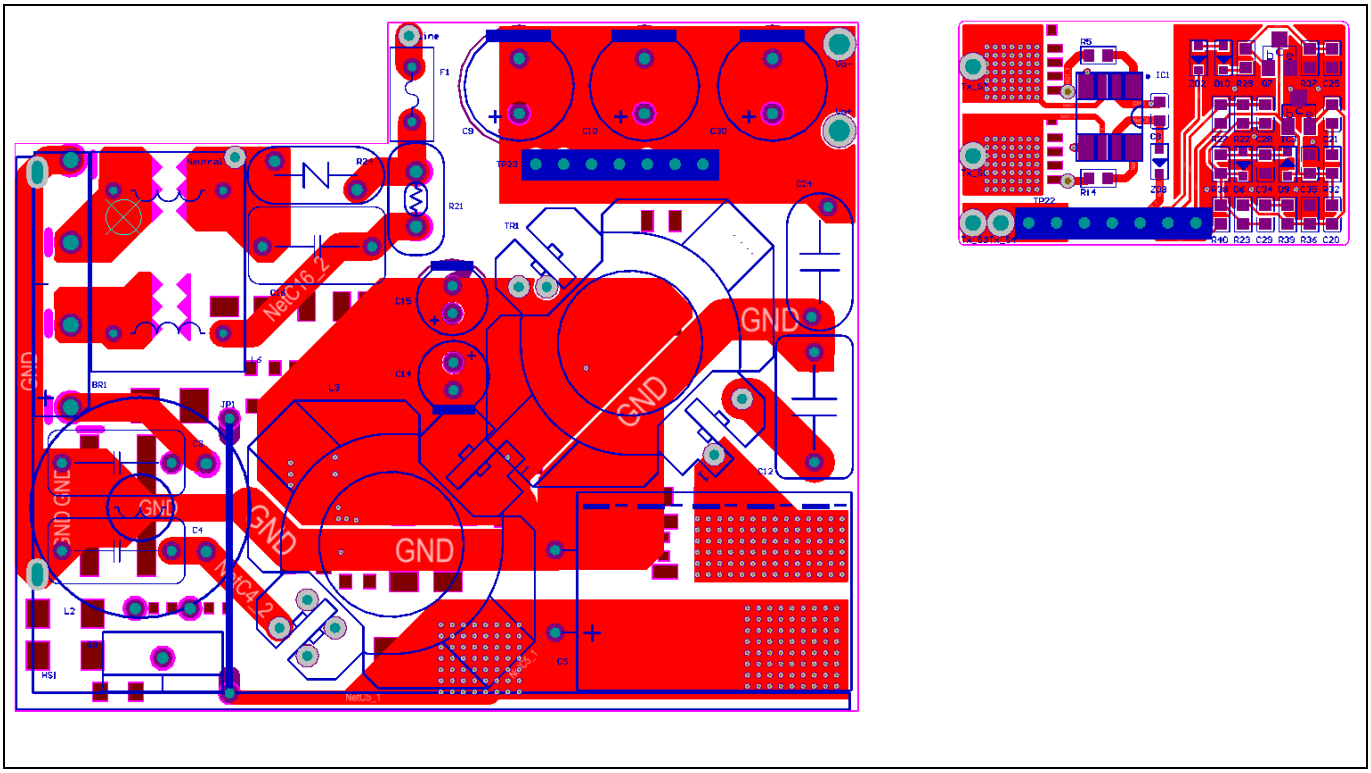


Figure 4 Top side component legend – view from component side

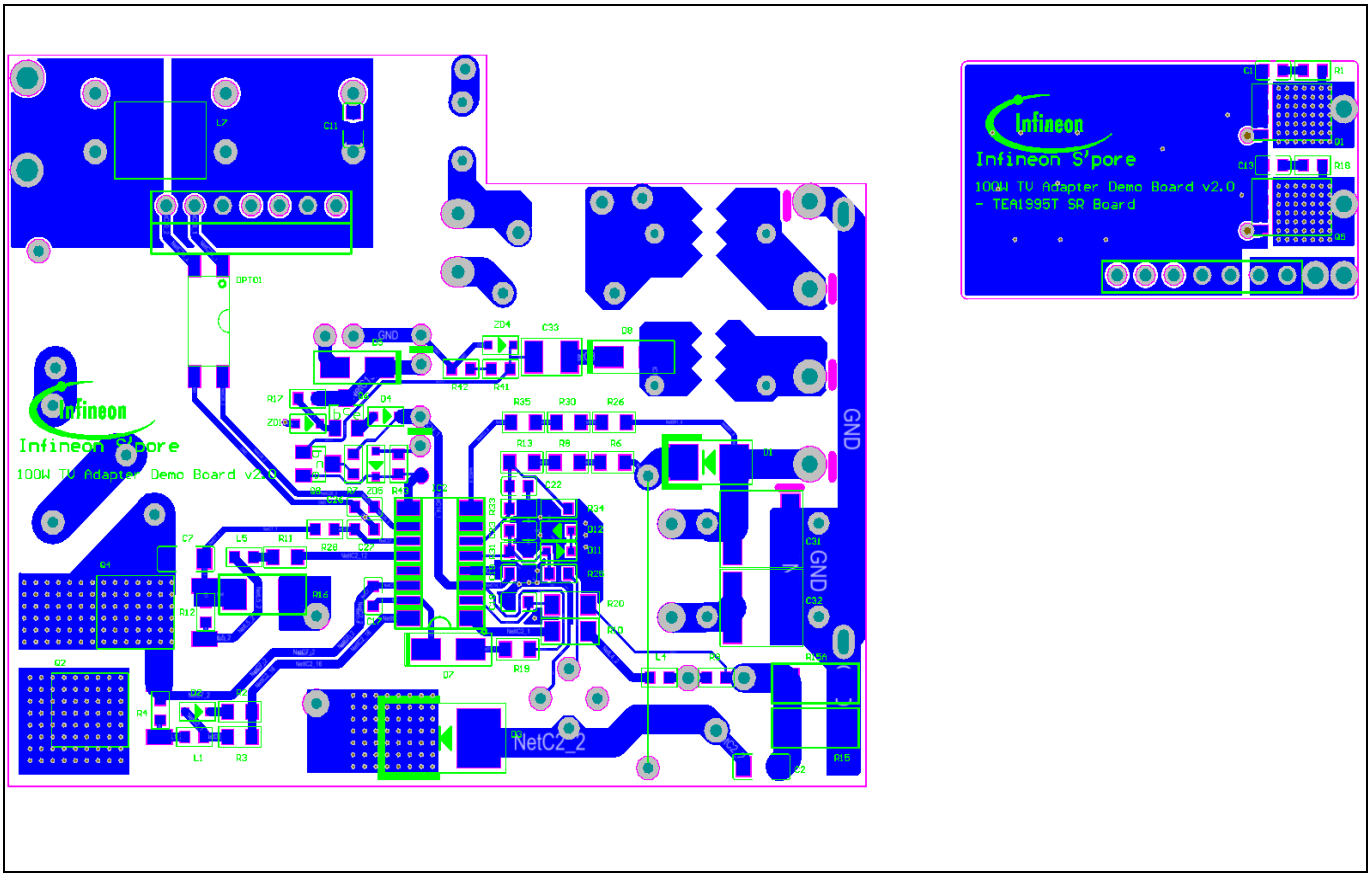


Figure 5 Bottom side component legend – view from solder side

8 Bill of material

Table 3 Bill of material

Item	Circuit code	Description / value	Quantity	Part Number	Manufacturer
1	BR1	600 V/6 A	1	VSIB660	Multicomp
2	C1	1 nF/50 V	1	GRM188R71H102KA01	Murata
3	C2	47 pF/2 kV	1	GRM31A7U3D470JW31	Murata
4	C3	NC	1		NC
5	C4	470nF/450 V	1	B32671P4474K000	EPCOS
6	C5	68 uF/450 V/BXW	1	450BXW68MEFC18X25	Rubycon
7	C7	47pF/2 kV	1	GRM31A7U3D470JW31	Murata
8	C8	100 nF	1	GRM188R71H104MA93	Murata
9	C9	680 uF/25 V	1	25ZL680MEFC10X20	Rubycon
10	C10	680 uF/25 V	1	25ZL680MEFC10X20	Rubycon
11	C11	1 uF/25 V	1	GRM219R71E105KA88	Murata
12	C12	47 nF/630 V	1	B32641B6473J	EPCOS
13	C13	1 nF/50 V	1	GRM188R71H102KA01	Murata
14	C14	47 uF/35 V	1	35YXF47MEFC6.3X11	Rubycon
15	C15	220 uF/25 V	1	25YXG220MEFC6.3X11	Rubycon
16	C16	330 nF/275 VAC	1		
17	C17	220 nF/50 V	1	GRM188R71H224KAC4	Murata
18	C18	1 nF/50 V	1	GRM188R71H102KA01	Murata
19	C19	100 nF/50 V	1	GRM188R71H104MA93	Murata
20	C20	100 pF/50 V	1	GRM033R71H101KA12	Murata

Bill of material

21	C21	3.3 nF/50 V	1	GRM188R71H332KA01	Murata
22	C22	3.3 nF/50 V	1	GRM188R71H332KA01	Murata
23	C23	NC	1		NC
24	C24	470 pF/250 VAC/Y1	1	DE2B3KY471KA3BM02	Murata
25	C25	100 nF/50 V	1	GRM188R71H104MA93	Murata
26	C26	330 pF/50 V	1	GRM1885C1H331JA01	Murata
27	C27	1 nF/50 V	1	GRM188R71H102KA01	Murata
28	C28	NC	1		NC
29	C29	10 nF/50 V	1	GRM188R71H103JA01	Murata
30	C30	680 uF/25 V	1	25ZL680MEFC10X20	Rubycon
31	C31	470 nF/500 V	1	GRM55DR72H474KW10L	Murata
32	C32	470 nF/500 V	1	GRM55DR72H474KW10L	Murata
33	C33	10 pF/2 kV	1	GRM31A7U3D100JW31	Murata
34	C34	470 nF/25 V	1	GRM188R71E474KA12	Murata
35	C35	1 nF/50 V	1	GRM188R71H102KA01	Murata
36	D1	400 V/5 A	1	S5GC-13-F	Multicomp
37	D2	100 V/250 mA	1	BAS16J	NXP
38	D3	600 V/3 A	1	MURS360T3G	ON-SEMI
39	D4	100 V/250 mA	1	BAS16J	NXP
40	D5	1 kV/1 A	1	US1M-13-F	DIODES INC.
41	D6	100 V/250 mA	1	BAS16J	NXP
42	D7	1 kV/1 A	1	US1M-13-F	DIODES INC.
43	D9	100 V/250 mA	1	BAS16J	NXP

Bill of material

44	D10	100 V/250 mA	1	BAS16J	NXP
45	D11	100 V/250 mA	1	BAS16J	NXP
46	D12	100 V/250 mA	1	BAS16J	NXP
47	F1	4 A/250 V	1	MST 4A 250V	Multicomp
48	IC1	TEA1995T	1	TEA1995T	NXP
49	IC2	IDP2303A	1	IDP2303A	INFINEON
50	IC3	TL431	1	TL431AIDBZR	TI
51	L1	600 R	1	BLM18KG601SN1	Murata
52	L2	210 uH	1		
53	L3	270 uH	1	NP10676	ICT
54	L4	600 R	1	BLM18KG601SN1	Murata
55	L5	600 R	1	BLM18KG601SN1	Murata
56	L6	18 mH	1		
57	L7	1 uH	1	FDSD0630-H-1R0M=P3	Murata
58	OPTO1	TCLT1008	1	TCLT1008	Vishay
59	Q1	60 V/50 A	1	BSC067N06LS3G	INFINEON
60	Q2	500 V/0.38 ohm	1	IPD50R380CE	INFINEON
61	Q3	600 V/0.23 ohm	1	IPA60R230P6	INFINEON
62	Q4	500 V/0.38 ohm	1	IPD50R380CE	INFINEON
63	Q5	60 V/50 A	1	BSC067N06LS3G	INFINEON
64	Q6	MMBT2222A	1	MMBT2222A	INFINEON
65	Q7	MMBT2222A	1	MMBT2222A	INFINEON
66	Q8	60 V/0.3 A	1	2N7002	INFINEON

Bill of material

67	R1	10 R	1		SMD
68	R2	2 R	1		SMD
69	R3	10 R	1		SMD
70	R4	10 k	1		SMD
71	R5	4.7 R	1		SMD
72	R6	3.3 M	1		SMD
73	R7	100 k	1		SMD
74	R8	3.3 M	1		SMD
75	R9	10 k	1		SMD
76	R10	10 R	1		SMD
77	R11	10 R	1		SMD
78	R12	10 k	1		SMD
79	R13	3.3 M	1		SMD
80	R14	4.7 R	1		SMD
81	R15	0.12 R	1	WSL2010R1200FEA	Vishay
82	R15A	0.12 R	1	WSL2010R1200FEA	Vishay
83	R16	0.1 R	1	WSLT2010R1000FEA18	Vishay
84	R17	10 k	1		SMD
85	R18	10 R	1		SMD
86	R19	10 R	1		SMD
87	R20	510 R	1		SMD
88	R21	5 A/2 Ω	1	SL10 2R005	AMETHERM
89	R22	13 k	1		SMD

Bill of material

90	R23	100 k	1		SMD
91	R24	S10K300	1	B72210S0301K101	EPCOS
92	R25	47 k	1		SMD
93	R26	18 k	1		SMD
94	R27	2.7 k	1		SMD
95	R28	510 R	1		SMD
96	R29	1 k	1		SMD
97	R30	18 k	1		SMD
98	R31	47 k	1		SMD
99	R32	20 k	1		SMD
100	R33	120 k	1		SMD
101	R34	130 k	1		SMD
102	R35	15 k	1		SMD
103	R36	15 k	1		SMD
104	R37	10 k	1		SMD
105	R38	130 k	1		SMD
106	R39	100 R	1		SMD
107	R40	10 R	1		SMD
108	R41	10 M	1		SMD
109	R42	10M	1		SMD
110	R43	30 k	1		SMD
111	R44	300 k	1		SMD
112	TR1	510 uH	1	NP10677	ICT

Bill of material

113	ZD1	15 V/500 mW	1	TDZ15J	NXP
114	ZD2	24 V/500 mW	1	TDZ24J	NXP
115	ZD3	11 V/500 mW	1	TDZ11J	NXP
116	ZD4	15 V/500 mW	1	TDZ15J	NXP
117	ZD5	3.3 V/500 mW	1	TDZ3V3J	NXP
118	HS1	Heatsink	1		

9 Magnetics construction

9.1 PFC choke, L3

ELECTRICAL SPECIFICATION @25°C	
TURNS RATIO	: W1:W2=66Ts:7Ts
L(1-12)	: 270 µH±10% @10 kHz, 50 mV
HI-POT	: 500 Vrms(W1 to W2) @ 50 Hz, for 2 Sec.
	: 500 Vrms(Wdgs to core) @ 50 Hz, for 2 Sec.

MATERIALS:	
BOBBIN	: RM10, Vertical, 4 Pins, PHENOLIC
CORE	: RM10, TPW33 or DMR95 or PG312 or equal
WIRE	: (W1)30xΦ0.10 mm, UEW, 155°C
	: (W2)2Φ0.36 mm, UEW, 155°C
TAPE	: 5.0 mm wide
TUBE	: Teflon tube
GLUE	: Araldite

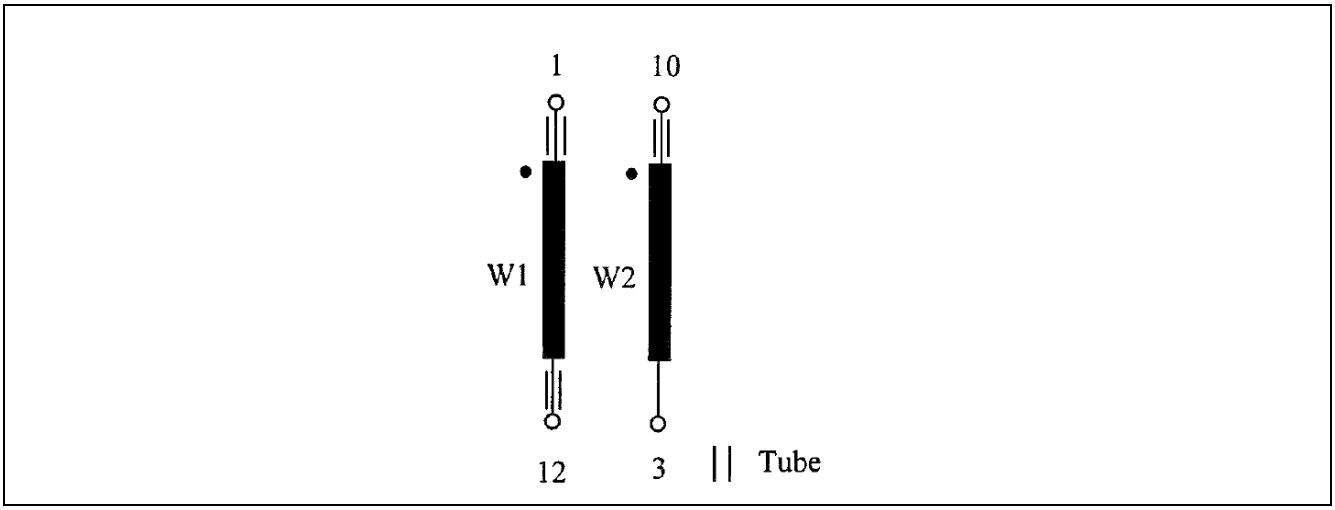


Figure 6 PFC choke electrical diagram

MECHANICAL (UNIT: mm)

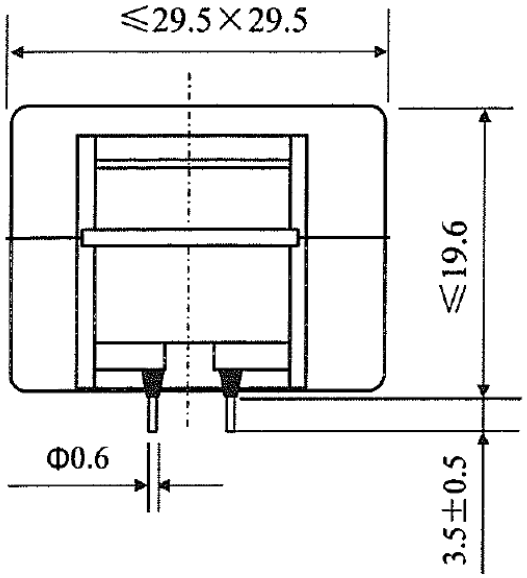


Figure 7 PFC choke – side view

MECHANICAL (UNIT: mm)

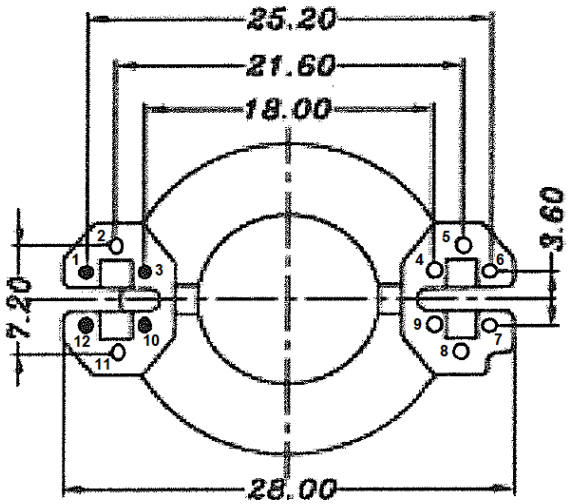


Figure 8 PFC choke – pin view

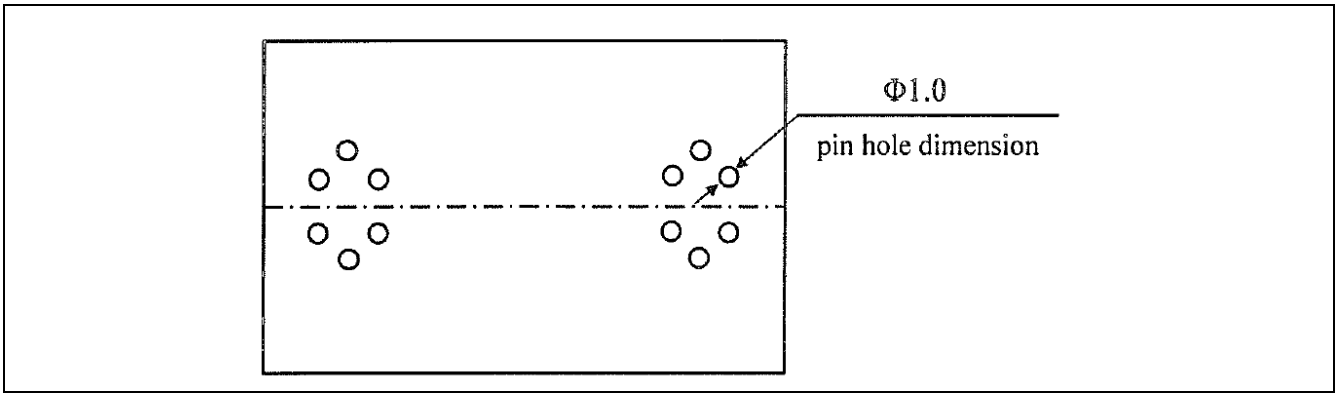


Figure 9 PFC choke pin hole gauge

9.2 LLC transformer, TR1

ELECTRICAL SPECIFICATION @25°C	
TURNS RATIO	: WI :W2:W3:W4=32Ts:3Ts:3Ts:3Ts
L(2-12)	Main indutance: 500 µH±10% @10 kHz, 50 mV Leakage indutance: 50 µH±10% @10 kHz, 50 mV
HI-POT	: 1000 Vrms(W1 to W2) @ 50 Hz, for 2 Sec.
	: 500 Vrms(Wdgs to core) @ 50 Hz, for 2 Sec.

MATERIALS:	
BOBBIN	: RM10, Vertical, 2 Sections, 4 Pins, PHENOLIC
CORE	: RM10, TPW33 or DMR95 or PG312 or equal
WIRE	: (W1)30xΦ0.10 mm, UEW, 155°C
	: (W2)Φ0.36 mm, UEW, 155°C
	: (W3,W4)108xAWG#40, Triple insulation wire
TAPE	: 5.0 mm wide
TUBE	: Teflon tube
GLUE	: Araldite

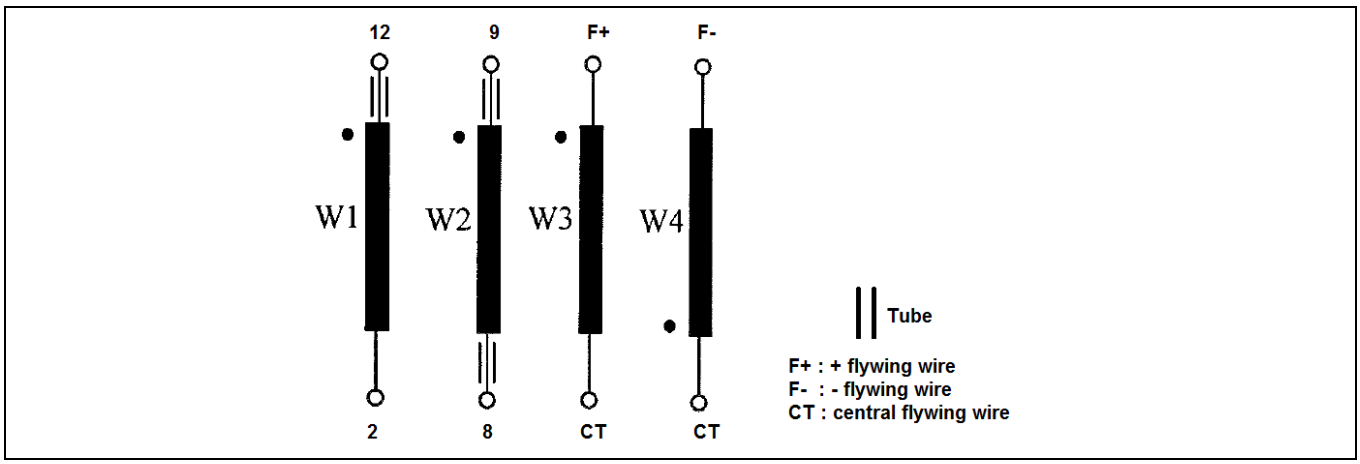


Figure 10 LLC resonant transformer electrical diagram

Magnetics construction

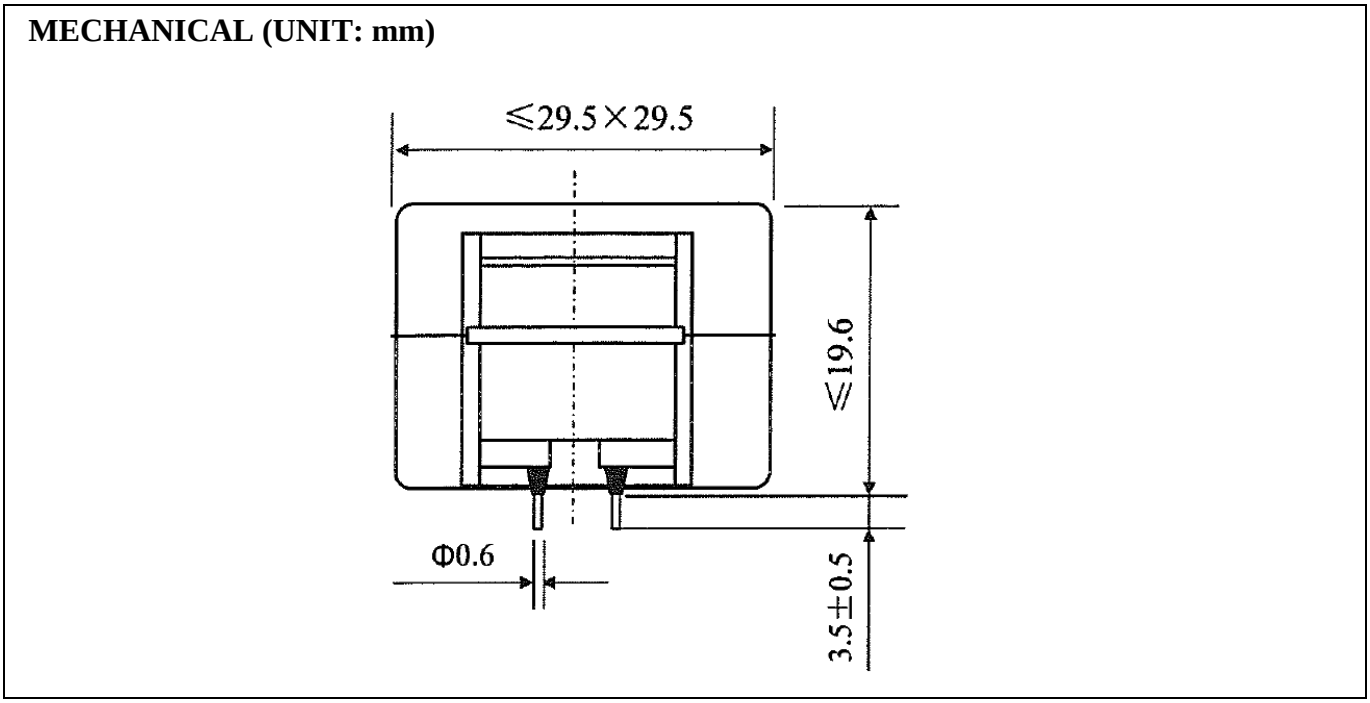


Figure 11 LLC resonant transformer complete – side view

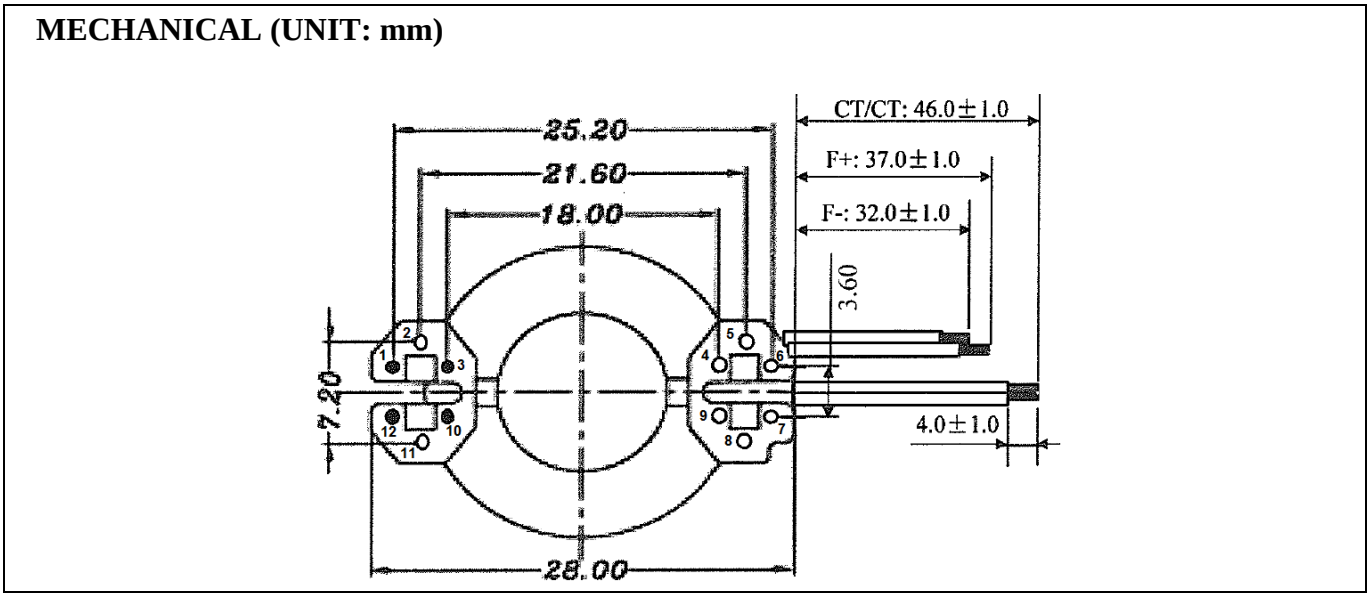


Figure 12 LLC resonant transformer complete – pin view

Magnetics construction

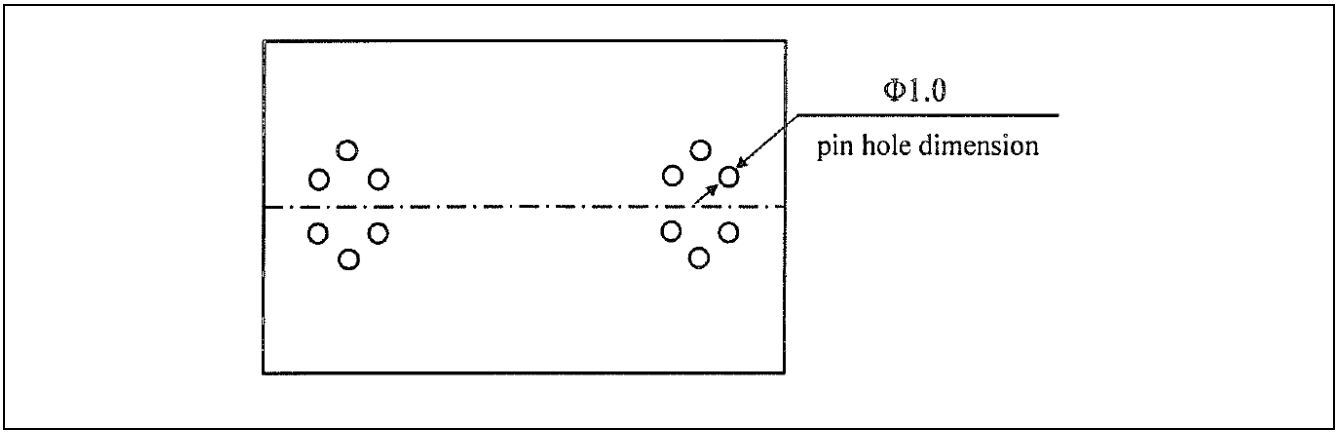


Figure 13 LLC resonant transformer pin hole gauge

10 Test results

10.1 Efficiency

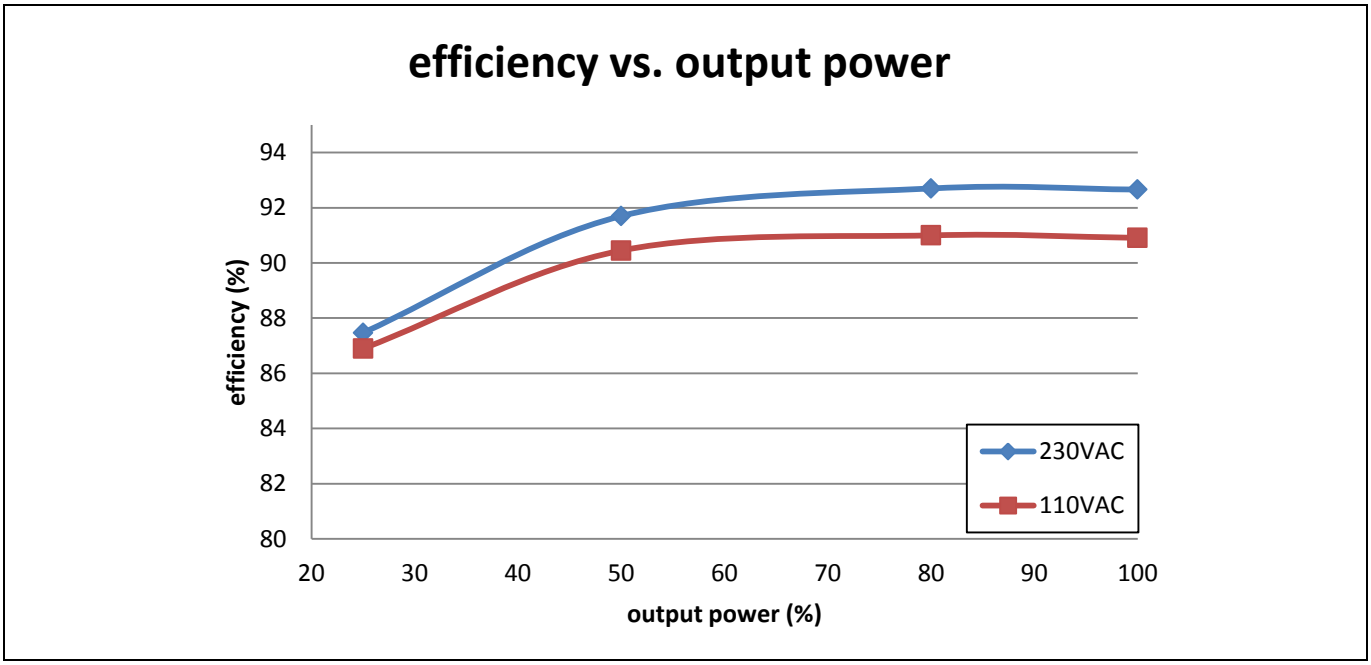


Figure 14 Efficiency measurments

The average effiency is higher than 88.3% for both high and low line over the load range from 25% to 100%. The full load efficiency at 230 V_{AC} reaches 92.6% with an average efficiency of 91.1%.

10.2 Standby power

The standby power consumption is less than 270 mW at 230 V_{AC} with 152 mW load.
Standby power consumption

Loading	Input Power (mW)	
	110 VAC	230 VAC
+19 V / 0 W	69.7	85.8
+19 V / 152 mW	251.4	264

10.3 Surge immunity (EN61000-4-5)

The surge immunity test was measured with a Noiseken LSS-15AX lightning surge simulator. The output common was connected to the primary side PE.

Pass 4 kV common mode test (line to earth and neutral to earth) and

Pass 2 kV differential mode test (line to neutral).

10.4 Conducted emissions (EN55022 class B)

The conducted EMI was measured by a Schaffner SMR25503 in accordance with EN55022 (CISPR 22) class B. The demoboard was set up at maximum load (100 W) with an input voltage of 115 V_{AC} and 230 V_{AC}. The system passes CISPR22 Class B with over 6dB margin.

Note: The system has a metal chasis during the measurement.

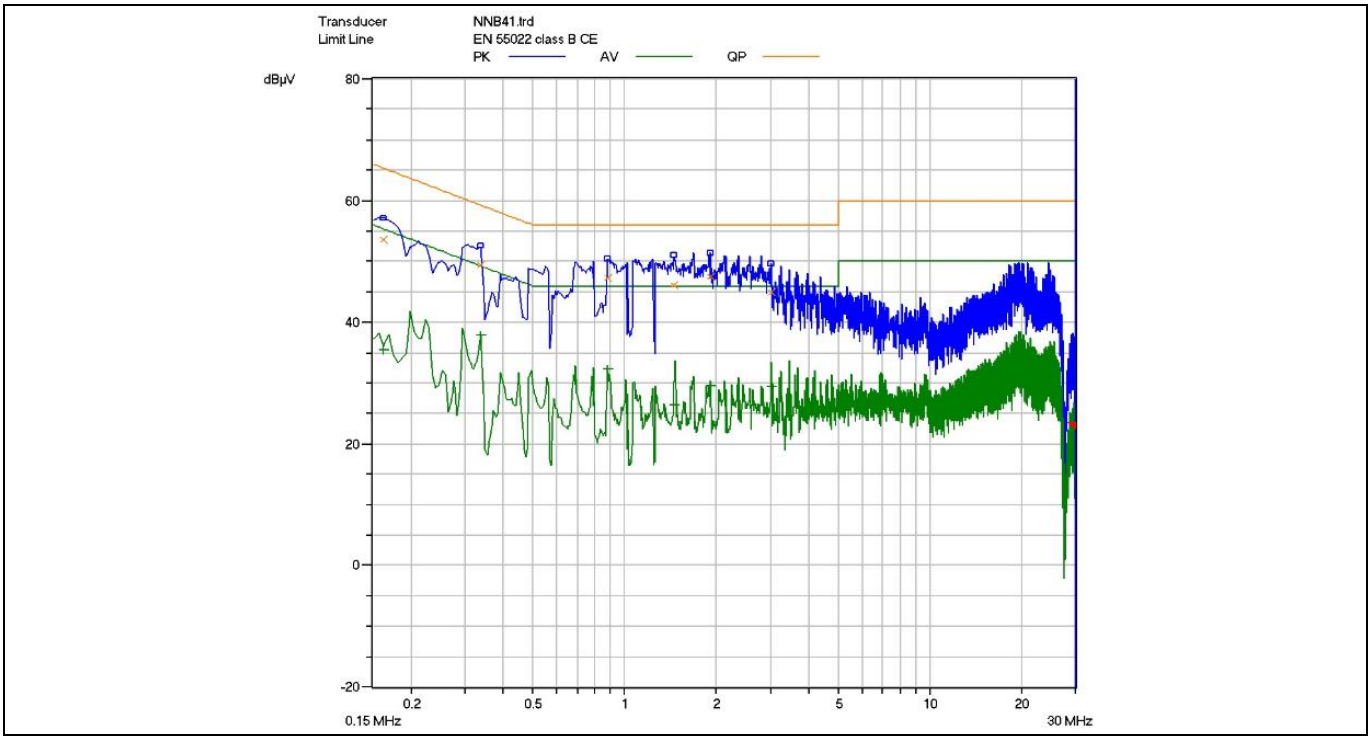


Figure 15 Conducted emissions (line) at 115 V_{AC} and maximum load

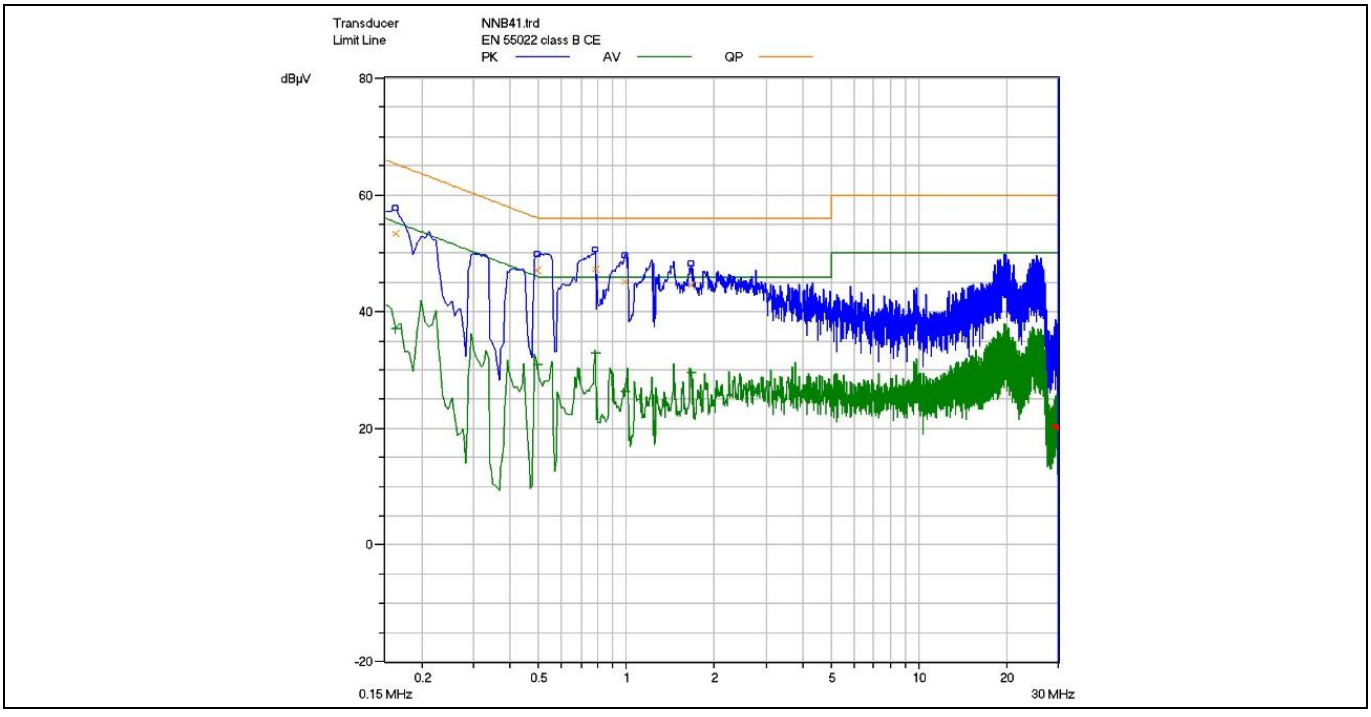


Figure 16 Conducted emissions (neutral) at 115 V_{AC} and maximum load

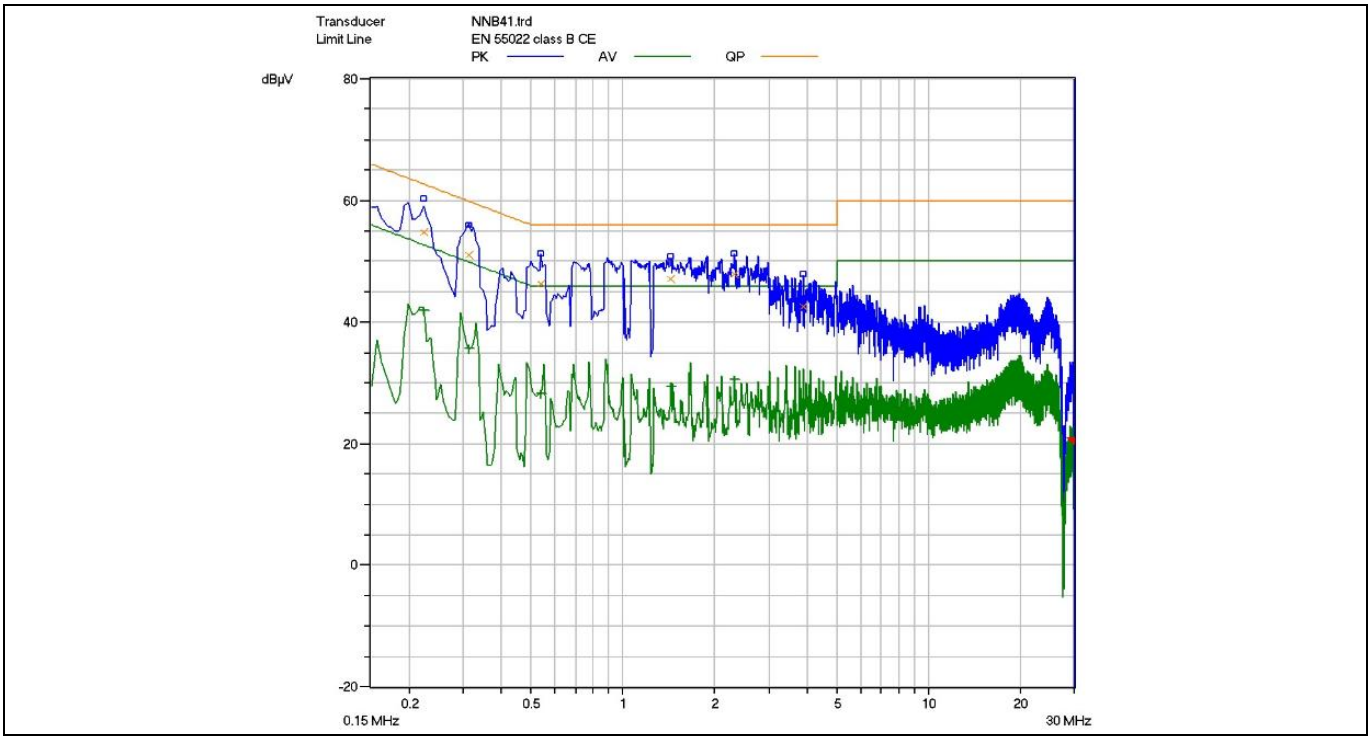


Figure 17 Conducted emissions (line) at 230 V_{AC} and maximum load

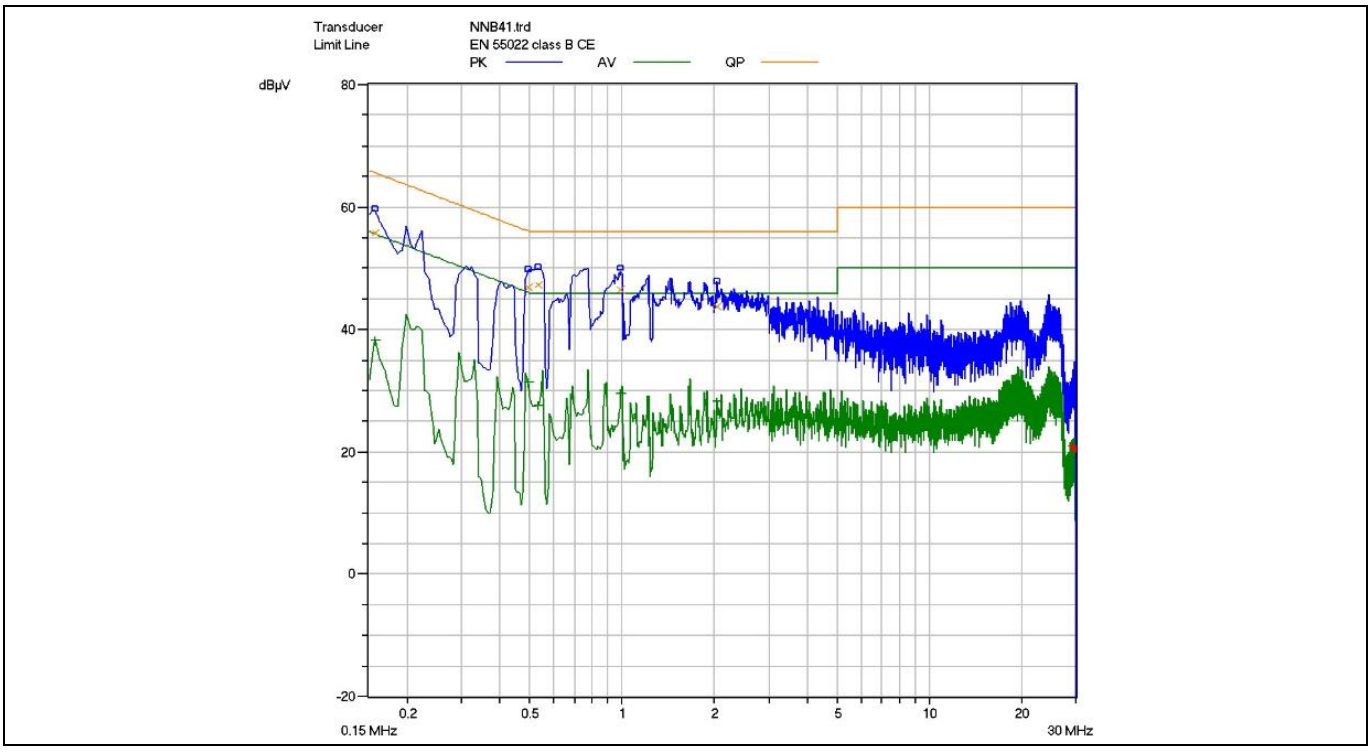


Figure 18 Conducted emissions (neutral) at 230 V_{AC} and maximum load

10.5 Loop stability measurement

The LLC loop gain/phase was measured by using Omnicron Bode 100. The measurement was done both at 115 Vac and 230 Vac input and 100 W output. As shown in Figure 19, LLC loop crossover frequency is 1.86 kHz and DC gain is 32 dB at 10 Hz. Phase margin is 60.1 degree at 1.86 kHz and gain margin is -10 dB at 3.95 kHz.

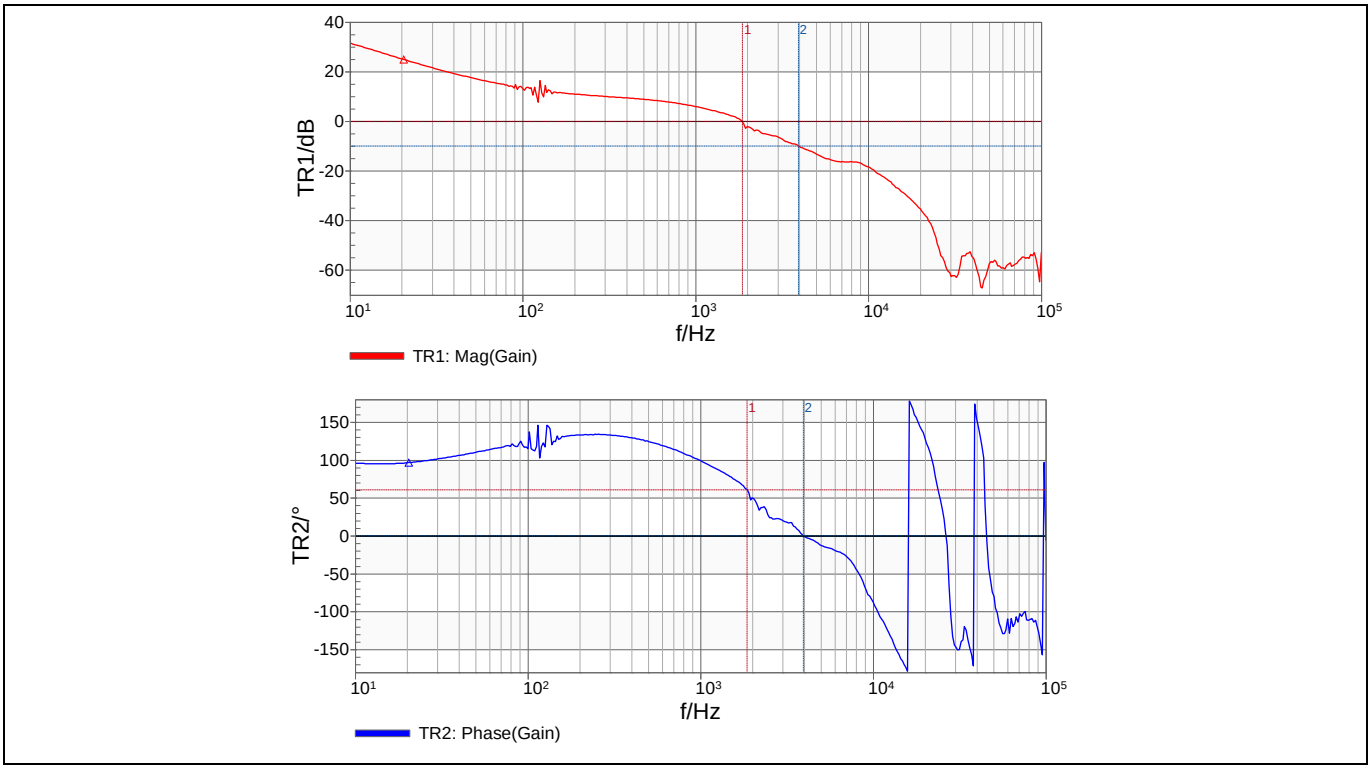


Figure 19 LLC loop gain and phase at 115 Vac and 100 W

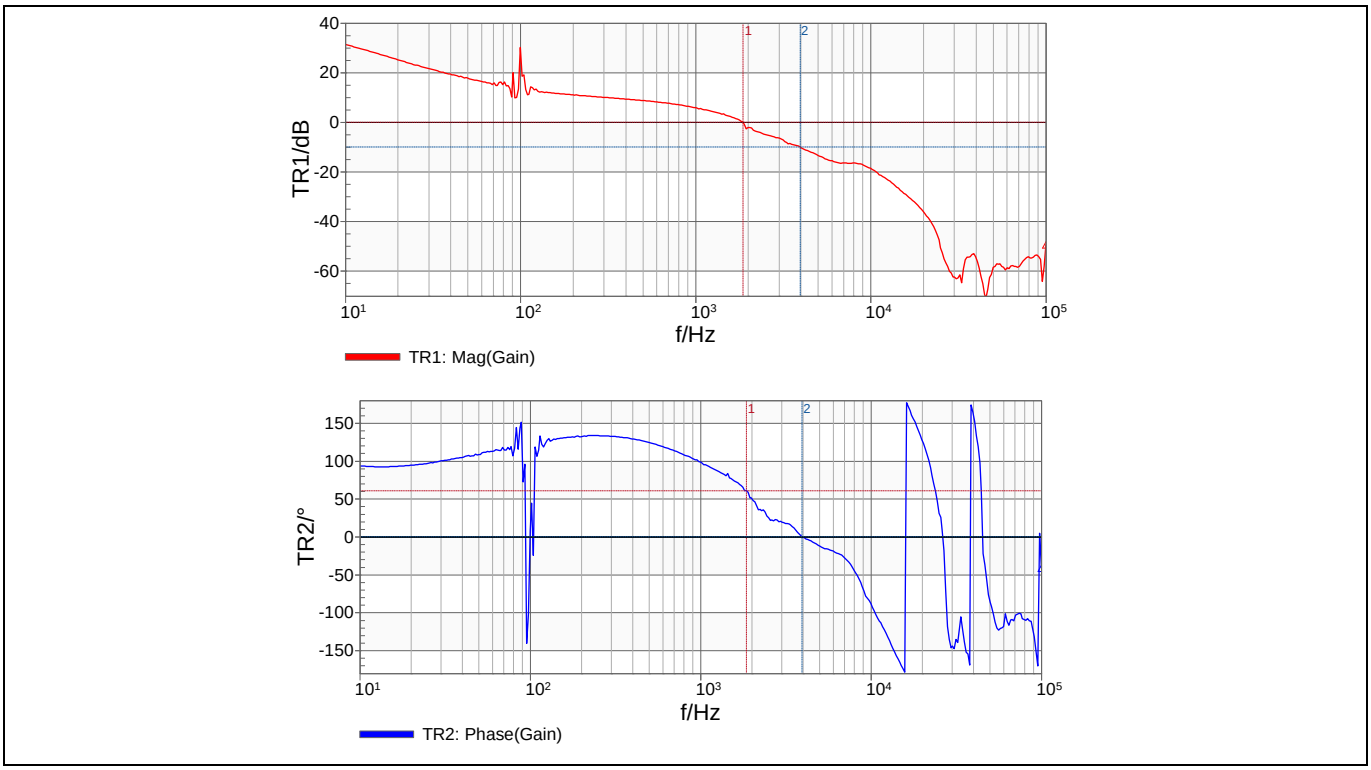


Figure 20 LLC loop gain and phase at 230 Vac and 100 W

10.6 Thermal measurement

The thermal test of the open frame demoboard was performed using an infrared thermography camera (TVS-500EX) at an ambient temperature of 25°C. The measurements were taken after two hours running at full load.

Test results

Table 4 Hottest temperature of demo board

No.	Major component	110 V_{AC} (°C)	230 V_{AC} (°C)
1	LLC transformer (point 1 main PCB top side)	76.7	75.6
2	PFC inductor (point 2 main PCB top side)	72.3	60.2
3	PFC MOSFET (point 3 main PCB top side)	66.5	58.4
4	Input bridge diode (point 5 main PCB top side)	74.0	56.4
5	SR driver IC (point 1 daugther board top side)	60.0	68.0
6	SR MOSFET (point 1 daughter board bottom side)	74.0	73.3
7	SR MOSFET (point 2 daughter board bottom side)	69.9	68.9
8	IDP2303A (point 1 PCB bottom side)	75.5	66.2
9	LLC high-side MOSFET (point 3 main PCB bottom side)	54.0	50.5
10	LLC low-side MOSFET (point 2 main PCB bottom side)	54.7	50.8
11	PFC rectifier diode (point 4 main PCB bottom side)	65.2	55.0
12	PFC shunt resistor (point 6 main PCB bottom side)	65.8	46.0
13	Ambient	25	25

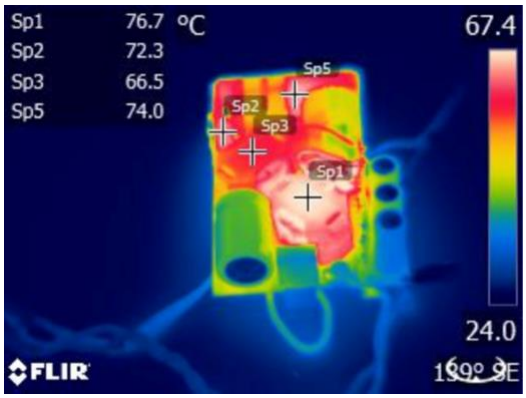
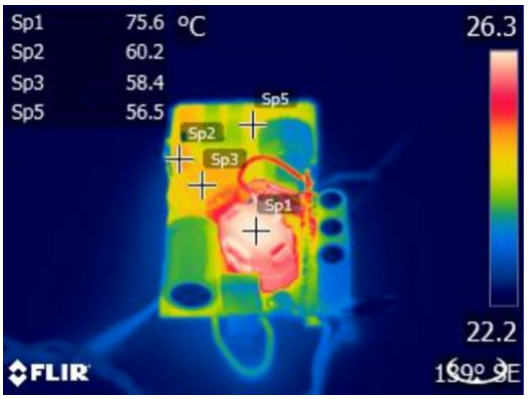
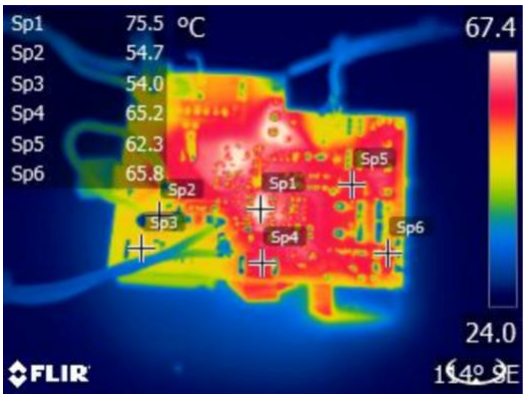
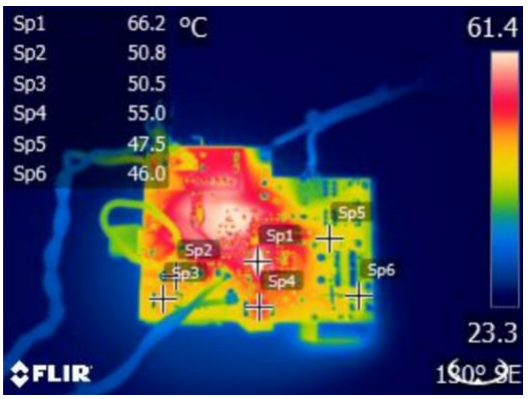
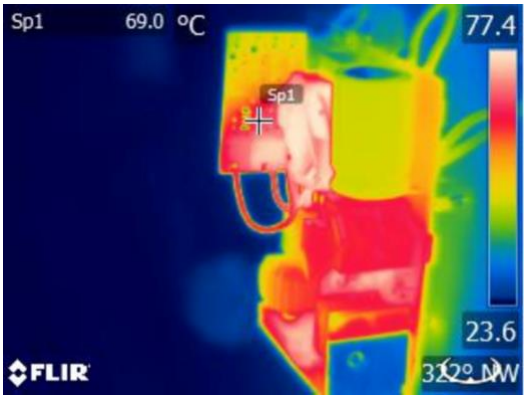
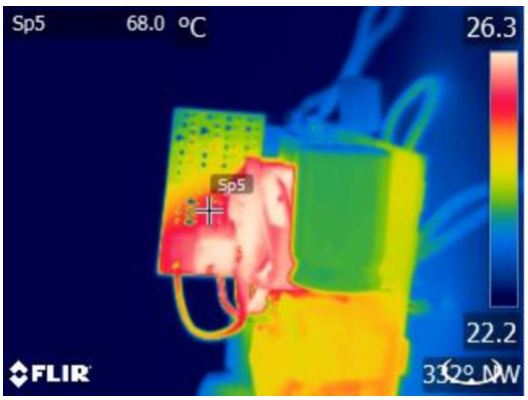
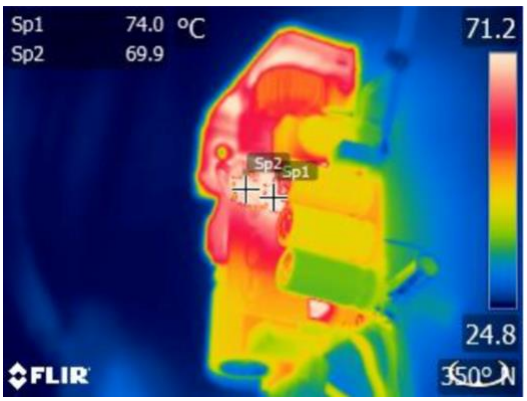
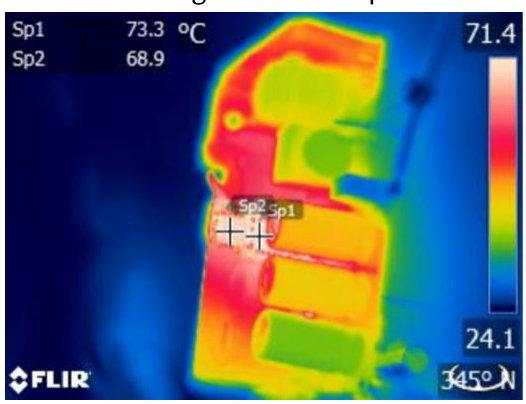
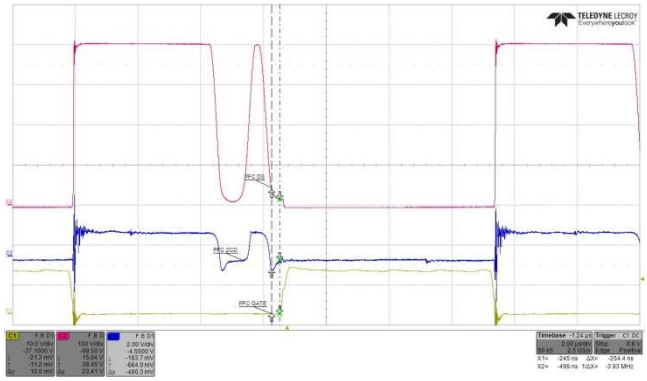
110 V_{AC} full load and 25°C ambient	230 V_{AC} full load and 25°C ambient
 PCB main board top side	 PCB main board top side
 PCB main board bottom side	 PCB bottom side
 PCB daugther board top side	 PCB daugther board top side
 PCB daugther board bottom side	 PCB daugther board bottom side

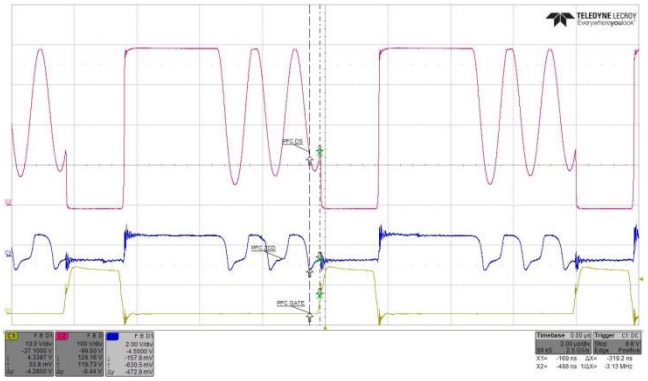
Figure 21 Infrared thermal image of DEMO-IDP2303A-120 W

10.7 PFC with valley switching

The IDP2303A features a multi-mode PFC, which has a default frequency range from 60 kHz to 120 kHz. The PFC MOSFET is determined to turn on by the PFC ZCD signal, when the PFC ZCD signal falls below 40 mV and after a certain blanking time, the PFC MOSFET turns on to charge up the PFC choke again. Due to this simple mechanism, PFC MOSFET valley switching is achieved, as shown in Figure 22, hence the PFC turns on loss can be significantly reduced. Moreover, with multi-mode operation, the PFC switching frequency is limited to the design range, which breaks down the switching loss under high line and light load.



PFC valley switching @ 110 V_{AC} and full load

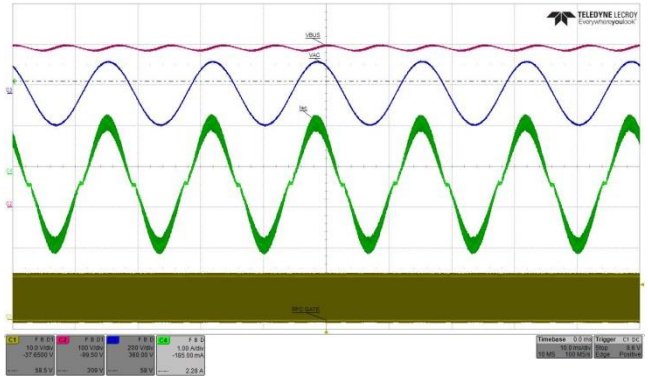


PFC valley switching @ 230 V_{AC} and full load

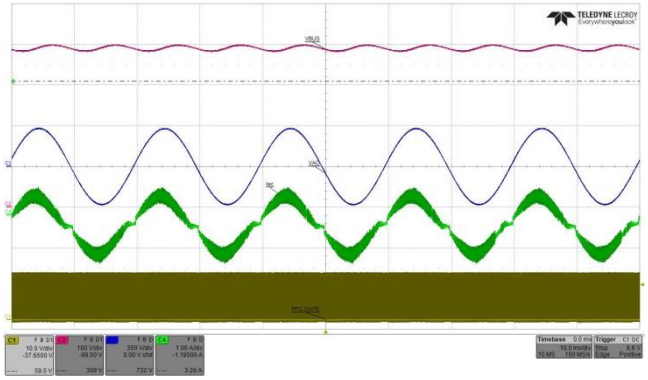
Figure 22 Multi-mode PFC with valley switching

10.8 Multi-mode PFC with unity power factor

As described in the IDP2303A datasheet, constant on time control is applied to achieve unity power factor. In Figure 23, the AC input current is sinusoidal and synchronous with the AC input voltage. Hence, unity power factor has been achieved.



AC input current @ 110 V_{AC} and full load



AC input current @ 230 V_{AC} and full load

Figure 23 PFC AC input current

10.9 PFC dynamic response

As described in the IDP2303A datasheet, the PFC regulator is built-in to modulate the PFC MOSFET on time to regulate the PFC bus voltage under control. In Figure 24, even in the case of an extremely dynamic load change between minimum and full load, the PFC bus voltage only varies within the acceptable range. Accordingly the following LLC stage will vary its switching frequency to maintain the LLC output under regulation.

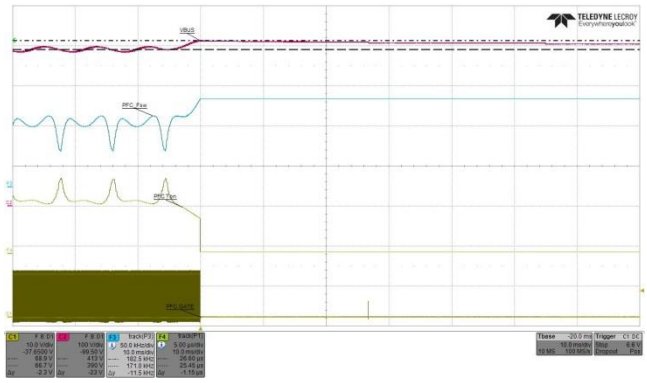
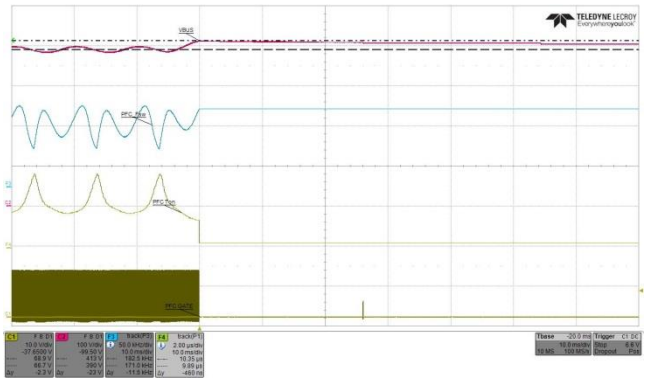
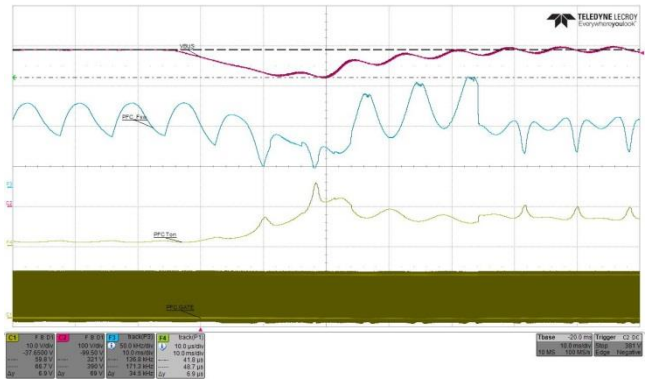
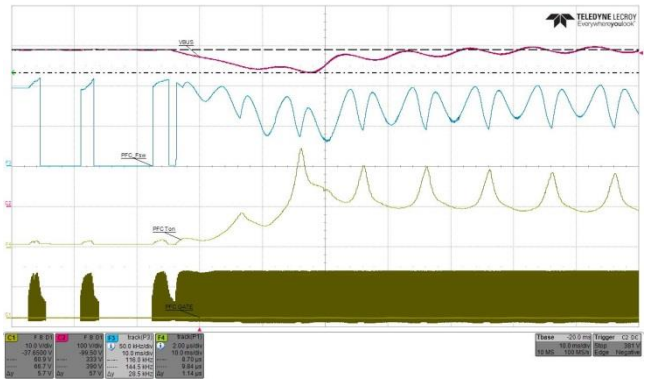
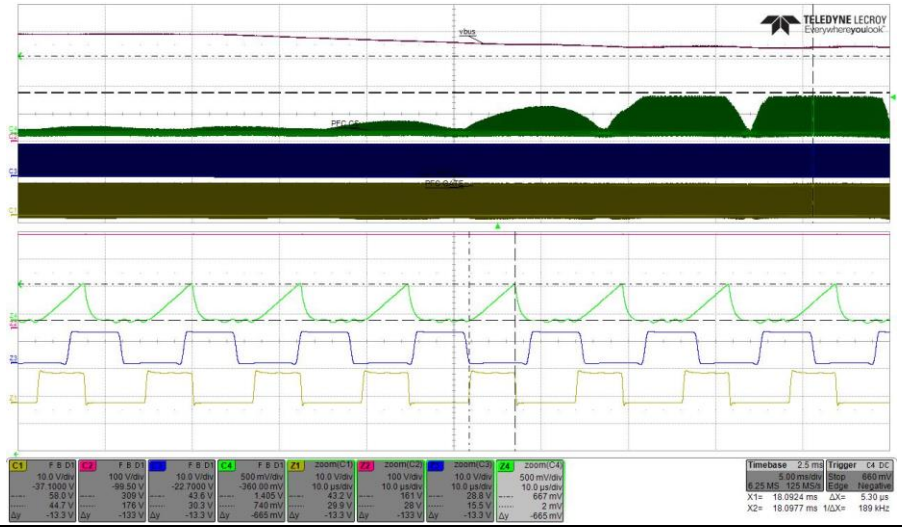
	
PFC bus ripple @ full load to min load and 110 V_{AC}	PFC bus ripple @ full load to min load and 230 V_{AC}
	
PFC bus ripple @ min load to full load and 110 V_{AC}	PFC bus ripple @ min load to full load and 230 V_{AC}

Figure 24 PFC bus voltage ripple when load changes

10.10 PFC over current protection

In order to limit the current flowing through the PFC choke, PFC over current protection is built-in to the IDP2303A. In Figure 25, the voltage across RCS2 and RCS4 is used to sense the PFC current. When the CS0 voltage exceeds 0.6 V (typ.), and after a propagation delay, the PFC MOSFET will be turned off to stop the current increasing.

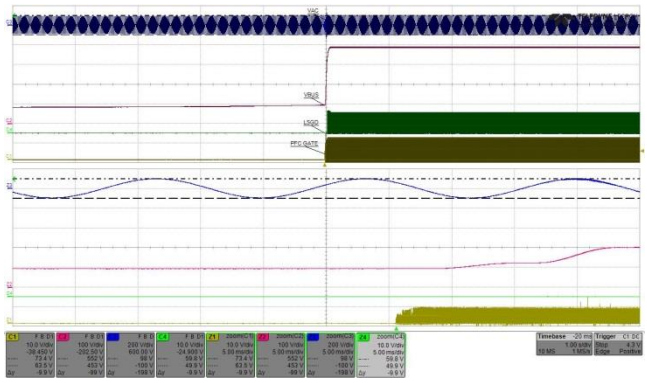


PFC over current protection

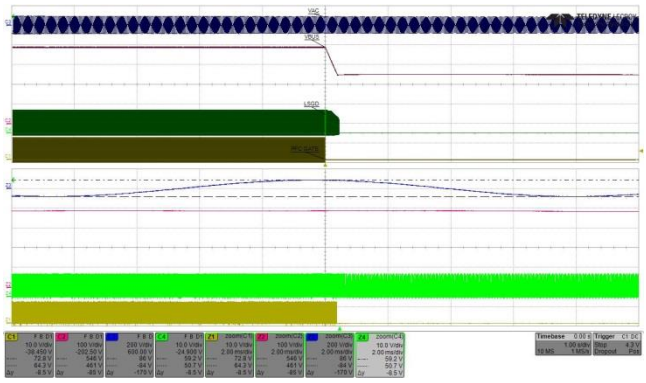
Figure 25 PFC over current protection @ 90 V_{AC} and full load

10.11 PFC brownin/brownout protection

To prevent the system working under extremely low AC input voltages, brown-in/brown-out protection is designed with configurable thresholds via the HV pin. It is implemented with a 51 kΩ HV resistor connected to the AC input, where the default thresholds are: brown-in 70 V_{AC} (RMS) and brown-out 60 V_{AC} (RMS). In Figure 26, with an AC slew rate of 1 V/s, the brown-in/brown-out protection is demonstrated. The measured brown-in threshold is 99 V peak (around 70 V_{AC} RMS), and the brown-out threshold is 85 V peak (around 60 V_{AC} RMS).



Brown-in @ 20% full load



Brown-in @ 20% full load

Figure 26 Brown-in/brown-out protection

10.12 PFC/LLC start up behavior

As described in the IDP2303A datasheet, both PFC and LLC soft-start features are implemented. In Figure 27 and Figure 28, the PFC bus voltage smoothly increases until reaching the target regulation value. To shorten the start-up time, the default svp (PFC PIT1 P coefficient) is set to 4 during the start-up phase. While under normal operation, svp is set to 6 to achieve more stable operation. Moreover, during the PFC start-up phase, its gate driver voltage is set to 7.5 V, when bus voltage reaches the LLC start-up threshold, the PFC gate driver voltage is reset to 10.5 V.

Test results

Accordingly, when the VS voltage reaches 2.05 V, the LLC starts switching with configurable soft-start behaviour. Its default maximum soft-start frequency is 270 kHz, and the LLC switching frequency smoothly sweeps from a high level to a low level and finally enters normal operation. For more details, please refer to the IDP2303A datasheet.

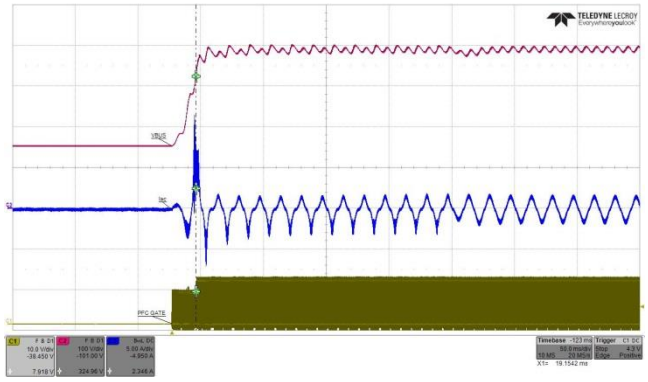
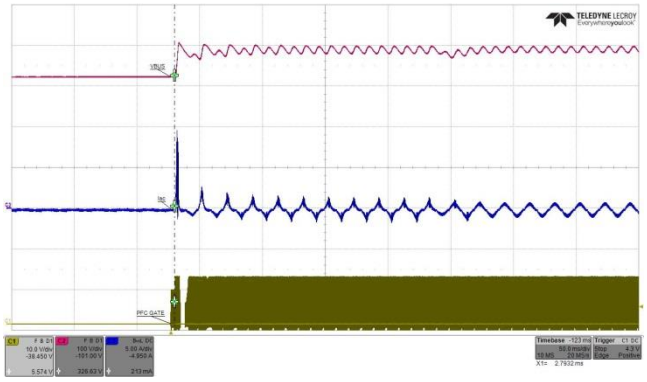
	
PFC start up @ 110 V_{AC} and full load	PFC start up @ 230 V_{AC} and full load

Figure 27 PFC startup behavior

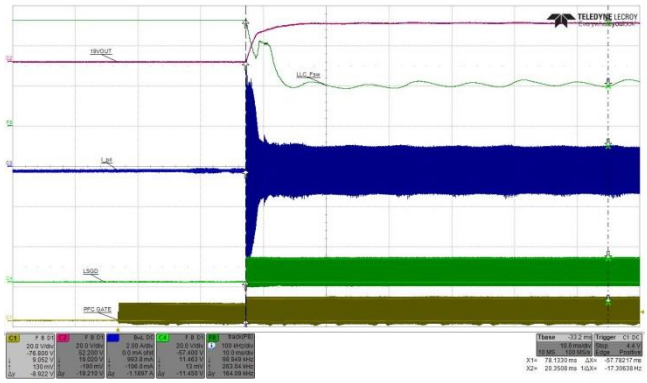
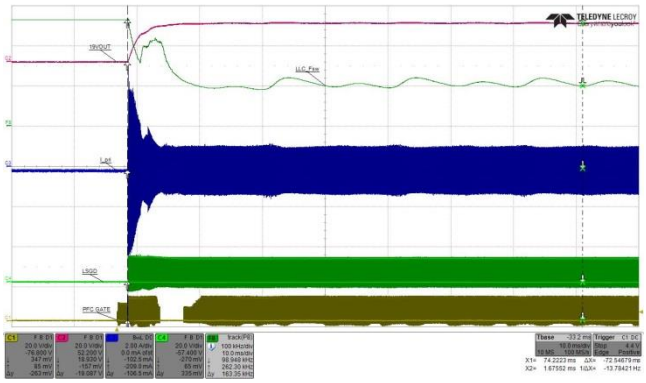
	
LLC start up @ 110 V_{AC} and full load	LLC start up @ 230 V_{AC} and full load

Figure 28 LLC start up behavior

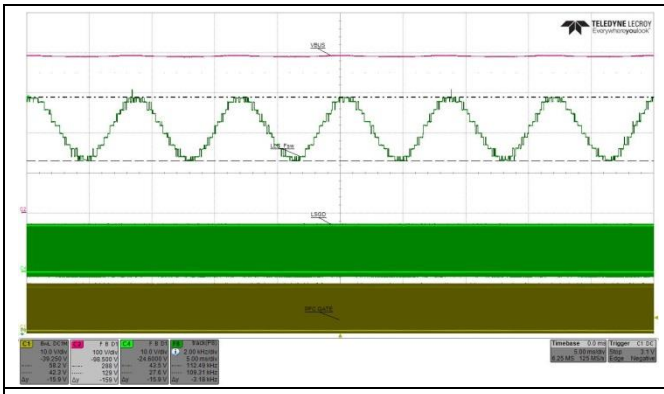
10.13 LLC line regulation

The LLC switching frequency will vary with reference to the PFC bus voltage ripple to regulate the LLC output. For example, at 110 V_{AC} and 20% of full load, the LLC switching frequency (f_{sw}) varies by 3.18 kHz from 112.5 kHz to 109.3 kHz to regulate its output. At 110 V_{AC} and 100% full load, the LLC f_{sw} varies by 11.3 kHz to regulate the output.

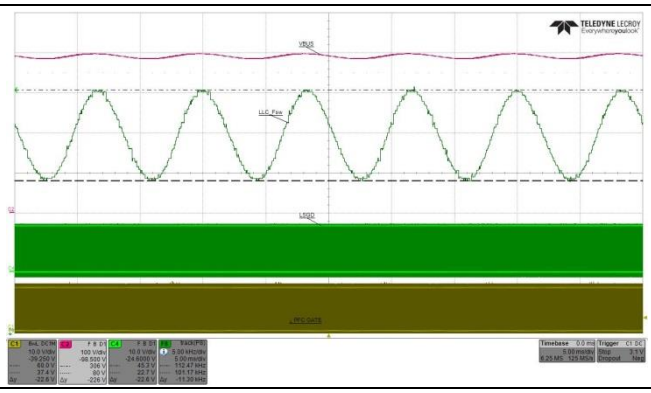
Figure 30 and Figure 31 show LLC output ripple noise which were measured by oscilloscope at 20 MHz bandwidth and 0.1 uF+10 uF was connected at measuring terminal. The maximum ripple/noise is 170 mV at 115

Test results

Vac, less than 190 mV (1% of Vout). At standby load 152 mW and 230 Vac, ripple/noise is 192 mV less than 2% of vout. At no load, ripple/noise is reduced to 67 mV due to adaptive burst frequency control.

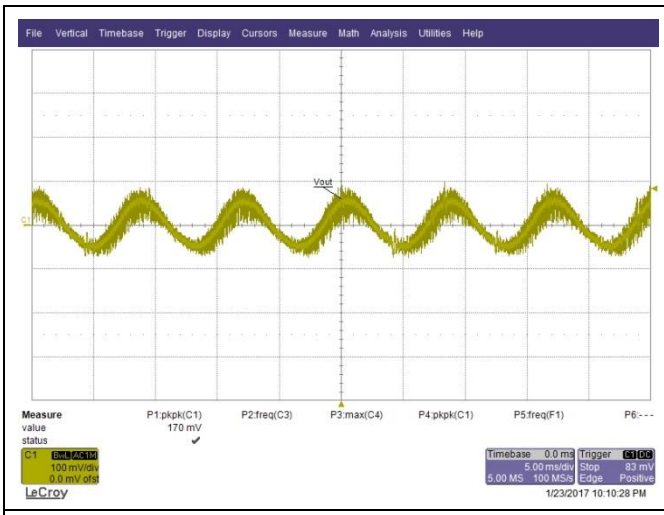


LLC f_{sw} @ 110 V_{AC} and 20% full load

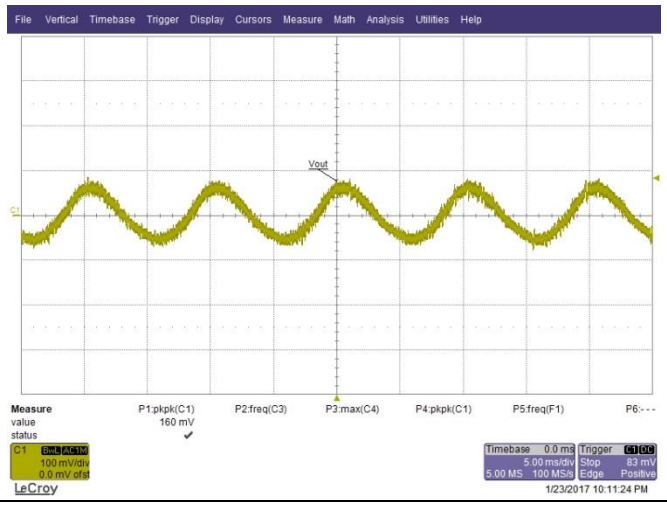


LLC f_{sw} @ 110 V_{AC} and 100% full load

Figure 29 LLC switching frequency varies against the PFC bus voltage

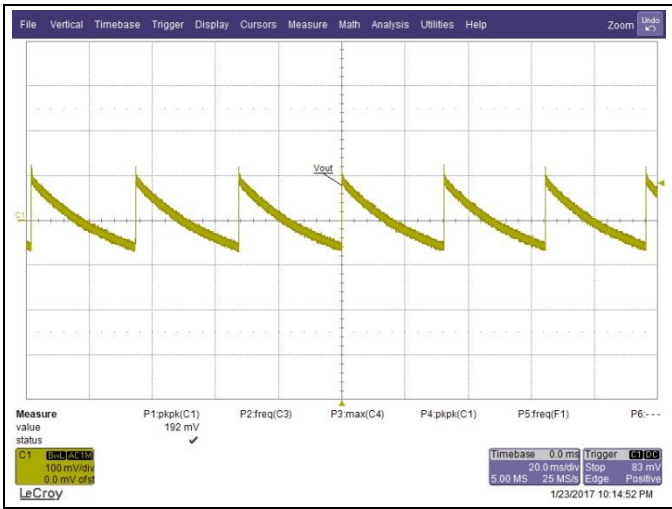


90 Vac

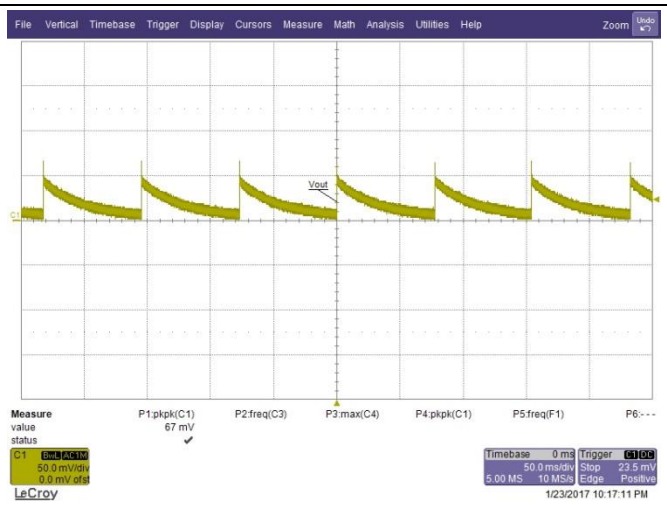


264 Vac

Figure 30 LLC output ripple noise at 100 W output



152 mW pout and 230 Vac input



0mW pout and 230 Vac input

Figure 31 LLC output ripple noise at burst mode

10.14 LLC load regulation

Figure 32 shows the dynamic behavior of the LLC stage during a load variation between 20% and 100% of full load. It can be seen that the LLC switching frequency varies against the load changes, and the measured output voltage undershoot/overshoot at 19 V is around 270 mV.

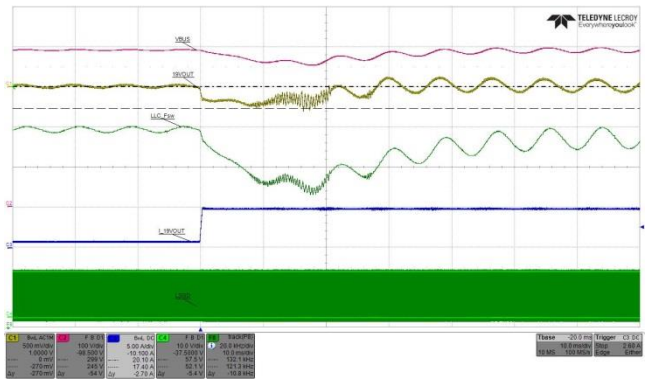
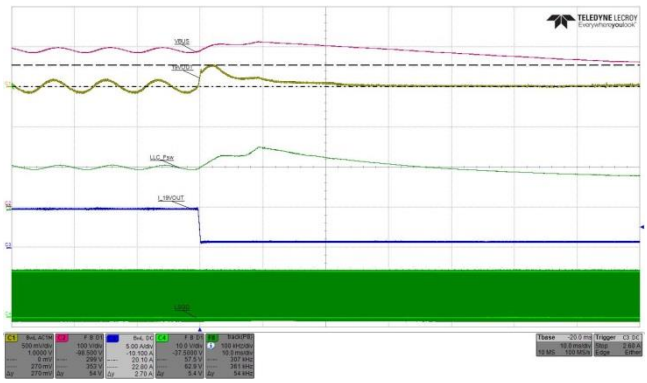
	
LLC fsw @ 110 V_{AC} and 20% ~ 100% full load	LLC fsw @ 110 V_{AC} and 20% ~ 100% full load

Figure 32 LLC switching frequency varies against the load changes

Figure 33 shows LLC output overshoot and undershoot when load has periodic step changes between 0W and 100 W. Output voltage peak-to-peak variation is 1.51 V, less than 1.9 V (+/-5% of Vout) regulation range.

	
Load step change between 0 W and 100 W at 115 Vac	Load step change between 0 W and 100 W at 230 Vac

Figure 33 LLC output overshoot and undershoot against the load periodic changes

10.15 LLC zero voltage switching

From the test results of Figure 34, it can be seen that the LLC zero voltage switching (ZVS) can be achieved over a very wide load range , which ensures high power conversion efficiency.

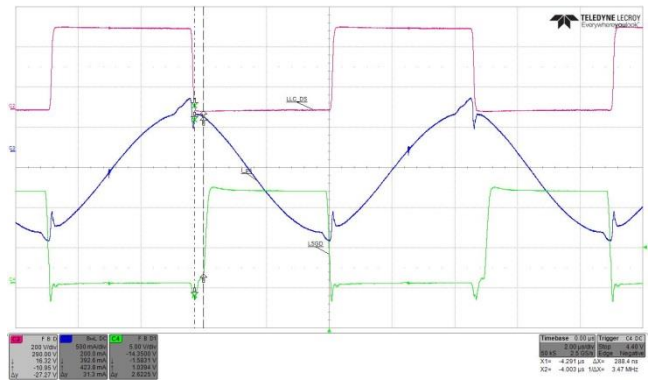
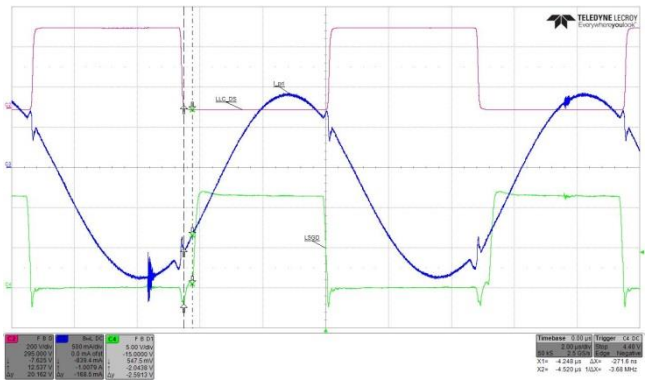
	
LLC ZVS @ 110 V_{AC} and 20% full load	LLC ZVS @ 110 V_{AC} and 100% full load

Figure 34 LLC zero voltage switching

10.16 PFC and LLC operation during holdup time

In order to meet the holdup time requirement, the LLC stage is required to cover a wide PFC bus voltage range. During the holdup time, the LLC switching frequency drops to regulate the output voltage against the bus voltage drop. As shown in Figure 35, after shutting down the AC input, the LLC keeps switching until the PFC bus voltage drops to the undervoltage protection threshold. The measured holdup time is around 13 ms, which meets most of the TV power supply specification.

When the undervoltage threshold is triggered, the PFC stops switching and the LLC continues switching at maximum frequency until Vcc reaches its UVLO threshold.

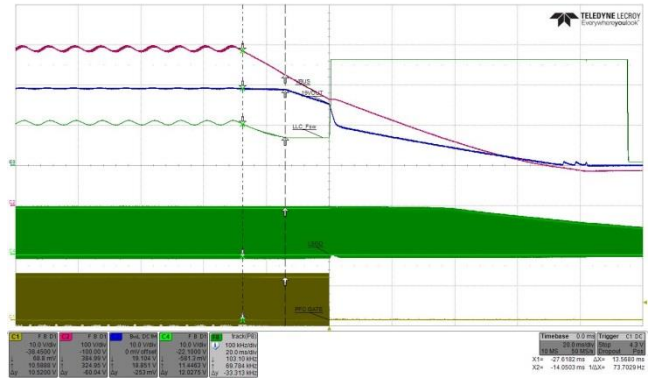
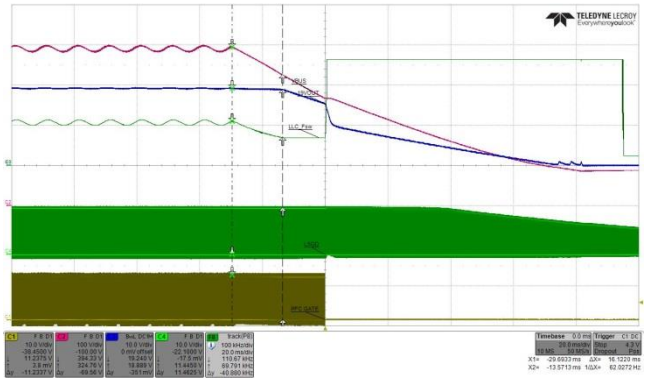
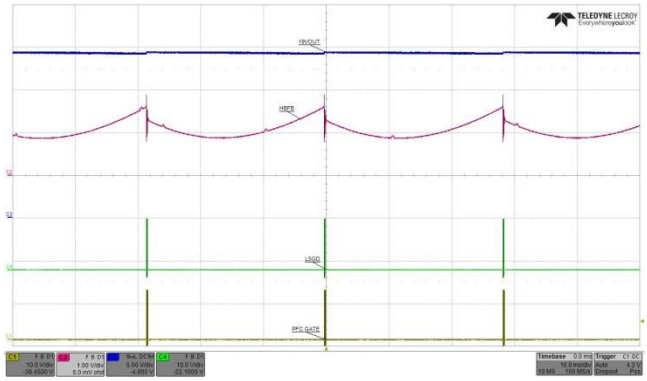
	
PFC/LLC operation @ 110 V_{AC} off, full load	PFC/LLC operation @ 230 V_{AC} off, full load

Figure 35 PFC and LLC operation after shutdown AC input with full load

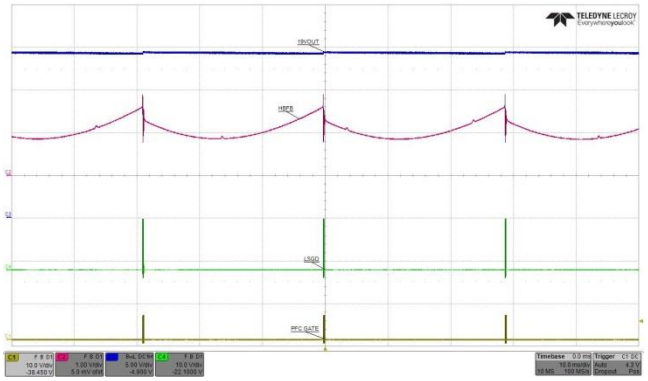
10.17 Burst mode operation

Burst mode operation is implemented in the IDP2303A to achieve low power consumption during standby operation. For this advanced burst mode control, the PFC and LLC are synchronized. However, during the burst on period if the bus voltage is higher than its target, then the PFC will not switch. To achieve ultra-low standby power consumption, the default target bus voltage during burst mode is around 360 V (the VS reference is set at 2.26 V).

In Figure 36, during the burst off period, V_{HBFB} will increase as vout starts to decrease due to the absence of an LLC switching signal. Once V_{HBFB} reaches the burst on threshold $V_{\_burst\_on}$, which is 1.65 V, the IC wakes up and resumes switching. The default LLC switching frequency under burst mode is set to 90 kHz, which is configurable and should be based on the LLC resonant tank design. For a detailed description of burst mode operation, please refer to the IDP2303A datasheet.



LLC burst mode operation @ 110 V_{AC}, standby load



LLC burst mode operation @ 230 V_{AC}, standby load

Figure 36 Burst mode operation at standby load

As shown in Figure 37, the LLC enters burst mode when the load jumps from full load to standby load and leaves burst mode when full load returns. There is 20 ms blanking time before the system enters burst mode as shown in the left side waveform. In the right side waveform, the system is leaving burst mode. It can be seen that another quick soft-start is implemented for the LLC when the system is leaving burst mode. Thus the LLC output undershoot is less than 5% of vout during the load jump from standby load to full load because the LLC burst frequency and on-time are optimized for standby load. Even during a load jump test from absolute no load to full load, the output undershoot will remain within 5% due to the adaptive burst frequency, as shown in Figure 37.

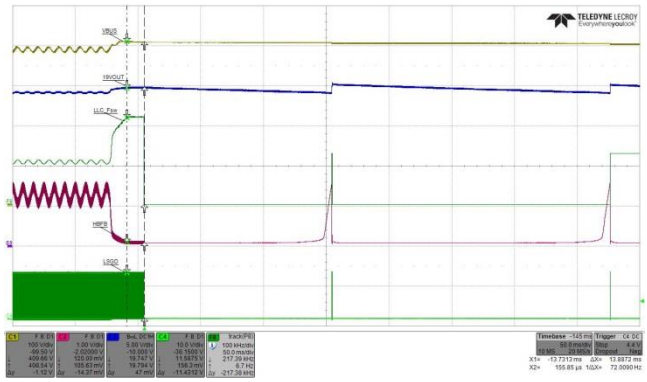
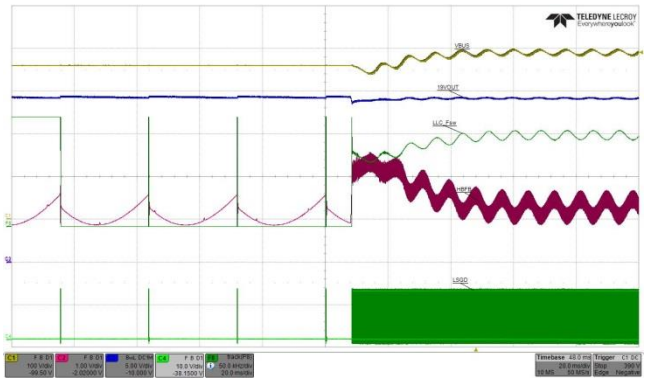
	
LLC jumps from full load to standby load @ 110 V_{AC}	LLC jumps from standby load to full load @ 110 V_{AC}

Figure 37 LLC entering/leaving burst mode operation at standby load

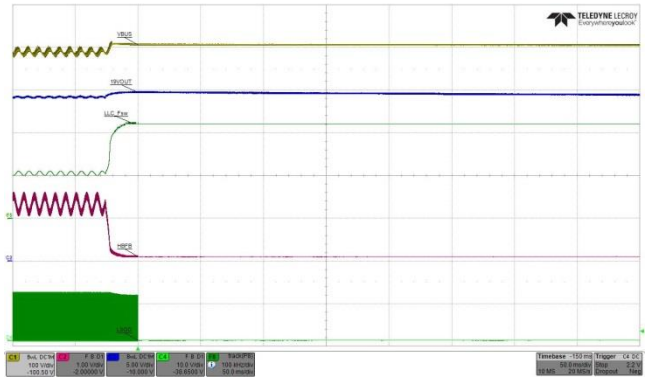
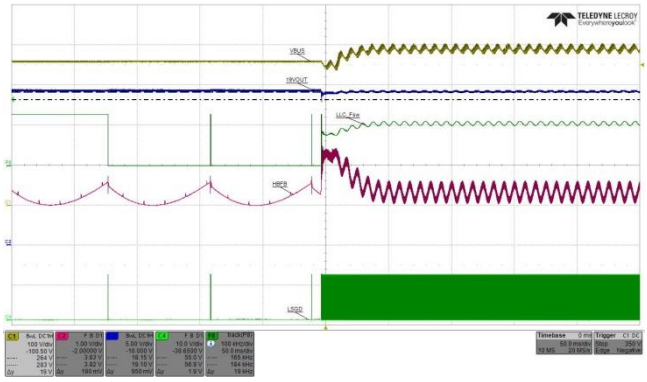
	
LLC jumps from full load to no load @ 110 V_{AC}	LLC jumps from no load to full load @ 110 V_{AC}

Figure 38 LLC entering/leaving burst mode operation at no load

10.18 LLC over current protection

The IDP2303A features two different over current protections: a first level overcurrent protection with the threshold $V_{\_OCP1}$ (there are 3 different $V_{\_OCP1}$ thresholds during soft-start, normal operation and burst mode, please refer to the datasheet) by software and a second level overcurrent protection with the threshold V_{OCP2} by hardware, where the threshold $V_{\_OCP1}$ is lower than the threshold V_{OCP2}. Overcurrent protection triggered by these two thresholds has different reactions in the HB LLC converter.

During LLC operation, the voltage across the shunt resistor R16 is compared with the threshold $V_{\_OCP1}$. Once the voltage is higher than the threshold, the LLC frequency will be increased to 200 kHz immediately, which is configurable and should be based on the LLC resonant tank design, followed by a soft-start. If during the soft-start, the over current situation is removed, the LLC will change from TCO to VCO and enter normal operation. But, if the overcurrent condition remains, after eight continuous OCP1 event triggers, the PFC and LLC will be stopped and enter auto-restart.

The second level over current protection is designed to prevent an extremely large current flowing through the shunt resistor. Once the LLC OCP2 is triggered, the PFC and LLC will immediately stop switching and enter auto-restart after two seconds break time.

In Figure 39, during normal operation, the first level OCP is triggered when the 19 V output is shorted to ground. Accordingly, the LLC switching frequency jumps to 200 kHz to limit the primary current. After eight continuous OCP1 triggers, the system enters auto-restart mode with two seconds break time. Once the overcurrent condition is removed, the system will recover with a soft-start.

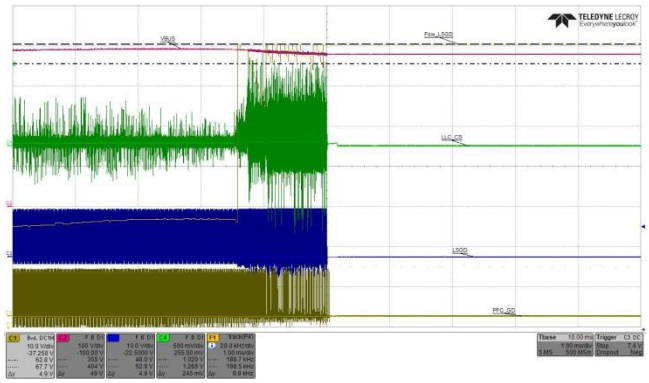
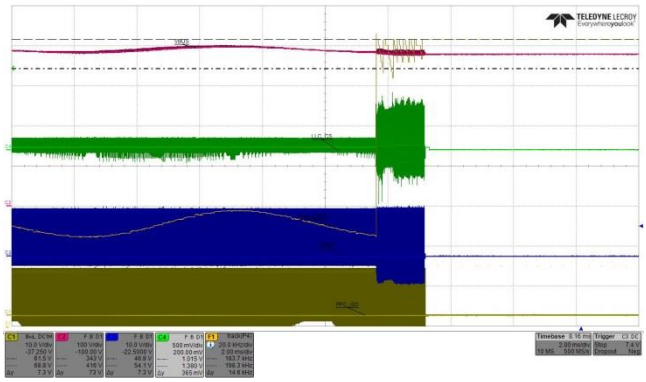
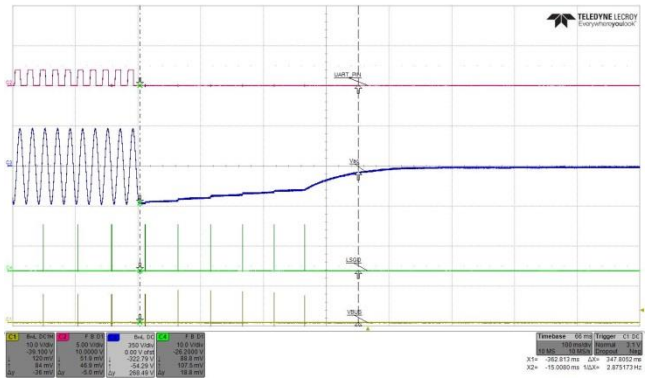
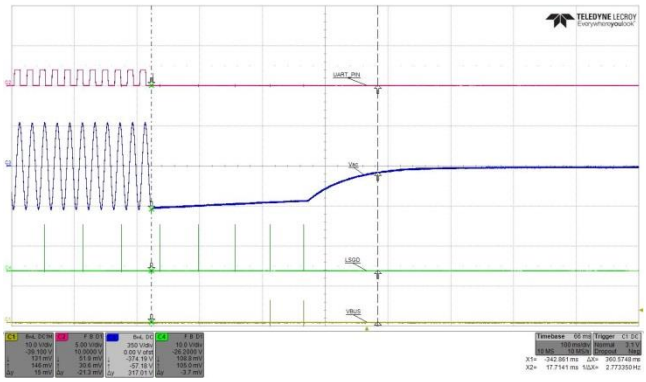
	
OCP1 @ 110 V_{AC} and 19 V output shorted	OCP1 @ 230V_{AC} and 19 V output shorted

Figure 39 LLC 1st level over current orotection

10.19 X-capacitor discharge during burst mode

In order to achieve low standby power consumption, the IDP2303A provides an active x-capacitor discharge feature to remove the passive discharge resistor. The AC input voltage is measured via a detection circuit to a UART pin during burst mode, and once the AC is unplugged, the IC detects the missing pulse. After a blanking time of 240 ms, it turns on the start-up cell to discharge the x-capacitor. For details, please refer to the IDP2303A datasheet.

In 0, the x-capacitor discharge feature during burst mode with typical standby loading is demonstrated, where it takes less than 1 s to detect and discharge the x-capacitor after the AC is unplugged.

	
X-capacitor discharge @ 230 V_{AC} and burst mode	X-capacitor discharge @ 264 V_{AC} and burst mode

X-capacitor discharge during burst mode

11 Configuration tools

The configurable parameters can be set via dpVision as shown in Figure 40. With selected applications, the table of configurable parameters can be loaded as shown in the right side of the figure. In order to provide a clear understanding, the parameters are explained with images, waveforms and descriptions. Detailed information about the configurable parameters is shown in the datasheet, and a detailed description of the configuration tool is shown in the dpVision user manual.

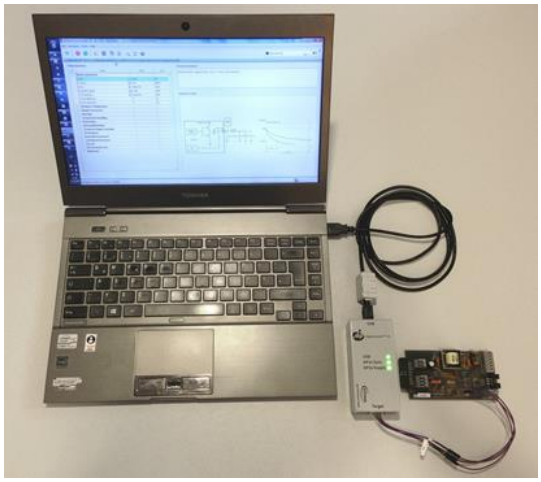
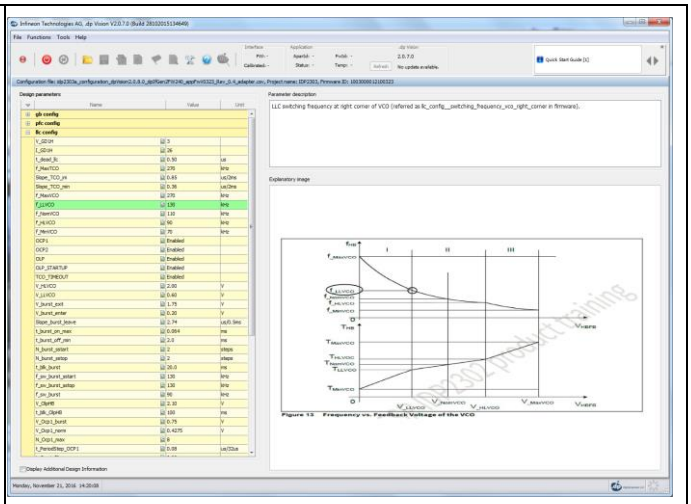
	
Configuration tool dpVision setup	dpVision parameter configuration page

Figure 40 Parameter configuration tool – dpVision

12 References

[1] IDP2303A datasheet, Infineon Technologies AG, 2016

[2] IPA60R230P6 datasheet, Infineon Technologies AG, 2015

[3] IPD50R380CE datasheet, Infineon Technologies AG, 2016

[4] BSC067N06LS3G datasheet, Infineon Technologies AG, 2013

Revision history

Major changes since the last revision

Page or Reference	Description of change
Page 20	Add leakage inductance

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