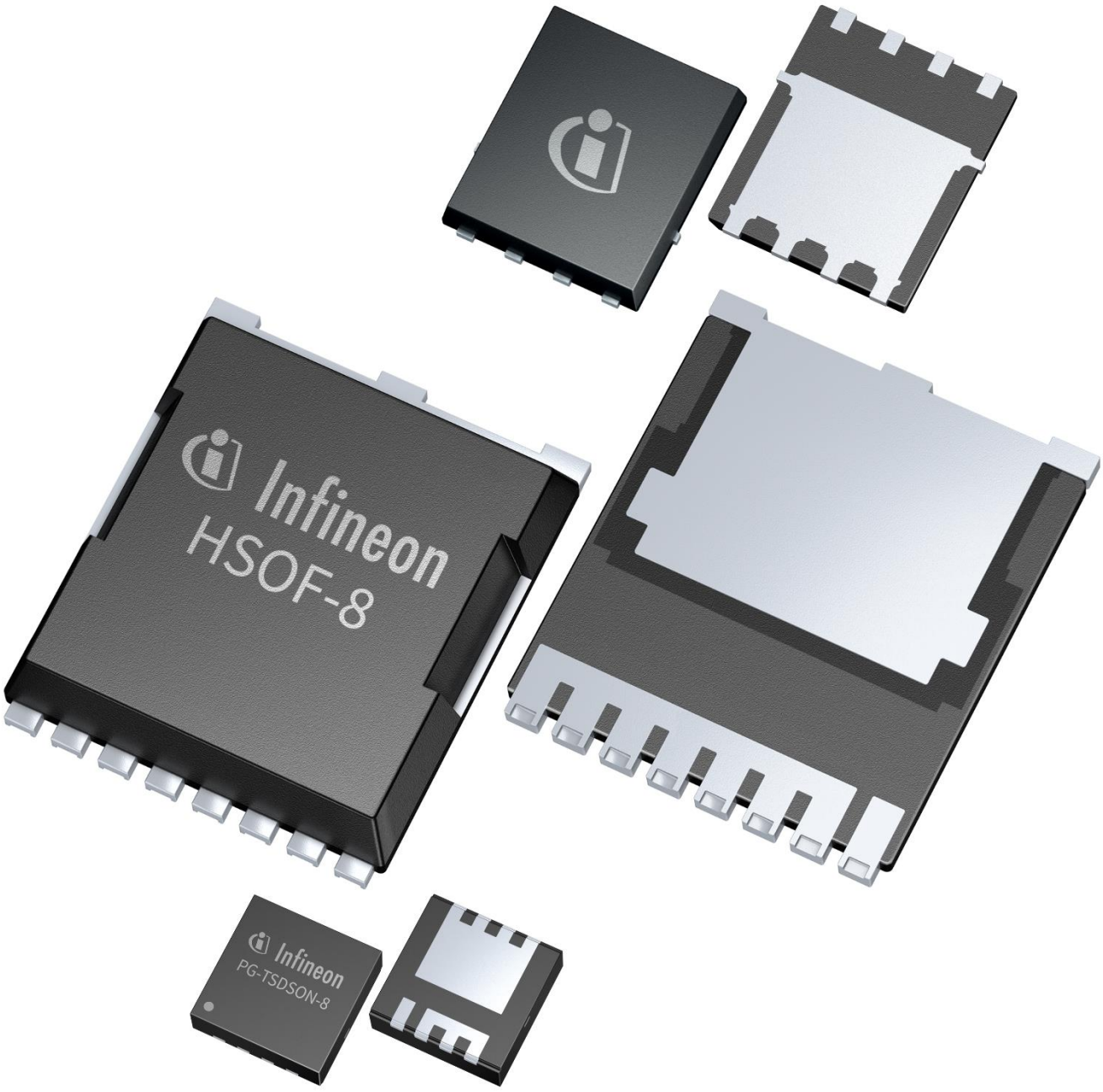
Recommendations for Board Assembly of Infineon Discrete Packages without Leads



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Acronyms and Abbreviations

AOI	Automated Optical Inspection
AXI	Automated X-ray Inspection
DSC	Double-Side Cooling
ESD	Electrostatic Discharge
FET	Field-Effect Transistor
HSOF	Heat Sink Small-Outline Flat lead
LTI	Lead Tip Inspection
NSMD	Non-Solder Mask Defined
PG	Plastic Green
PCB	Printed Circuit Board
PQFN	Power Quad Flat No-lead
QFN	Quad-Flat No-lead
SMD	Solder-Mask Defined
SMD	Surface-Mount Device
SMT	Surface-Mount Technology
SO8	Small-Outline 8 pin
S2O8	SuperSO8
S3O8	Shrink SuperSO8
SSO8	SuperSO8
TDSON	Thin Dual Small-Outline Non-leaded
TOLL	Transistor Outline Lead-Less
TSON	Thin Small-Outline Non-leaded
TSDSON	Thin Shrink Dual Small-Outline Non-leaded
USON	Ultra-thin Small-Outline Non-leaded
VSON	Very thin Small-Outline Non-leaded
WSON	Very Very thin Small-Outline Non-leaded

1 Package Description

This document provides information about the Surface Mount Technology (SMT) board assembly of packages with non-leaded, leadless and short flat terminations that protrude from the package mold body without having a distinctly solderable sidewall.

This recommendation does not discuss Quad-Flat No-lead packages (QFN) or Thin Small Leadless/ Non-Leaded Packages (TSNP/TSLP). These package families are described in separate documents.

1.1 SON and TFN Package Type

Infineon Small Outline Non-leaded (SON) packages are available in various families. Some of the packages are also called Power Quad Flat No-Lead (PQFN). Further designations for TDSON-8 packages include “Small-Outline package 8 pin” (SO8), “SuperSO8” (SSO8, S2O8). The TSDSON-8 package can also be found as “Shrink SuperSO8” (S3O8). The Thin Tri-side Flat-pack Non-leaded packages (TTFN) use three sides of the package outline for termination access instead the otherwise used dual side approach. **Figure 1** shows examples of the SON and TFN package family.

- PG-TSON packages
- PG-T(S)DSON packages
- PG-LSON packages
- PG-USON packages
- PG-VSON packages
- PG-WSON packages
- PG-TTFN packages

PG = Plastic Green
T = Thin
S = Shrink
D = Dual
L = Low profile
V = Very thin
W = Very Very thin
U = Ultra-thin
SO = Small Outline
TF = Tri-side Flat-pack
N = Non-leaded

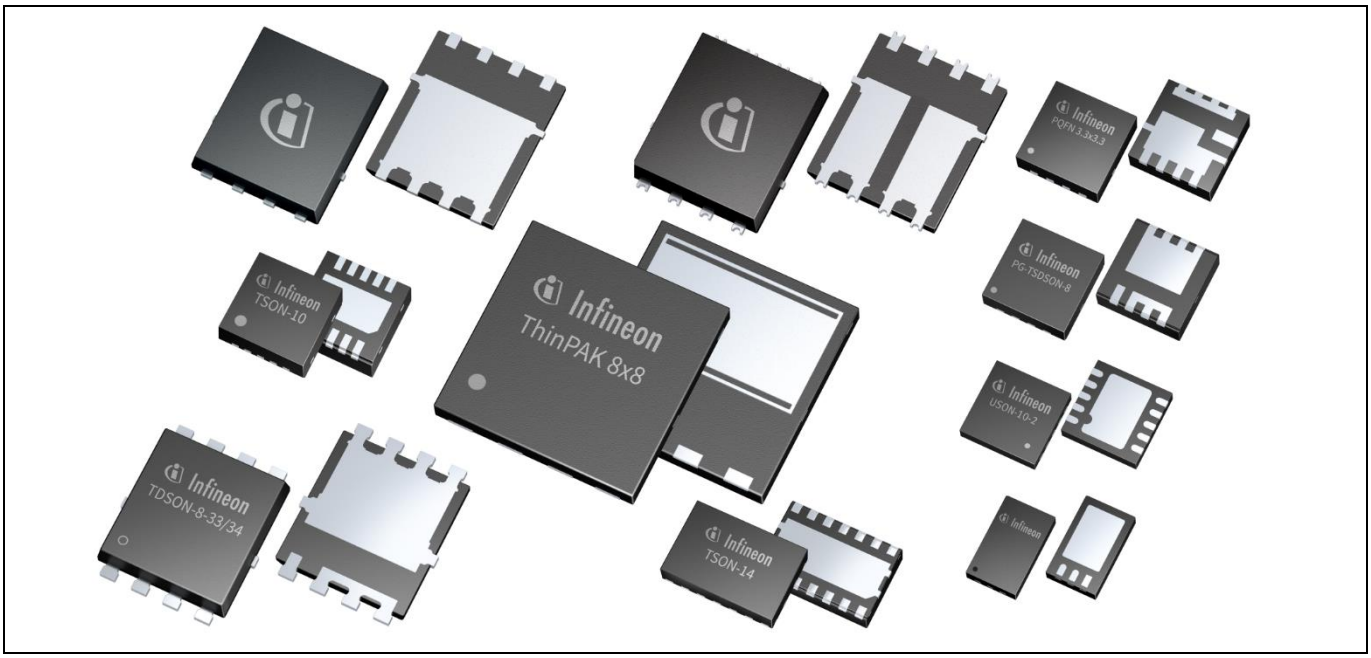

Figure 1 Examples of SON and TFN packages.

1.2 HSOF Package Type

Infineon Heat Sink Small Outline Flat leaded (HSOF) packages include different footprint designs. Another designation for these packages is “Transistor Outline Leadless” or “TO-Leadless” (TOLL). The smaller package version is also called “shrink TOLL” or “sTOLL”. Examples of the HSOF package family can be seen in **Figure 2**.

- PG-HSOF packages

PG = Plastic Green
H = Heat Sink
SOF = Small Outline Flat lead

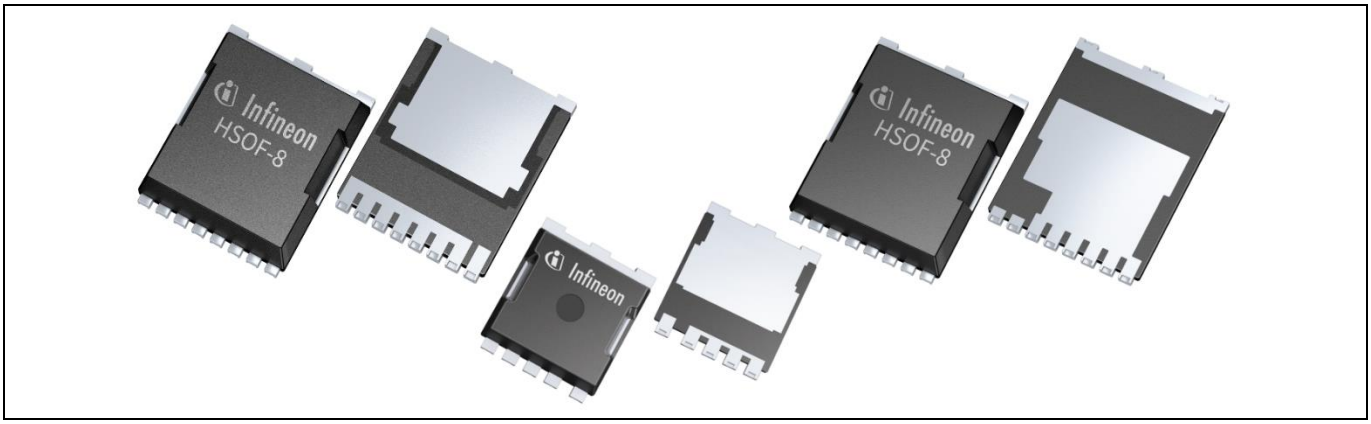

Figure 2 Examples of HSOF packages.

1.3 Non-Leaded Package Types with Double-Side Cooling

The Double-Side Cooling (DSC) concept allows for adding an additional thermal drain to the package. The second heat slug on top of the component provides a superior thermal management and the possibility to decouple a heatsink or heatspreader mounting from the PCB pad design. Infineon offers packages from the SON family with DSC features. **Figure 3** shows examples of non-leaded DSC type packages.

- PG-WSON packages

PG = Plastic Green
W = Very Very thin
SO = Small Outline
N = Non-leaded

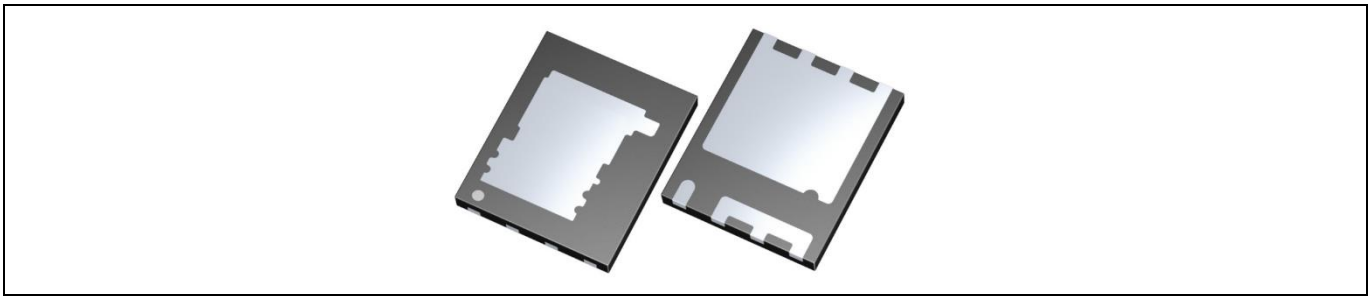

Figure 3 Example of a non-leaded DSC package.

For information about the optimal thermal management and assembly considerations such as top-side heatsink mounting, please contact your local Infineon sales, application, or quality engineer.

1.4 Package Features and General Handling Guidelines

The components of the SON and HSOF families feature near-chip-scale plastic encapsulated packages with a copper leadframe using perimeter lands on the bottom of each package to provide electrical and thermal contact to the Printed Circuit Board (PCB).

The SON package family covers a large variety of applications including power and non-power versions with different termination types such as flat and non-leaded with various package thicknesses from thin to ultra-thin.

General Handling Guidelines

Semiconductor devices are sensitive to excessive electrostatic discharge (ESD), moisture, mechanical handling, and contamination. Therefore, they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing.

For further information about component handling, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Internal Construction

Depending on the thermal output produced by the die, areas for heat transfer are provided by appropriately dimensioned exposed die pads. Dual-pad versions of the TDSON-8 even contain two separated Field-Effect Transistor (FET) dies with full thermal management capabilities for both devices on a so-called half-bridge configuration.

The electrical connection between the die and the leadframe can be implemented in various ways as shown in **Figure 4**. There are multiple versions of packages with wire bond as well as with copper clip interconnects but also such featuring both. Packages with copper clip interconnect provide an overall low conduction resistance due to the increased conductor cross section. Packages with top-side heat slug basically feature and extended copper clip that protrudes the top outline of the mold body.

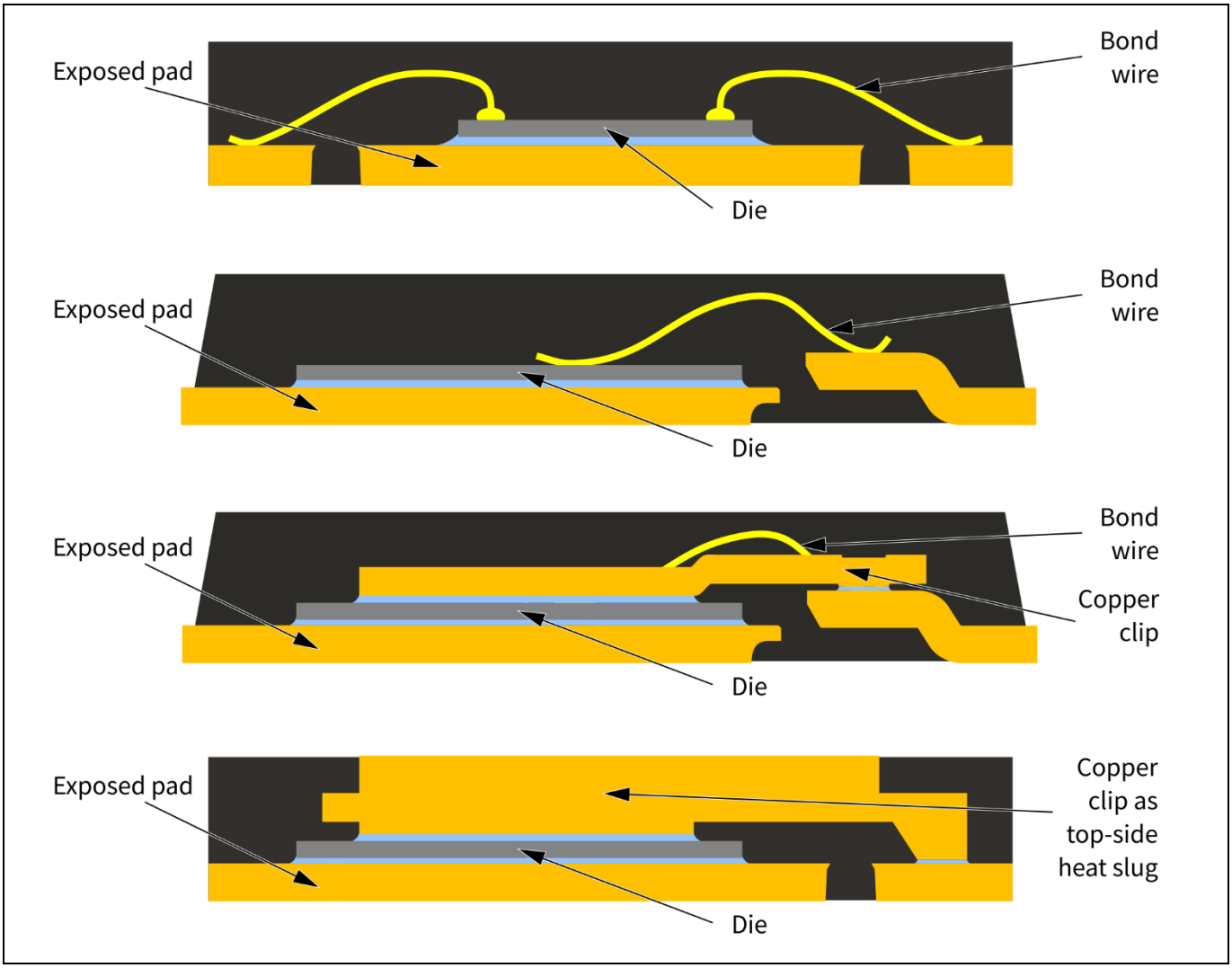

Figure 4 **Schematics showing the inner setups (from top to bottom) of a configuration with two-side wire bonds, with one side wire bond, with a combination of copper clip and wire bond (also with copper clip only possible), and with a copper clip that is extended to a heat slug for enabling top-side cooling.**

Termination Design

The non-leaded land pattern provides for optimal electrical performance due to decreased conductor lengths, while optimizing the package-to-chip ratio.

Fused-lead version packages have interconnected source leads that serve as a combined external termination and therefore provide an extended path for heat dissipation and current which prevents current crowding.

Lead Tip Inspection (LTI) features provide a partial or full plating of the termination tip as can be seen in **Figure 5**. The features allow for Automated Optical Inspection (AOI) of the solder joint connection and are available for various Infineon SON and HSOF components.

For further information about LTI features, please contact your local Infineon sales, application, or quality engineer.

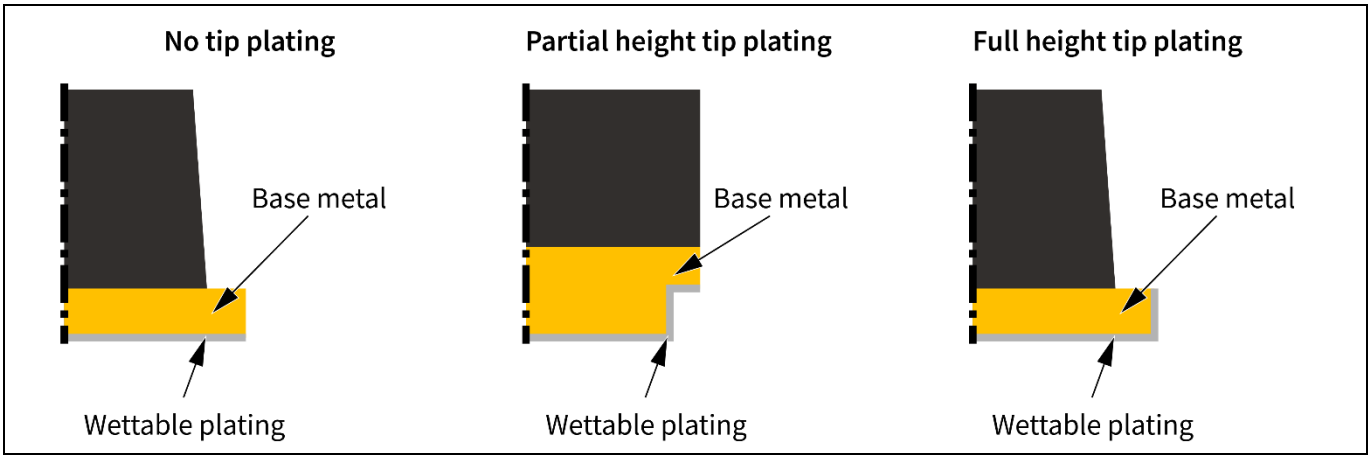

Figure 5 Schematic comparison of termination tip without (left) and with different LTI variants (center and right).

Figure 6 and **Figure 7** show cross-sections of terminations with and without LTI features, and variants of solder joint fillet formation at the termination tips.

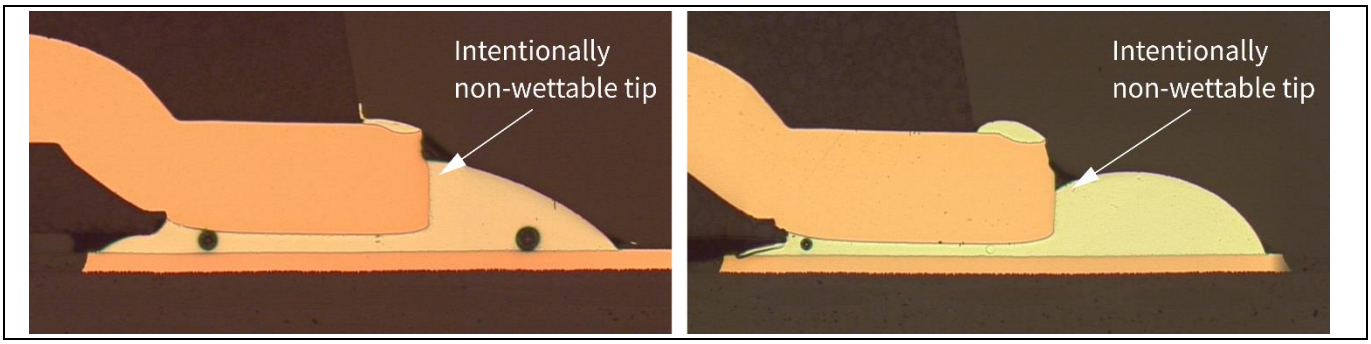

Figure 6 Cross sections of TDSON-8 without LTI. The wetting behavior on the cut edge is inconsistent.

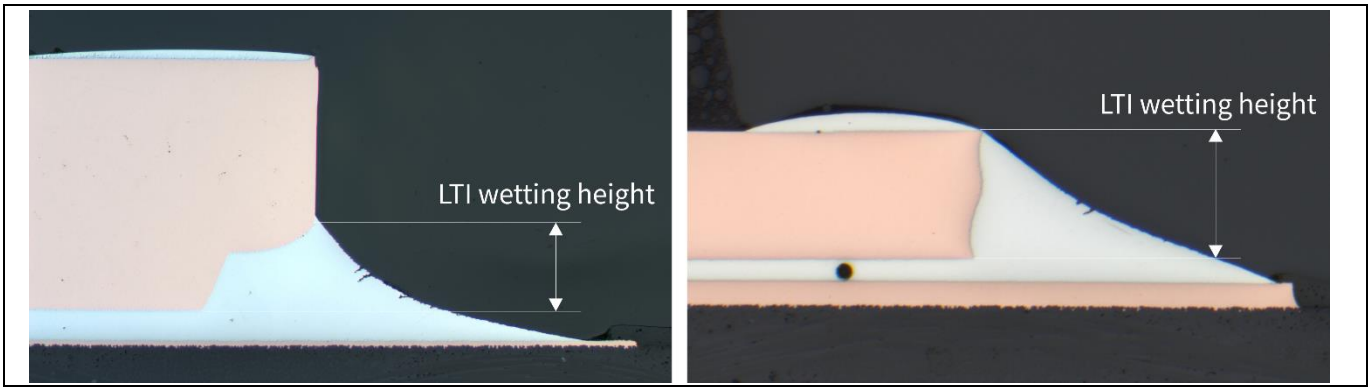

Figure 7 Cross section of a soldered trapezium groove LTI on the HSOF-8 (left) and of a soldered fully plated LTI on the TDSON-8 (right).

2 Printed Circuit Board

2.1 Routing

Printed circuit board design and construction are key factors for achieving solder joints with high reliability. Packages with exposed pads should not be placed opposite to each other on either side of a PCB if double-sided mounting is used. This will stiffen the assembly and cause solder joints to fatigue earlier than in a design in which the components are offset. Furthermore, the board stiffness itself has a significant influence on the reliability of the solder joint interconnect if the system is used in critical temperature-cycling conditions.

2.2 Pad Design

The quality and reliability of interconnect solder joints to the board are affected by:

- Pad type (Solder-Mask Defined, SMD or Non-Solder-Mask Defined, NSMD)
- Specific pad dimensions
- Pad finish (also called metallization or final finish)
- Via layout and technology

Beside their electrical function, the exposed pads on the landing area of the SON and HSOF packages are designed to conduct high thermal loads into the PCB in order to achieve an optimal thermal performance. Therefore, the exposed pad area on the PCB should be congruent with the area on the package. For optimal heat dissipation in high-current applications, the SMD pad type is preferred since it allows for large copper areas under the solder mask layer of the PCB. Beside the power application aspect, the SMD design type can also be beneficial in terms of routing flexibility. If the central die pad is not used as a thermal pad, it is still a connection to ground. Using a PCB pad of the same size as the package pad will increase the solder joint reliability and the electrical performance for some applications. A comparison between a SMD pad design for power application with an NSMD pad design is shown in **Figure 8**. Mixing different pad definition types in one footprint is not recommended.

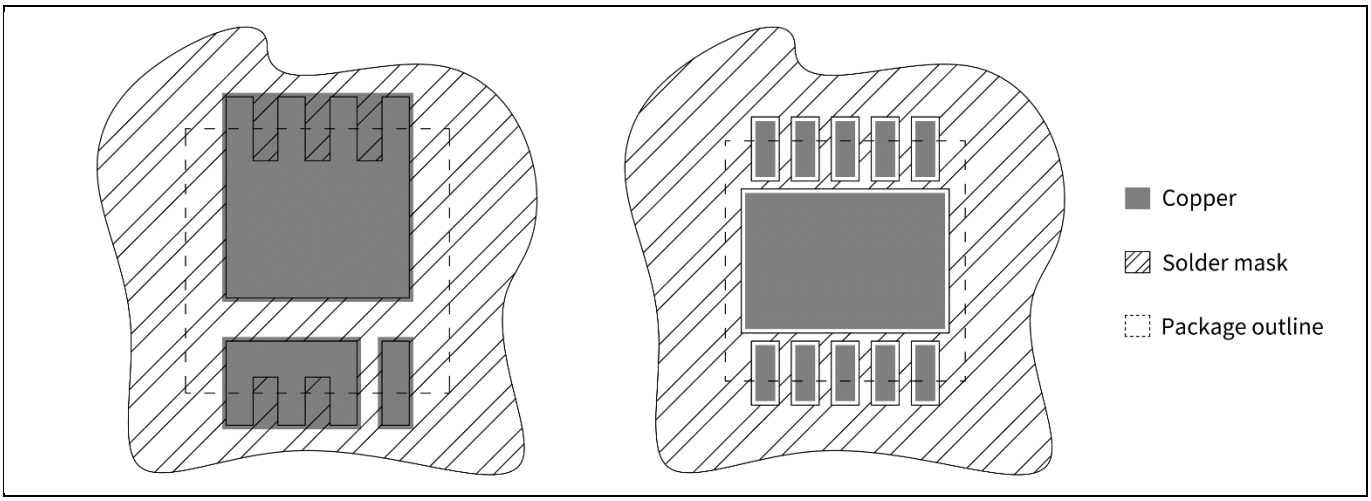

Figure 8 Example of SMD pads for a TSDSON-8 power package (left) and of NSMD pads for an USON-10 package (right).

Figure 9 shows three different kinds of leadless or non-leaded component terminations. By taking into account the bare copper areas of cut edges that are not intended to be wettable by design (see also IPC-A-610 [6]) as well as natural mold flash areas, all terminations can be considered to be of the “bottom-only” type. In order to

support the self-aligning effect by the liquid solder wetting forces during reflow, it is recommended to extend the PCB pads by approx. 250 µm beyond the package perimeter and by approx. 50 µm in the heel region of the termination (see **Figure 11**).

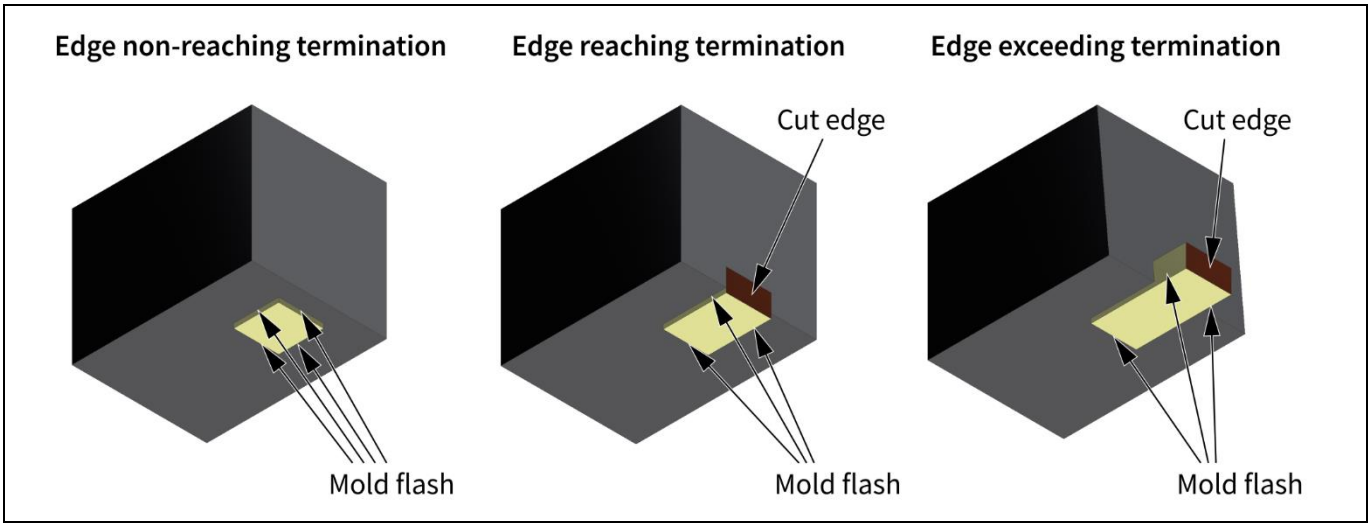

Figure 9 Models of the basic termination types with wettable areas on bottom only. Cut edge areas and such covered with mold flash are considered to be non-wettable by design.

Generally, an optimal PCB design depends on the specific application as well as on the specific design rules of the chosen board manufacturer.

For further information about PCB pad design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Pad Design for LTI Features

Depending on the termination type different LTI feature geometries are available which can be seen in **Figure 10**. The features can be of different width and height depending on the specific termination geometry.

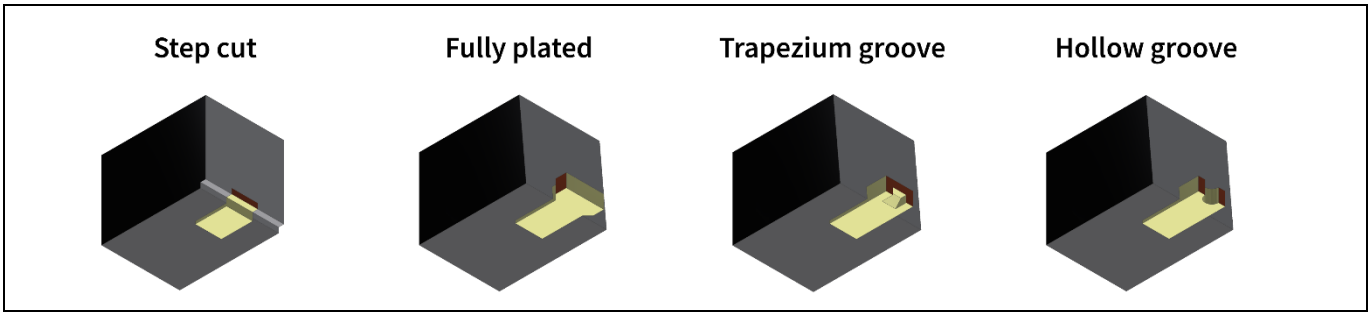

Figure 10 Available LTI features on SON and SOF packages.

To ensure an optimal response during the AOI, the pad extension should be increased to more than 400 µm rather than the above-mentioned approx. 250 µm for standard terminations. The solder paste volume should be accordingly increased by a sufficient amount to ensure a homogeneous and reproducible solder joint fillet formation at the termination tip. The increased extension of the PCB pad for LTI-featured terminations for optimal solder meniscus formation is shown schematically in **Figure 11**.

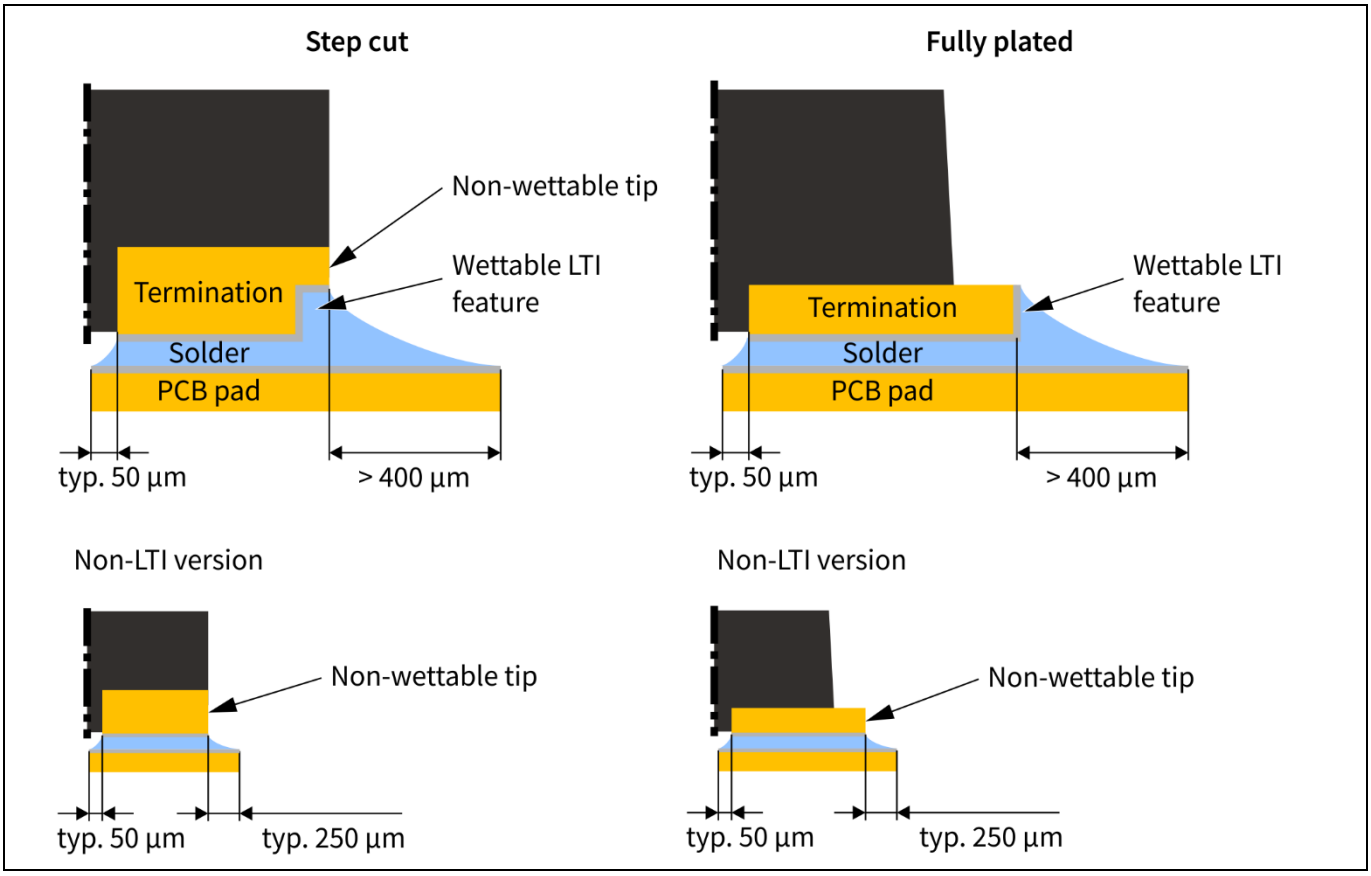

Figure 11 Schematic comparisons of a "step cut" LTI example with partial leadframe thickness wetting height, and a "fully plated" LTI example with full leadframe thickness wetting height. For comparison, non-LTI examples are shown (lower 2 illustrations). For complete LTI functionality, a distinct solder meniscus must be formed at the termination tip by sufficient extension of the pad over the package edge.

For further information about PCB pad design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1].

Further details and specific footprint recommendations can be found in the package data base that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show an example of the footprint layout for each package.

Please also feel free to contact your local sales, application, or quality engineer.

2.3 Via-in-Pad Design

Thermal and electrical connections to the inner and/or bottom copper planes of the PCB are usually created by plated through-hole vias in the board. The heat is then transferred from the chip over the package die pad and the solder joint to the thermal pad on the board and further through the PCB by the thermal vias.

The diameter and the number of vias in the thermal pad depend on the specific thermal requirements of the final product, the power consumption of the product, the application, and the construction of the PCB. A typical hole diameter for thermal vias is 0.2 - 0.5 mm. An array with 1.0 - 1.2 mm pitch can be a reasonable starting point for further design optimization. The implementation of thermal vias has several impacts on the board assembly as outlined below. A constant increase of number of vias does not necessarily translate into a constant decrease of the thermal resistance of the entire assembly set-up. Thermal and electrical analysis

and/or testing together with a proper board assembly design procedure are recommended to determine the optimal number of vias needed.

One of the primary exposed pad design objectives, besides the thermal management, should be to avoid the penetration of the vias by solder. Consequences of solder penetration can be a decreased stand-off between the PCB and the package, an increased void formation ultimately resulting in an insufficient solder joint area or surplus solder on the opposite side of the PCB.

A first approach for risk reduction should be the prevention of a direct print of solder paste on the via opening. Since the stencil for large area prints such as on die pads is usually segmented, it is a good practice to position the vias under the beam intersections of the aperture as shown in **Figure 12**. With such an approach, a good solder joint on a central die pad can be formed using vias that remain open on both sides of the board.

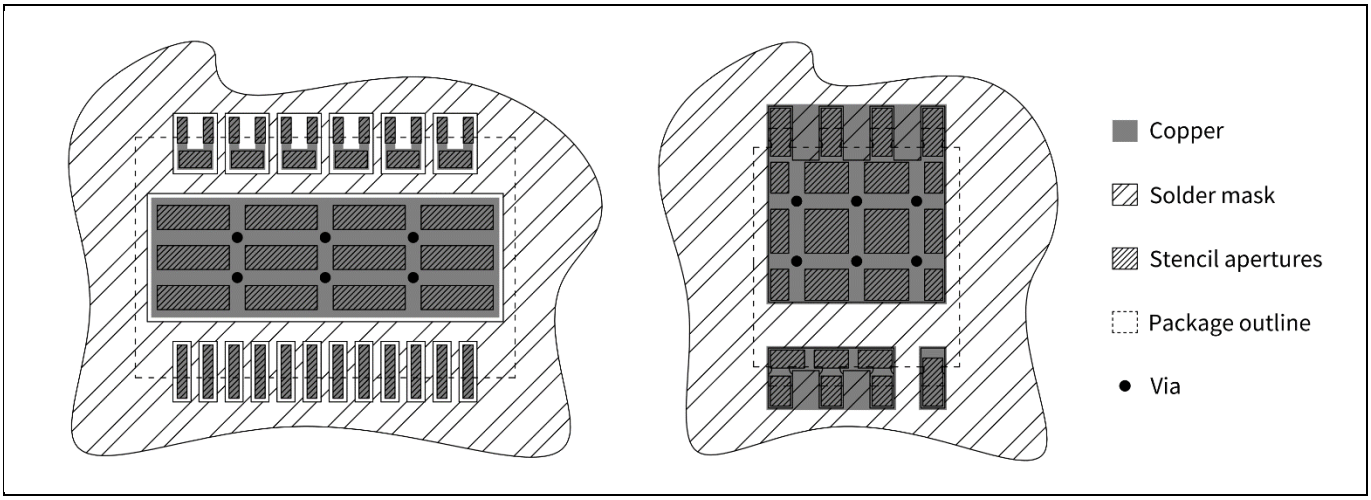

Figure 12 Exemplary via-in-pad designs for a TSON (left) and a TDSON component (right).

Components with a non-centered die pad tend to tilt due to the varying solder volume along the package axis. Therefore, despite of the precautionary stencil design approach, the solder can move into the via, driven by the wetting forces. If the solder then protrudes to the opposite side of the PCB, it may interfere with a second solder paste print process. To minimize the effect, dummy areas on the opposite side as shown in **Figure 13** can sequester the surplus solder to avoid beading and solder lumping.

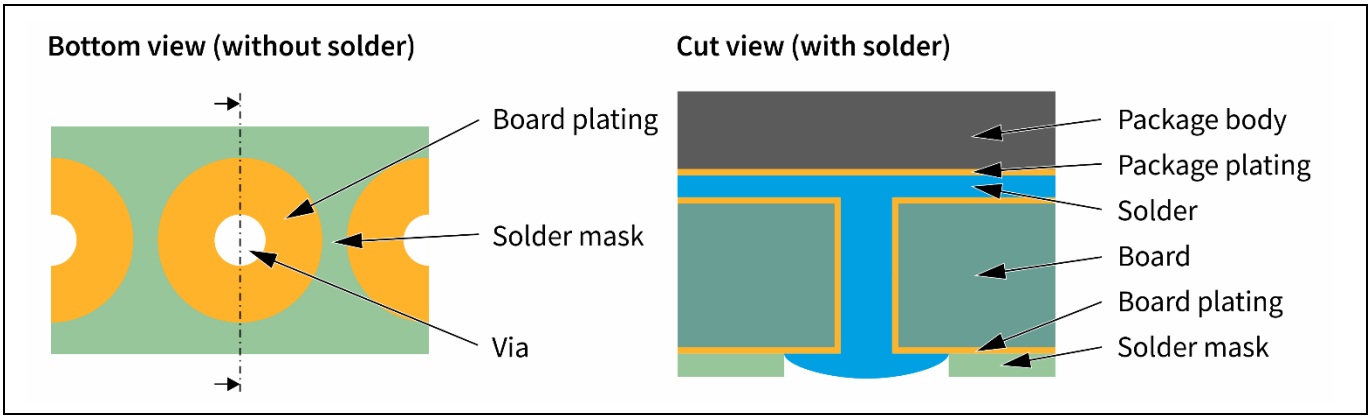

Figure 13 Wettable “dummy” area on the opposite side of the board surrounds the vias to act as a buffer for surplus solder.

Printed Circuit Board

In case the solder variance in volume below the die pad is too high due to the wetting of vias, they can be closed by “tenting.” This process includes covering the vias by a solder mask (e.g. dry-film solder mask). If the via tenting is done only on the opposite side of the board, the voiding rate will increase significantly. Another method to close vias is called “plugging” (filling with epoxy), followed by overplating. Very small vias (100 µm in diameter or smaller) should be filled with copper and overplated. In both cases, the specification of a planar filling is necessary to avoid cavities that will trap gases, forming voids during reflow soldering.

In case it is not necessary to provide a direct connection from the solder pad under the exposed die pad to the inner layers of the PCB, the vias can be placed next to the footprint near the package and covered with solder mask.

For further information about vias in pad, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3 PCB Assembly

3.1 Solder Paste Stencil

In SMT the solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. While an excessive solder paste volume will cause solder bridging, an insufficient solder paste volume can lead to reduced solder spreading between all contact surfaces. To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut (mostly made from stainless steel) or electroformed stencils (nickel) are preferred. The latter are applied especially when fine-pitch components are assembled.

The stencil apertures are usually of the same dimensions as the relevant pad on the PCB (not counting possible edge rounding). In most cases, the thickness of a stencil has to be matched to the needs of all components on the PCB. For typical Power-SON packages, 120 µm to 150 µm thick stencils are recommended (for small pitch versions, a 100 µm thick stencil is recommended).

The solder paste volume in apertures larger than approximately 5 mm may be scooped out depending on the specific squeegee pressure and rigidity. Such apertures are necessary for many die pad prints, should be segmented into smaller areas. The reduction of the die pad print also reduces the tilt of non-symmetric components towards the leads side. Internal investigations have shown that the ratio between stencil openings and drain pad can vary from 50% to 65% (in special cases even from 40% to 80%). When reducing the die pad print, potential vias in the pad have to be considered as outlined in the relevant section above.

For individual design adaptations to reach the optimal amount of solder, the stencil thickness, the PCB pad finish, quality and solder masking, the via layout, and the solder paste type should be considered. In every case, application-specific experiments are recommended.

Further details and specific stencil aperture recommendations can be found in the package data base that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show an example of the stencil aperture layout for each package.

For further information about solder stencil design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.2 Solder Paste

Pb-free solder pastes typically contain some type of SnAgCu alloy (SAC solder with typically 1-4% Ag and <1% Cu). The most common alloy is SAC305 (3.0% Ag and 0.5% Cu). The average alloy particle size must be suitable for printing the solder stencil aperture dimensions. Using Type 3 or Type 4 paste is recommended for the assembly of integrated SON and HSOF components, depending on the specific stencil aperture size and therefore solder paste transfer efficiency.

The solder alloy particles are dispersed in a blend of liquid flux and chemical additives (approx. 50% by volume or 10% by weight), forming a creamy paste. The flux and chemical solvents have various functions such as adjusting the viscosity of the paste for stencil printing or removing contaminants and oxides on the surface.

The solder paste solvents have to evaporate during reflow soldering, while residues of the flux will remain on the joint. The capacity of the flux additive for removing oxides is given by its activation level, which also affects the potential need for removing the flux residuals after the assembly. For leadless packages in which the solder joint is formed mainly on the package bottom side, a “no clean” paste is recommended to avoid subsequent cleaning steps underneath the package. The small gaps make cleaning highly difficult if not impossible. Certain precautions have to be taken if any kinds of flux residues remain on the board prior to any kind of coating. For

power packages, leakage currents and the potential for shorting below components have to be considered when choosing the specific flux type (e.g. halide-free vs. zero halides).

Generally, solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.3 Component Placement

Although the self-alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints, the components have to be placed accurately depending on their geometry. Positioning the packages manually is not recommended, especially for packages with small terminations and pitch. An automated pick-and-place machine is recommended to obtain reliable solder joints.

Component placement accuracies of +/-50 µm and less are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or at additional individual mounting positions (local fiducials). These fiducials are detected by a vision system immediately prior to the mounting process.

For further information about component placement, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.4 Reflow Soldering

For printed PCB assembly of the HSOF and SON components, the widely used method of reflow soldering in a forced convection oven is recommended. Soldering in a nitrogen atmosphere can generally improve the solder joint quality but is not necessary to create a reliable joint.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to reach an optimal solder joint quality. The position and the surrounding of the component on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly. Power packages where leakage currents and shorting below the component have to be considered should be soldered with decreased flux spreading. Therefore, it is recommended to optimize the reflow profile in such a way that excessive flux or solder spattering is avoided.

Minimum Reflow Conditions

The lower temperatures and durations of an optimal reflow profile shall stay above those of the solderability qualification. The solderability of the terminations of Infineon components is tested according to the standards IEC 60068-2-58 and J-STD-002 [2][3].

Maximum Reflow Conditions and Cycles

Components which are Moisture-Sensitivity Level (MSL) classified by Infineon have been tested by three reflow runs in accordance with the J-STD-020 standard, including a double-sided reflow and one rework cycle. The maximum temperatures must not be exceeded during board assembly. Please refer to the product barcode label on the packing material that states this maximum reflow temperature according to the J-STD-020 [4] standard as well as the MSL according to the J-STD-033 standard [5].

HSOF and SON packages are generally suited for mounting on double-sided PCBs. If the solder joint thickness is a critical dimension, solder joints of components on the first side will again reflow in the second step. In the reflow zone of the oven (i.e. where the solder is liquid), the components are only held in place by wetting forces from the molten solder. Gravity acting in the opposite direction will elongate the solder joints, unlike joints on

the top side, where gravity will force the components closer to the PCB surface. This shape will be frozen during cooling and therefore will result in a higher stand-off on the bottom side after the reflow process. Heavy vibrations in a reflow oven may cause devices to drop off the PCB.

For further information about reflow soldering, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

4 Cleaning

After the soldering process, some flux residues may remain on the board, especially near the solder joints. Generally, cleaning beneath a component with bottom-only terminations is difficult due to the small gap between the component body and the PCB. Therefore, a “no-clean” flux is recommended whose residues usually do not have to be removed after the soldering process.

In case the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and cleaning solution have to be selected while taking into account the type of package, the flux used in the solder paste (rosin/resin-based, water-soluble, etc.) as well as the environmental and safety aspects. Even small residues of the cleaning solution should be removed or dried out very thoroughly. For recommended cleaning solutions, please contact the solder paste or flux manufacturer.

5 Inspection

5.1 Optical Solder Joint Inspection

Compared to leaded SMD components (e.g. the gullwing type), the solder joints of SON and HSOF components are mainly formed underneath the package. **Figure 14** shows a TDSON-8 with several termination locations. They can be situated stand-alone as single ones, they can be fused together by a small bridge, or they can be fused together to the die pad. The last two types allow for an optimized current distribution. Components with non-symmetric footprints tend to tilt slightly. The tips of the terminations often have bare copper (e.g. cut edges) that are not intended to wet by design according to the IPC-A-610 [6]. Non-wetting of the termination tip is not a criterion for rejection. Consequently, reliable visual inspection of such solder joints with conventional AOI systems is limited.

LTI features allow for automated optical inspection of the solder joint quality at the termination tips. In case the termination is fused together with the exposed pad, the solder joint fillet formation on the LTI on the die pad side may differ from that on the single termination side. This effect is shown in **Figure 15** and **Figure 16**.

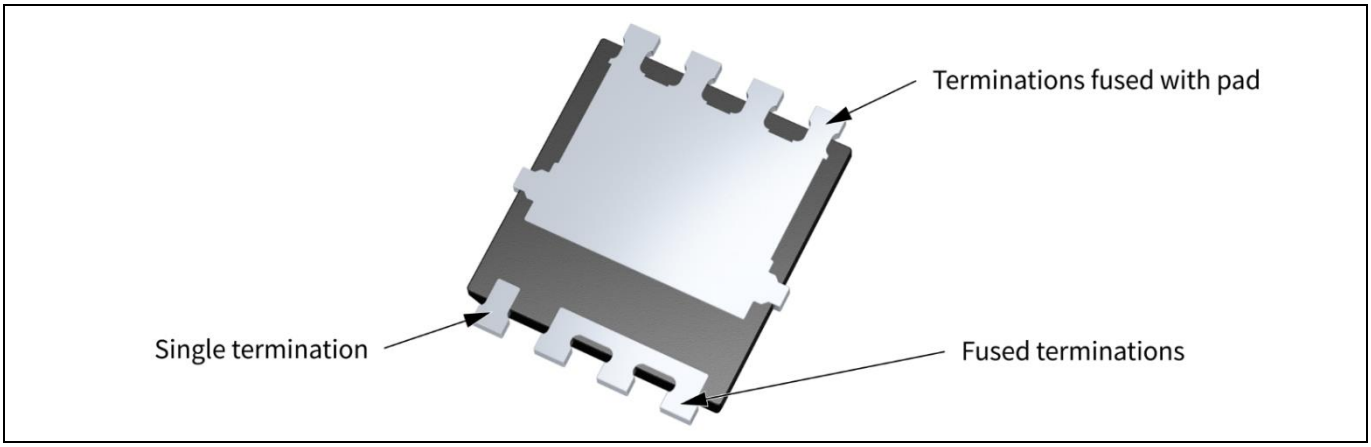

Figure 14 TDSON-8 package landing area showing the various termination characteristics.

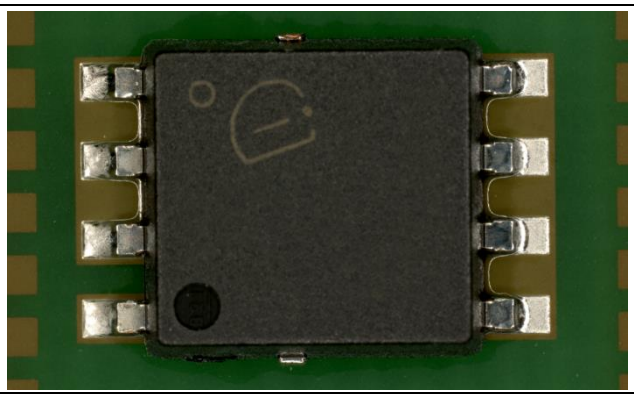

Figure 15 Photograph of a TDSON-8 with LTI solder joints on a test board. The different appearance of the gate and source leads on the left side compared to the leads fused with the pad on the right side is visible.

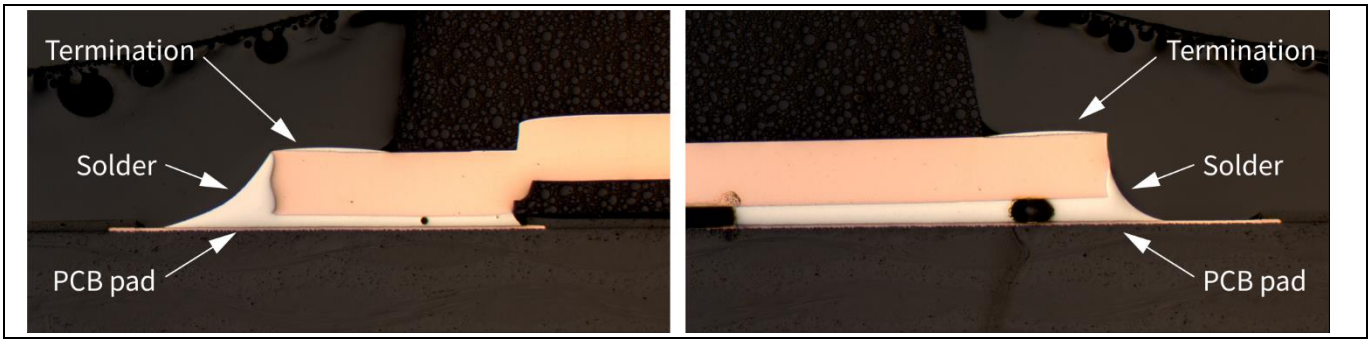

Figure 16 Cross section of a TDSON-8 assembled on board. The natural tilt of the package is visible causing the different appearance of the solder joint fillet on leads that are fused with the pad (right) compared to the single ones (left). However, the LTI tips are wetting properly on both sides.

For engineering tasks, cross-sectioning can offer detailed information about the solder joint quality. Due to its destructive character, cross-sectioning during monitoring is naturally not practical.

For further information about the acceptability of electronic assemblies inspected optically, please also refer to the IPC-A-610 standard [6].

5.2 X-Ray Solder Joint Inspection

Automated X-ray Inspection (AXI) systems are appropriate for efficient inline control of components that cannot be inspected properly by optical systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analyzing, and data transferring routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray.

Figure 17 shows typical X-ray photographs of TDSON-8 and TSDSON-8 components. Internal solder joints, wire and clip bonds, leadframe, and the solder joints that connect the package to the PCB are visible. Large exposed pads may tend to increase voiding because they do not provide a sufficient ratio between volume and surface necessary for proper outgassing of the organic compounds during reflow. Generally, the extent of voiding depends on the board pad size, the stencil layout, the solder paste, the reflow profile, and the via layout. For thermal evaluations, the entire thermal path must be considered as well as all boundary conditions such as the application environment or the electrical use of the component.

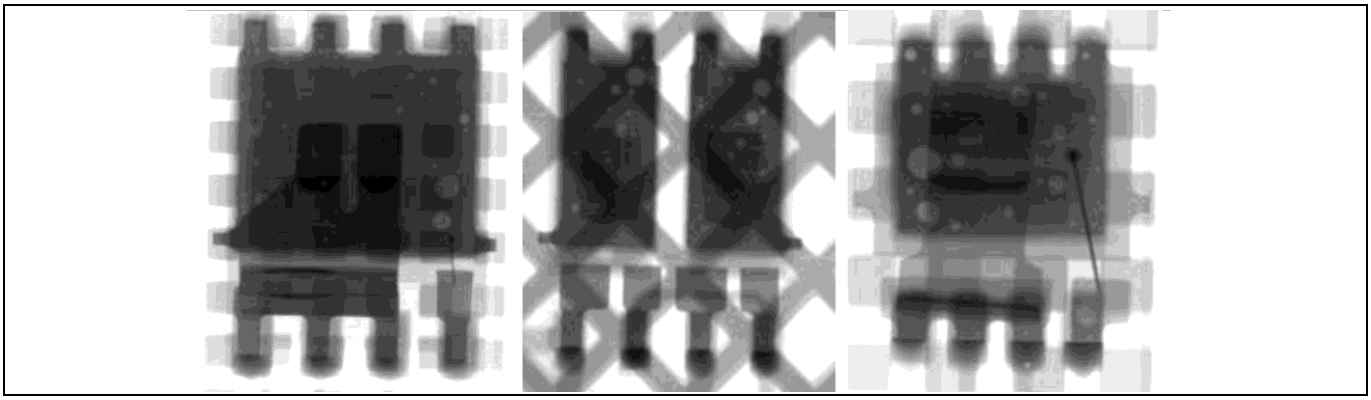

Figure 17 X-ray photographs of properly a soldered TDSON-8 (left), a TDSON-8 with dual pad (center), and a TSDSON-8 (right).

6 Rework

Single solder joint repair of bottom-only terminated packages is highly difficult, if not impossible, and is therefore generally not recommended. Furthermore, the reuse of de-soldered components is not recommended. The de-soldered components should be replaced by new ones.

A rework process is commonly done on special rework equipment. There are various systems available that meet the requirements for reworking SMD packages. All handling guidelines discussed in this document have to be respected. Special focus should be on the following items:

- Due to the decreased automation level given by the general rework approach, even higher care compared to standard assembly must be taken. Tools that do not damage the component mechanically have to be chosen. Mechanical forces that do not necessarily cause visible external damage can still cause internal damage that reduces the component's reliability. A proper handling system with vacuum nozzle may be the gentlest process and is therefore recommended. However, the impact of rework tools has to be assessed properly. In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es).
- During rework, special care must be taken concerning the proper moisture level of the component according to the J-STD-033. Drying the PCB and the component prior to rework might be necessary. A proper drying procedure for SMD packages is described in the international J-STD-033 standard [5]. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum temperature according to the J-STD-020 standard. Depending on the specific heating profile used during rework, components adjacent to the mounting location might also experience a further "reflow run" in terms of the J-STD-020 standard [4]. Internal investigations have shown that the temperature profile must be recorded.

If a device is suspected to be defective and a failure analysis is planned, Infineon usually expects customers to desolder the component prior to return to Infineon. The component shall be returned in a proper condition according to the original package outlines.

In some special cases such as solder joint inspection Infineon may request that the PCB or part of the PCB with the component still attached should be sent to Infineon.

Note: *Before returning a device for failure analysis at Infineon, please clarify the return condition of the suspected component (i.e. onboard or desoldered) with the Infineon Application Engineer or Customer Quality Manager who supports your company.*

For further information about component rework on PCB, please refer to the General Recommendations for Board Assembly of Infineon Packages document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

7 References

[1] Infineon Technologies: Packages. www.infineon.com\packages.

[2] International Electrotechnical Commission: IEC 60068-2-58. Environmental testing - Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD).

[3] Electronic Components Industry Association, Assembly and Joining Processes and JEDEC Solid State Technology Association Committee: EIA/IPC/JEDEC J-STD-002. Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.

[4] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-020. Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices.

[5] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-033. Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

[6] Association Connecting Electronics Industries: IPC-A-610. Acceptability of Electronic Assemblies.

Revision History

Page or reference	Major changes since the last revision
Section 1 “Package Description”	Introduction of double-side cooled packages.
Section “Pad Design for LTI Features”	Moved from section 2.3 to section 2.2.
Section 7 “Rework”	Update of sample conditions in case of return.
Entire document	Editorial review.

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