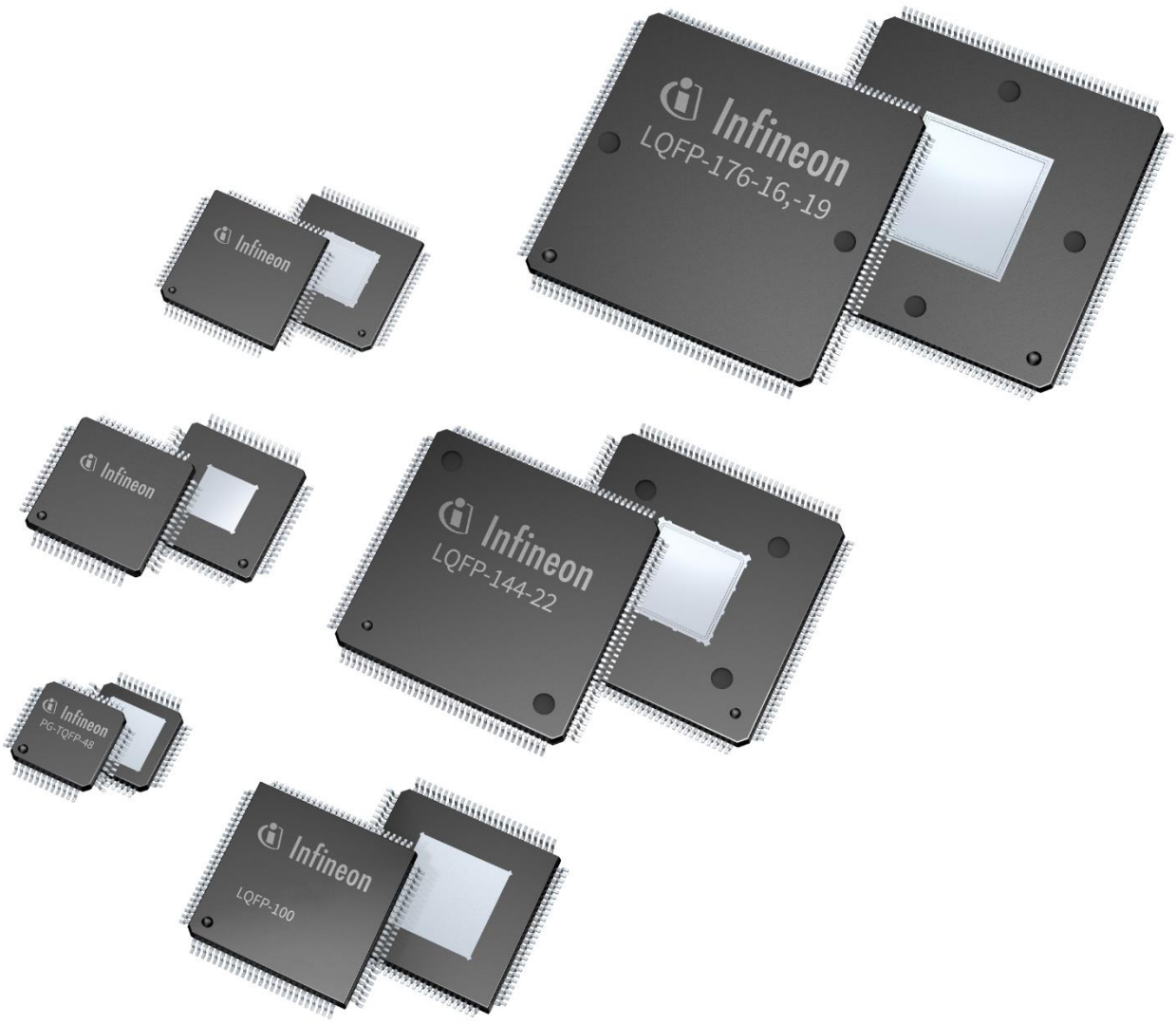
Recommendations for Board Assembly of Infineon Quad Flat Packages



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Acronyms and Abbreviations

AOI	Automated Optical Inspection
AXI	Automated X-ray Inspection
ESD	Electrostatic Discharge
IC	Integrated Circuit
I/O	Input/Output
LF	Lead Frame
LQFP	Low-profile Quad Flat Package
MQFP	Metric Quad Flat Packages
MSL	Moisture-Sensitivity Level
Ni/Pd/Au	Nickel/Palladium/Gold
NSMD	Non-Solder Mask Defined pad
PG	Plastic Green
PCB	Printed Circuit Board
PPF	Pre-Plated lead Frame
QFP	Quad-Flat Package
SAC	Tin Silver Copper (SnAgCu)
SMD	Solder Mask Defined
SMD	Surface-Mount Device
SMT	Surface-Mount Technology
Sn	matte tin plating
TQFP	Thin Quad Flat Packages

1 Package Description

This recommendation provides information about the board assembly of Infineon Quad Flat Packages (QFP) by Surface Mount Technology (SMT). The typical gullwing leads are arranged on all four sides of the package mold body. An exposed die pad in the center of the package landing allows for optimum heat transfer and electrical grounding. The reliable setup and high lead count of QFP makes them ideal carriers for microcontroller or gate driver Integrated Circuits (IC).

This document does not discuss other Infineon dual row packages with gullwing leads. These package families are described in a separate document.

1.1 QFP Package Type

Infineon QFP come with different total heights and lead pitches. The typical pitch of Low-profile Quad Flat Packages (LQFP) and Thin Quad Flat Packages (TQFP) is of 0.5 mm. The latter also provides a pitch down to 0.4 mm. Metric Quad Flat Packages (MQFP) have a typical pitch of 0.65 mm up to 0.8 mm. **Figure 1** shows representatives of the QFP package families.

- PG-LQFP
- PG-MQFP
- PG-TQFP

PG = Plastic Green
L = Low-profile
M = Metric
T = Thin
QFP = Quad Flat Package

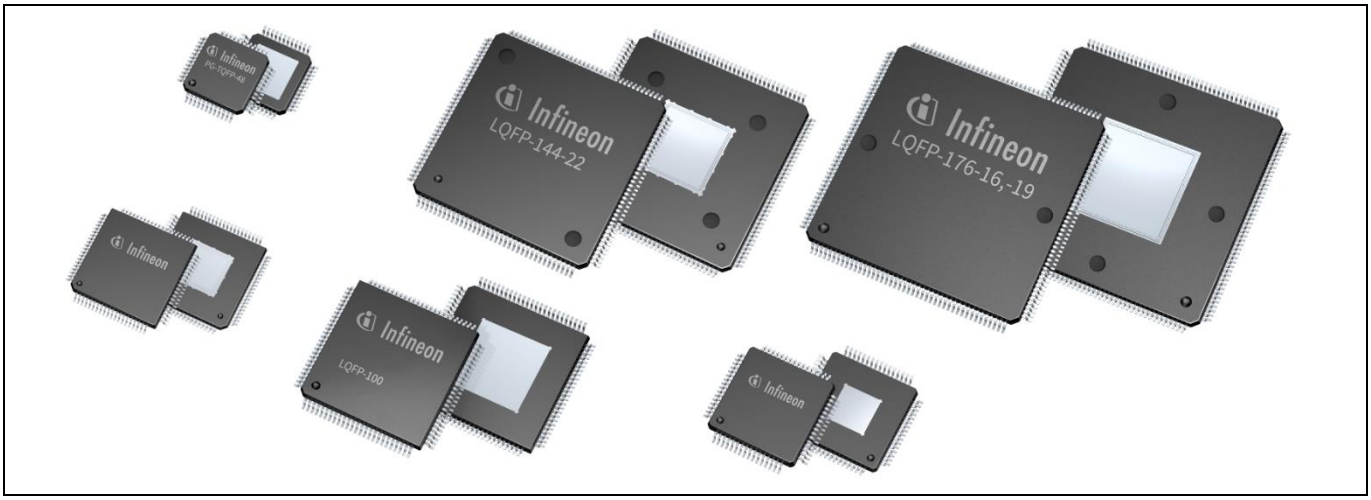

Figure 1 Examples of QFP packages.

1.2 Package Features and General Handling Guidelines

General Handling Guidelines

Semiconductor devices are sensitive to excessive electrostatic discharge (ESD), certain moisture levels, mechanical handling, and contamination. Therefore, they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing.

For further information about component handling, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Package Description

Internal Construction

Infineon QFP are plastic encapsulated lead frame packages. Most of them have an exposed die pad on the bottom of the package, which is created by an appropriate lead frame down-set. The exposed pads are usually soldered to the Printed Circuit Board (PCB) for mechanical, electrical and thermal connection. **Figure 2** shows the typical setup of QFP with and without exposed die pad.

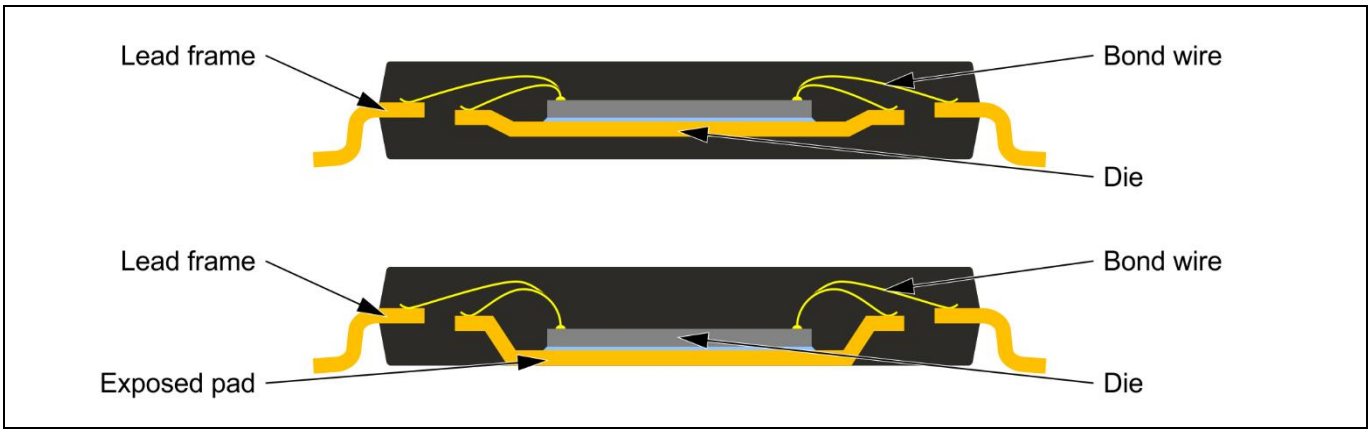

Figure 2 Schematics showing the inner setup of a QFP without (top) and with exposed die pad (bottom).

Termination Design

The gullwing lead is considered to be one of the most reliable terminations for Surface-Mount Devices (SMD). To form gullwing terminations, the leads are bent outwards at the tip. These bent Input/Output (I/O) lead foot and heel areas form the seating plane that is then soldered to the PCB.

The distance between the I/O lead seating plane and the exposed pad landing area at the package bottom is defined as the package stand-off. On QFP it can vary around the nominal value of 100 µm by ±50 µm. Consequences to the board assembly are discussed in the following sections.

Termination Plating

Infineon QFP are available with matte tin (Sn) surface finish or with a Pre-Plated lead Frame (PPF). While the Sn-plating is applied to the base metal by a post-mold process, the PPF provides a solderable surface that is already deposited on the lead frame prior to the die attach process. The PPF surfaces basically consist of a nickel/palladium/gold (Ni/Pd/Au) stack-up. While the Sn melts during reflow, the sacrificial Au layer of the PPF surface is dissolved. The solder connection is then made with the Ni layer.

Figure 3 shows cross-sections of gullwing leads with Sn plated and PPF surface. While the appearance of solder wetted PPF surfaces is slightly different to Sn surfaces it is in full agreement with IPC-A-610 standard [6]. Images of the outer solder joint appearance can be found in **Figure 8**.

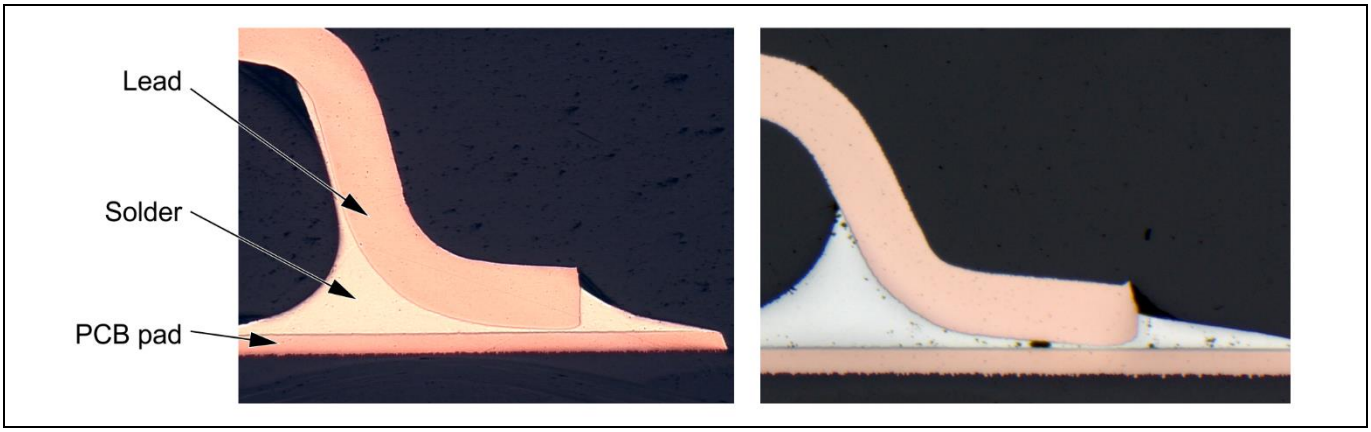

Figure 3 Soldered gullwing leads with post-mold plated Sn (left) and with pre-plated Ni/Pd/Au (right).

For further information about the specific component configuration, please contact your local Infineon sales, application, or quality engineer.

2 Printed Circuit Board

2.1 Routing

Printed circuit board design and construction are key factors for achieving solder joints with high reliability. Packages with exposed pads should not be placed opposite to each other on either side of a PCB when doing double-sided mounting. This will stiffen the assembly and cause solder joints to fatigue earlier than in a design in which the components are offset. Furthermore, the board stiffness itself has a significant influence on the reliability of the solder joint interconnect if the system is used in critical temperature-cycling conditions.

2.2 Pad Design

The quality and reliability of interconnect solder joints to the board are affected by:

- Pad type (Solder-Mask Defined, SMD or Non-Solder-Mask Defined, NSMD)
- Specific pad dimensions
- Pad finish (also called metallization or final finish)
- Via layout and technology

The NSMD pad design is recommended for QFP components. The approach applies to the peripheral terminations as well as to the exposed pads. Mixing different pad definition types in one footprint is not recommended.

The exposed pads of QFP can feature anti-flash profiles. These are meander structures at the outline of the pad to taper off potential mold flash during fabrication process. In **Figure 4** such an anti-flash profile is shown. Despite that structure, the exposed pad outline is used for soldering purpose as can be seen in **Figure 5**.

Besides their electrical function, the exposed pad areas of QFP packages are designed to conduct high thermal loads into the PCB in order to achieve an optimal thermal performance. Therefore, the exposed pad area on the PCB should be congruent with the area on the package at minimum. Using a PCB pad of the same size as the package exposed pad will also increase the solder joint reliability, and the electrical performance for some applications. **Figure 5** shows an example of print pattern on a PCB pad for a die pad connection including thermal vias.

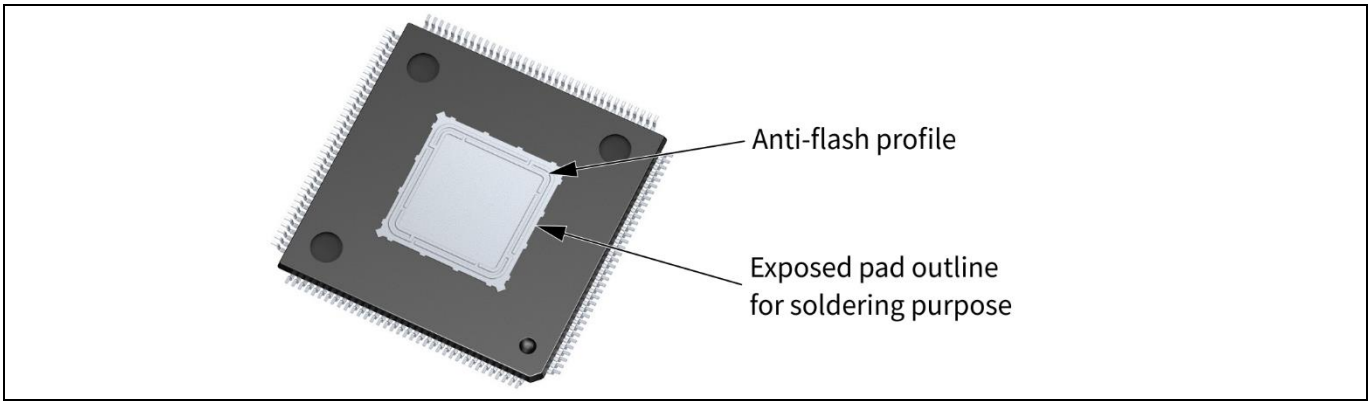

Figure 4 QFP with anti-flash profile in the exposed pad. The outer extension of the exposed pad including the anti-flash profile should be used as the reference for the PCB pad design.

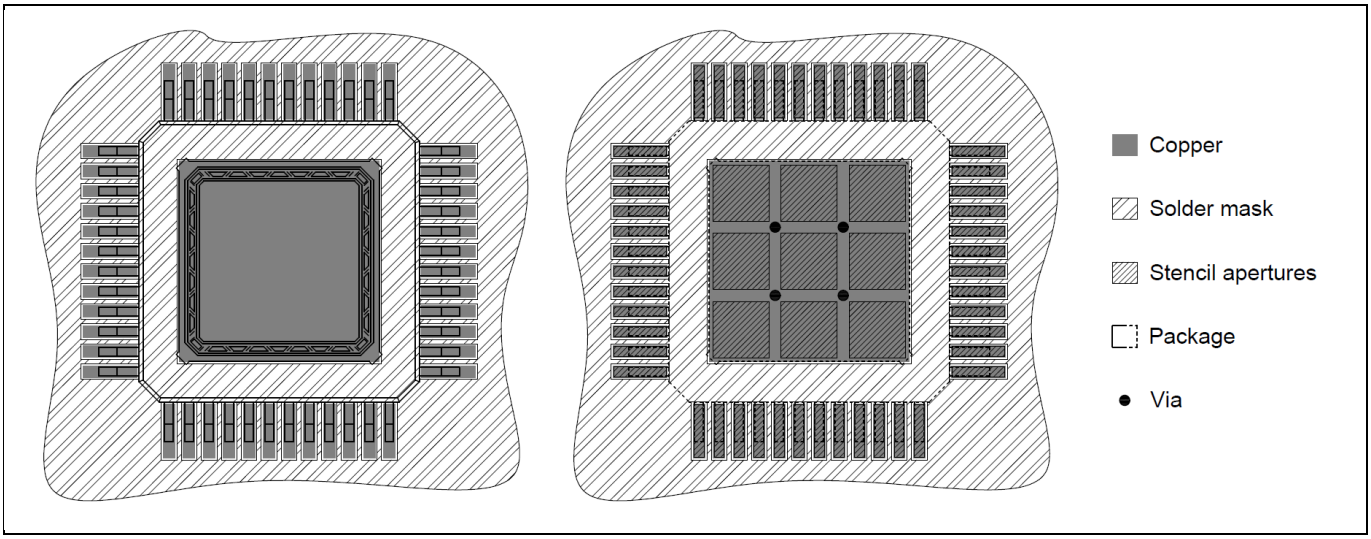

Figure 5 **Example of a pads and stencil design for QFP. The outer extension of the exposed pad including the anti-flash profile is used as the reference for the PCB pad (left). Potential vias-in-pad should be placed in between the stencil apertures to avoid solder flowing into the vias (right).**

Figure 6 shows schematic depictions of the backward PCB pad extension at the gullwing lead heel that is necessary for an optimal solder fillet formation. According to the IPC-A-610 the minimum solder wetting height shall reach an extended line projected from the lead tip top corner in parallel to the PCB pad plane [6]. As a rule of thumb often the line parallel to the lead top plane is used to take into account the lower bend angle.

The PCB pad and therefore the solder paste print should have a distinct distance to the package mold in order to avoid an unclean solder process as it is induced by e.g. solder spatters.

Generally, an optimal PCB design depends on the specific application as well as on the specific design rules of the chosen board manufacturer.

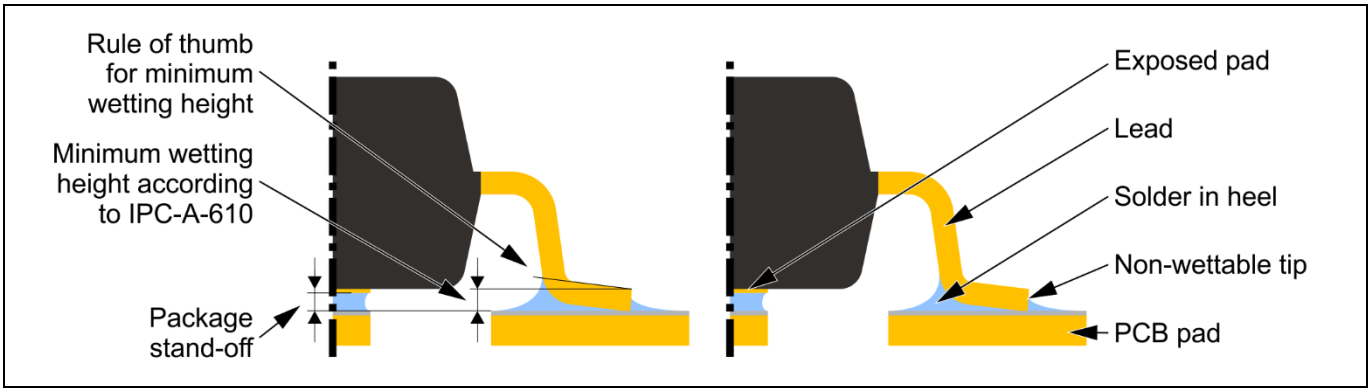

Figure 6 **Schematic depiction of a QFP mounted on a PCB. There are two critical parameters to consider. First is the package stand-off between the landing plane of the exposed pad and the copper plane of the PCB. The second is the pad extension for optimal solder fillet formation at the gullwing heel according to the IPC-A-610 [6].**

For further information about PCB pad design, please refer to the *General Recommendations for Borad Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

Further details and specific footprint recommendations can be found in Infineon package data that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show you an example of the stencil aperture layout for each package.

2.3 Via-in-Pad Design

Thermal and electrical connections to the inner and/or bottom copper planes of the PCB are usually created by plated through-hole vias in the board. The heat is then transferred from the chip over the package die pad and the solder joint to the thermal pad on the board and further through the PCB by the thermal vias.

The diameter and the number of vias in the thermal pad depend on the specific thermal requirements of the final product, the power consumption of the product, the application, and the construction of the PCB. A typical hole diameter for thermal vias is 0.2 - 0.5 mm. An array with 1.0 - 1.2 mm pitch can be a reasonable starting point for further design optimization. The implementation of thermal vias has several impacts on the board assembly as outlined below. A constant increase of number of vias does not necessarily translate into a constant decrease of the thermal resistance of the entire assembly set-up. Thermal and electrical analysis and/or testing together with a proper board assembly design procedure are recommended to determine the optimum number of vias needed.

One of the primary exposed pad design objectives, besides the thermal management, should be to avoid the penetration of the vias by solder. Consequences of solder penetration can be a decreased stand-off between the PCB and the package, an increased void formation ultimately resulting in an insufficient solder joint area, or surplus solder on the opposite side of the PCB.

A first approach for risk reduction should be the prevention of a direct print of solder paste on the via orifice. Since the stencil for large area prints such as on die pads is usually segmented, it is a good practice to position the vias under the beam intersections of the aperture as shown in **Figure 5**. With such an approach, a good solder joint on a central die pad can be formed using vias that remain open on both sides of the board.

Despite the precautionary stencil design approach, the solder can move into the via, driven by the wetting forces. If the solder then protrudes to the opposite side of the PCB, it may interfere with a second solder paste print process. To minimize the effect, dummy areas on the opposite side as shown in **Figure 7** can catch the surplus solder to avoid beading and solder lumping.

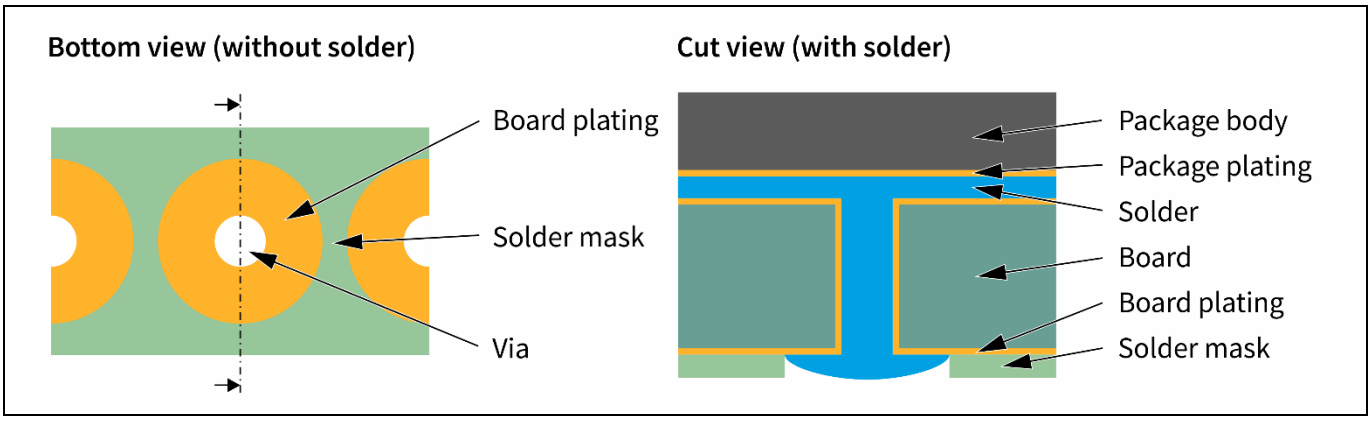

Figure 7 Wettable “dummy” area on the opposite side of the board surrounds the vias to act as a buffer for surplus solder.

In case the solder variance in volume below the die pad is too high due to the wetting of vias, they can be closed by “tenting.” This process includes covering the vias by a solder mask (e.g. dry-film solder mask). If the via tenting is done only on the opposite side of the board, the voiding rate will increase significantly. Another method to close vias is called “plugging” (filling with epoxy), followed by overplating. Very small vias (100 µm in

diameter or smaller) should be filled with copper and be overplated. In both cases, the specification of a planar filling is necessary to avoid cavities that will trap gases, forming voids during reflow soldering.

In case it is not necessary to provide a direct connection from the solder pad under the exposed die pad to the inner layers of the PCB, the vias can be placed next to the footprint near the package and covered with solder mask.

For further information about vias in pad, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3 PCB Assembly

3.1 Solder Paste Stencil

In SMT the solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. While an excessive solder paste volume will cause solder bridging, an insufficient solder paste volume can lead to reduced solder spreading between all contact surfaces. To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut stencils (mostly made from stainless steel) are preferred.

The stencil apertures are usually of the same dimensions as the relevant pad on the PCB. In most cases, the thickness of a stencil has to be matched to the needs of all components on the PCB. For typical QFP with pitch 0.5 mm, stencils 130 µm to 150 µm (5 to 6 mil) thick are recommended. QFP with pitch 0.4 mm should be printed with a maximum stencil thickness of 130 µm (5mil).

The solder paste volume in apertures larger than approximately 5 mm may be scooped out depending on the specific squeegee pressure and rigidity. Such apertures necessary for many exposed pad prints, should be segmented into smaller areas.

When reducing the die pad print the stand-off between gullwing landing area and exposed pad plane has to be considered. The QFP stand-off can vary around the nominal value of 100 µm by ±50 µm. Therefore, the recommended reduction of approx. 70% to 80% is lower compared with e.g. some leadless packages, where pins and pads are in one plane. When choosing the print pattern and reduction, also the volume and height, provided by the solder stencil thickness has to be considered. Areas on the pad, which are not covered by the print, are preferred positions for vias as shown in **Figure 5**.

For individual design adaptations to reach the optimum amount of solder, the stencil thickness, the PCB pad finish, solder mask quality, the via layout, and the solder paste type should be considered. In every case, application-specific experiments are recommended.

Further details and specific stencil aperture recommendations can be found in the package data base that is available on the Infineon web page [1]. Please choose a specific package when searching the data base, which will then show an example of the stencil aperture layout for each package.

For further information about solder stencil design, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.2 Solder Paste

Pb-free solder pastes typically contain some type of SnAgCu alloy (SAC solder with typically 1-4% Ag and <1% Cu). The most common alloy is SAC305 (3.0% Ag and 0.5% Cu). The average alloy particle size must be suitable for printing the solder stencil aperture dimensions. Using Type 4 paste is recommended for the assembly of QFP. The decision for lower type numbers and therefore higher grain sizes should depend on the specific stencil aperture size and therefore solder paste transfer efficiency.

The solder alloy particles are dispersed in a blend of liquid flux and chemical additives (approx. 50% by volume or 10% by weight), forming a creamy paste. The flux and chemical solvents have various functions such as adjusting the viscosity of the paste for stencil printing or removing contaminants and oxides on the surface.

The solder paste solvents have to evaporate during reflow soldering, while residues of the flux will remain on the joint. The capacity of the flux additive for removing oxides is given by its activation level, which also affects the potential need for removing the flux residuals after the assembly. Generally, “no-clean” paste is recommended to avoid subsequent cleaning steps underneath the package. The small gaps can make cleaning

highly difficult. Certain precautions have to be taken if any kinds of flux residues remain on the board prior to any kind of coating. For power packages, leakage currents and the potential for shorting below components have to be considered when choosing the specific flux type (e.g. halide-free vs. zero halides).

Generally, solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.3 Component Placement

Although the self-alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints, the components have to be placed accurately depending on their geometry. Positioning the packages manually is not recommended, especially for packages with small terminations and pitch. An automated pick-and-place machine is recommended to obtain reliable solder joints.

Component placement accuracies of +/-50 µm and less are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or at additional individual mounting positions (local fiducials). These fiducials are detected by a vision system immediately prior to the mounting process.

For further information about component placement, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

3.4 Reflow Soldering

For PCB assembly of QFP components, the widely used method of reflow soldering in a forced convection oven is recommended. Soldering in a nitrogen atmosphere can generally improve the solder joint quality but is not necessary to create a reliable joint.

The soldering profile should be in accordance with the recommendations of the solder paste manufacturer to achieve optimal solder joint quality. The position and the surrounding of the component on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly. Power packages where leakage currents and shorting below the component have to be considered should be soldered with decreased flux spreading. Therefore, it is recommended to optimize the reflow profile in such a way that excessive flux or solder spattering is avoided.

Minimum Reflow Conditions

The lower temperatures and durations of an optimal reflow profile must stay above those of the solderability qualification. The solderability of the terminations of Infineon components is tested according to the standards IEC 60068-2-58 and J-STD-002 [2][3].

Maximum Reflow Conditions and Cycles

Components that are Moisture-Sensitivity Level (MSL) classified by Infineon have been tested by three reflow runs in accordance with the J-STD-020 standard, covering a double-sided reflow and one rework cycle. The maximum temperatures must not be exceeded during board assembly. Please refer to the product barcode label on the packing material that states this maximum reflow temperature according to the J-STD-020 [4] standard as well as the MSL according to the J-STD-033 standard [5].

Typical Infineon QFP are generally suited for mounting on double-sided PCBs. Solder joints of components on the first PCB side will again reflow in the second step. In the reflow zone of the oven (i.e. where the solder is liquid), the components are only held in place by the wetting forces from the molten solder. Gravity acting in

the opposite direction will elongate the solder joints, unlike joints on the top side, where gravity will force the components closer to the PCB surface. This shape will be frozen during cooling and therefore will result in a higher stand-off on the bottom side after the reflow process. Heavy vibrations in a reflow oven may cause devices to drop off the PCB.

For further information about reflow soldering, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

4 Cleaning

After the soldering process, some flux residues may remain on the board, especially near the solder joints. Generally, cleaning beneath a SMT component is difficult due to the small gap between the component body and the PCB. Therefore, a “no-clean” flux is recommended whose residues usually do not have to be removed after the soldering process.

In case the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and cleaning solution have to be selected while taking into account the type of package, the flux used in the solder paste (rosin/resin-based, water-soluble, etc.) as well as the environmental and safety aspects. Even small residues of the cleaning solution should be removed or dried out very thoroughly. For recommended cleaning solutions, please contact the solder paste or flux manufacturer.

5 Inspection

5.1 Optical Solder Joint Inspection

The visual inspection of the solder joints at the gullwing-shaped QFP leads with conventional Automated Optical Inspection (AOI) systems is a standard procedure. **Figure 8** shows optical images of two properly soldered QFP with either having Sn plating or a PPF. As can be seen, the gullwing leads with PPF surface can appear different on their top side from those with Sn plating because the Ni/Au surface does not melt together with the solder during reflow. According to IPC-A-610 the top side of a gullwing lead is not taking part in the solder joint formation [6]. Irrespective of the specific geometry of a gullwing lead the solder joint is generally considered to be of good quality when the heel region is wetted up to a certain height and the sidewall is sufficiently covered. The tips of the leads have bare copper (e.g. cut edges) that is not intended to wet by design according to the IPC-A-610 [6].

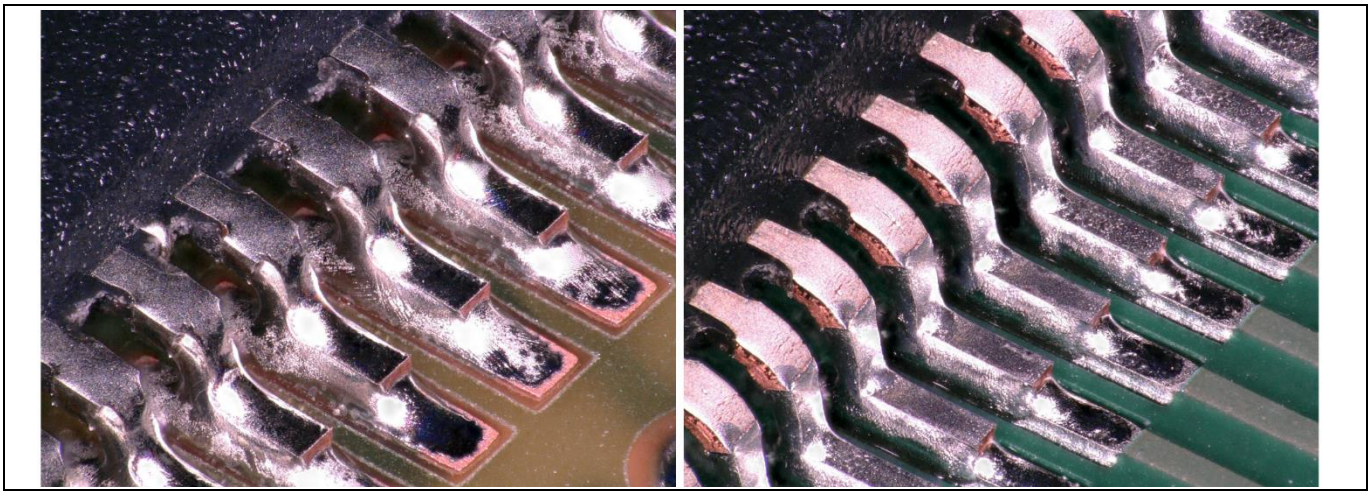

Figure 8 Optical images of QFP with Sn plated gullwing leads (left) and with PPF surface (right). In the latter example, the top side of the leads does appear different because the plating does not melt together with the solder during reflow.

For engineering tasks, cross-sectioning can offer detailed information about the solder joint quality. Due to its destructive character, cross-sectioning during monitoring is naturally not practical.

For further information about the acceptability of electronic assemblies inspected optically, please also refer to the IPC-A-610 standard [6].

5.2 X-Ray Solder Joint Inspection

Automated X-ray Inspection (AXI) systems are appropriate for efficient inline control of component parts that cannot be inspected properly by optical systems (such as exposed pads). AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analyzing, and data transferring routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray.

Figure 9 shows a typical X-ray photograph of a QFP component. The internal lead frame, as well as the wire bonds, and the solder joints that connect the package to the PCB are visible. Large exposed pads may tend to increase voiding because they do not provide a sufficient ratio between volume and surface necessary for proper outgassing of the organic compounds during reflow. Generally, the extent of voiding depends on the

board pad size, the via and stencil layout, the solder paste, and the reflow profile. For thermal evaluations, the entire thermal path must be considered as well as all boundary conditions such as the application environment or the electrical use of the component.

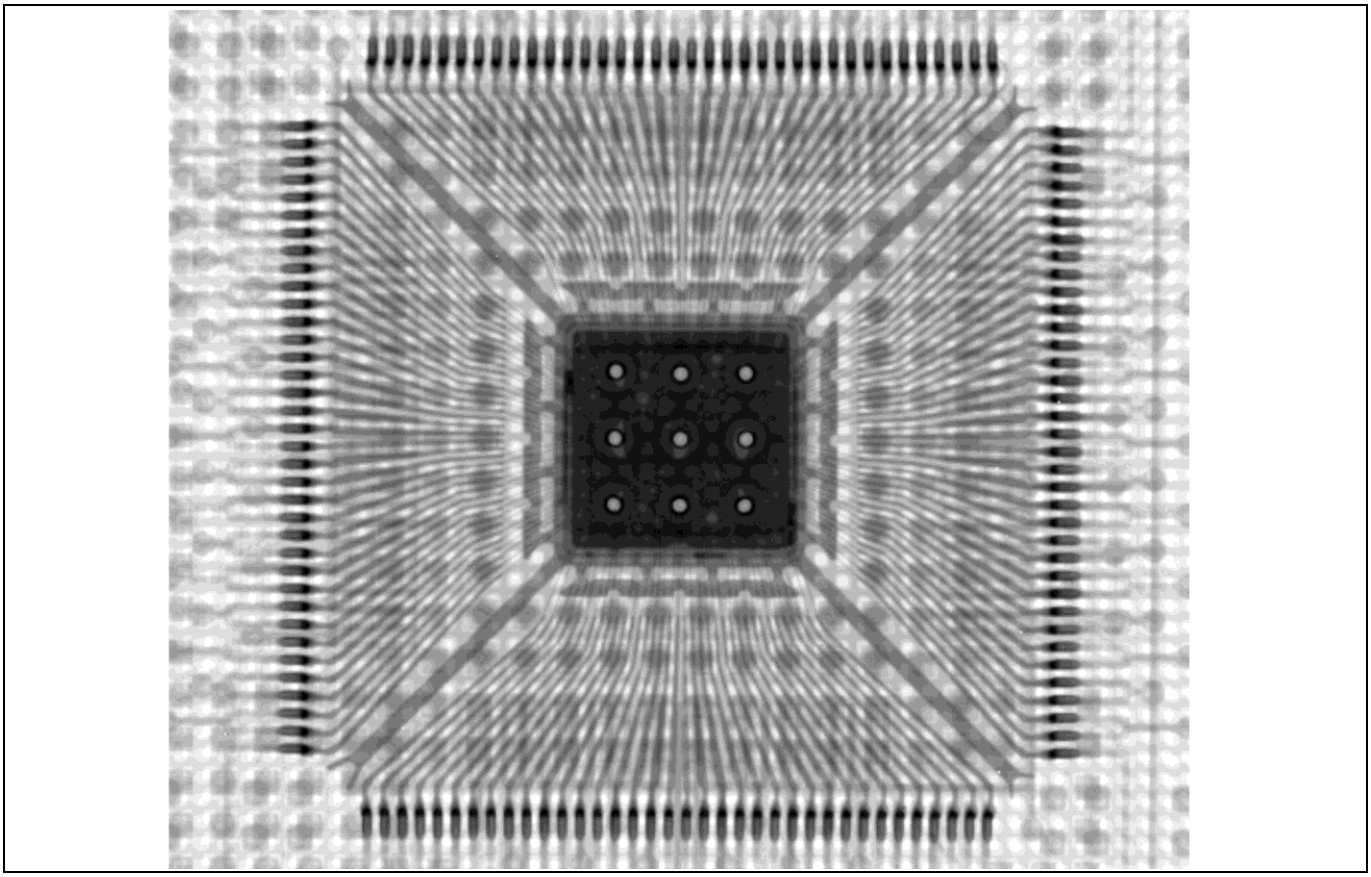

Figure 9 **X-ray photograph of a properly soldered QFP. The I/O lead solder joints as well as the exposed pad solder joint including vias-in-pad are visible.**

6 Rework

QFP components are in general reworkable. Single solder joint repair of small pitch terminated packages can, however, be very difficult and is not recommended. The reuse of completely de-soldered components is not recommended. The de-soldered components should be replaced by new ones.

A rework process is commonly done on special rework equipment. There are various systems available that meet the requirements for reworking SMD packages. All handling guidelines discussed in this document have to be respected. Special focus should be on the following items:

- Due to the decreased automation level given by the general rework approach, even higher care compared to standard assembly must be taken. Tools that do not damage the component mechanically have to be chosen. Mechanical forces that do not necessarily cause visible external damage can still cause internal damage that reduces the component's reliability. A proper handling system with vacuum nozzle may be the gentlest process and is therefore recommended. However, the impact of rework tools has to be assessed properly. In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es).
- During rework, special care must be taken concerning the proper moisture level of the component according to the J-STD-033. Drying the PCB and the component prior to rework might be necessary. A proper drying procedure for SMD packages is described in the international J-STD-033 standard [5]. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), the applied temperature profile at the component must never exceed the maximum temperature according to the J-STD-020 standard. Depending on the specific heating profile used during rework, components adjacent to the mounting location might also experience a further "reflow run" in terms of the J-STD-020 standard [4]. Internal investigations have shown that the temperature profile must be recorded.

If a device is suspected to be defective and a failure analysis is planned, Infineon usually expects customers to desolder the component prior to return to Infineon. The component shall be returned in a proper condition according to the original package outlines.

In some special cases such as solder joint inspection Infineon may request that the PCB or part of the PCB with the component still attached should be sent to Infineon.

Note: *Before returning a device for failure analysis at Infineon, please clarify the return condition of the suspected component (ie onboard or desoldered) with the Infineon Application Engineer or Customer Quality Manager who supports your company.*

For further information about component rework on PCB, please refer to the *General Recommendations for Board Assembly of Infineon Packages* document that is available on the Infineon web page [1]. Please also feel free to contact your local sales, application, or quality engineer.

7 References

[1] Infineon: Packages. www.infineon.com\packages.

[2] International Electrotechnical Commission: IEC 60068-2-58. Environmental testing - Part 2-58: Tests - Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD).

[3] Electronic Components Industry Association, Assembly and Joining Processes and JEDEC Solid State Technology Association Committee: EIA/IPC/JEDEC J-STD-002. Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.

[4] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-020. Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices.

[5] JEDEC Solid State Technology Association: IPC/JEDEC J-STD-033. Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.

[6] Association Connecting Electronics Industries: IPC-A-610. Acceptability of Electronic Assemblies.

Revision History

Page or reference	Major changes since the last revision
Section 6 “Rework”	Update of sample conditions in case of return.
Entire document	Editorial review.

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