Infineon Power Solutions for Xilinx

Zynq UltraScale+ MPSoC

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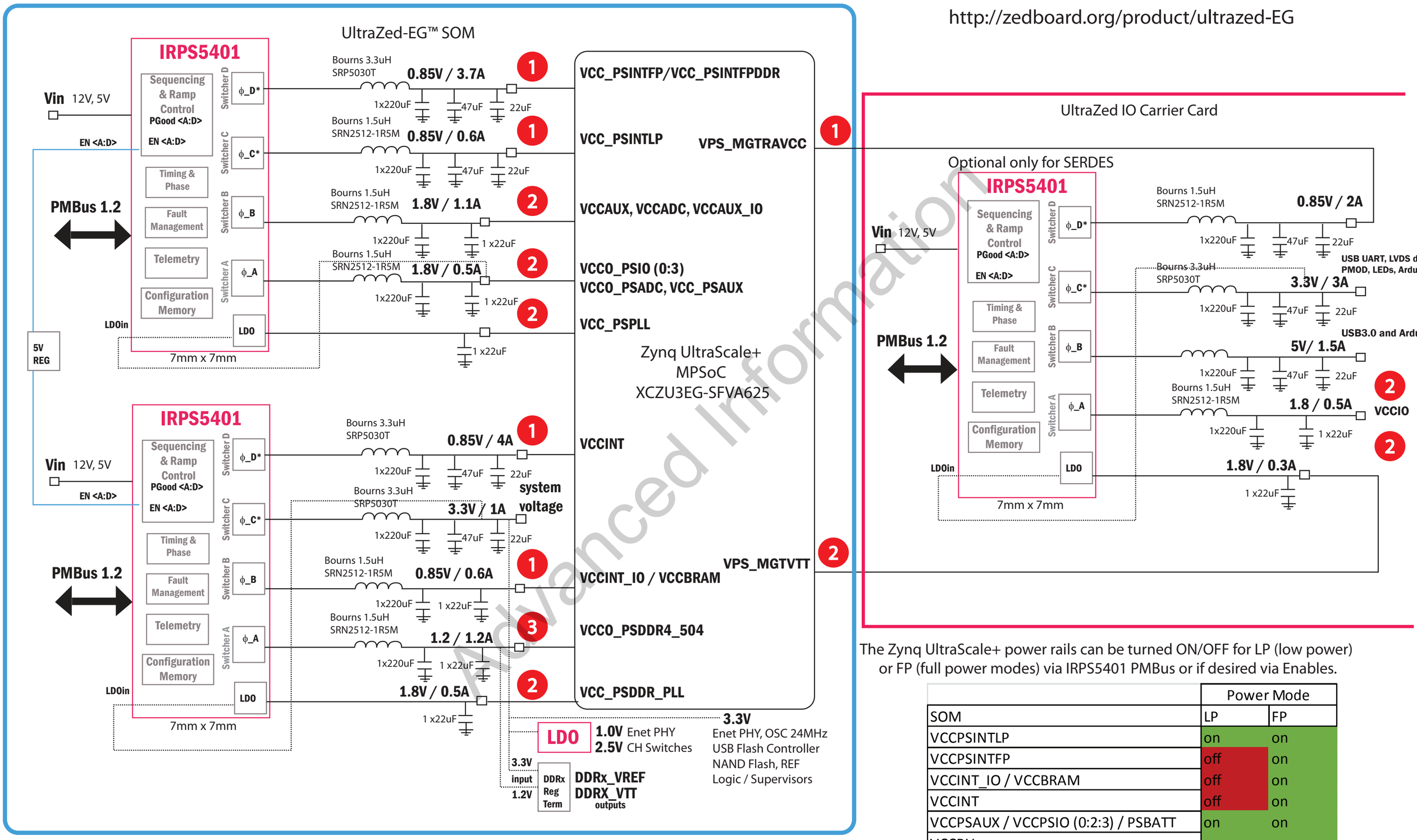
Introduction

- Infineon power solutions focusing on tight board space applications
- Featuring 5 output PMIC, IRPS5401
- Power solutions for Xilinx Zynq Ultrascale+ MPSoC from Zu02 to Zu19
- Power maps are optimized for power rail consolidation
- Sequencing for power up and power down shown with delay estimates
- Infineon power solutions provide scalable power for core voltage vs. Zynq Ultrascale+ MPSoC family
- PCB board size estimates provided. Usually the size estimate provide fits the largest power stage and Cout
- Estimated values for inductors and output capacitors based upon Xilinx DC, AC and voltage ripple requirements
- IRPS5401 digital compensation values calculated for Xilinx power requirements vs. L vs. C.

Infineon Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu03_Zu02
Flexible Mode: Always on - Cost Optimized
Always on - Efficiency Optimized, and Full Power / Low Power Mode Capable

http://zedboard.org/product/ultrazed-EG



The Zynq UltraScale+ power rails can be turned ON/OFF for LP (low power) or FP (full power modes) via IRPS5401 PMBus or if desired via Enables.

	Power Mode	
SOM	LP	FP
VCCPSINTLP	on	on
VCCPSINTFP	off	on
VCCINT_IO / VCCBRAM	off	on
VCCINT	off	on
VCCPSAUX / VCCPSIO (0:2:3) / PSBATT	on	on
VCCPLL	on	on
VCCDDR / VCCO / DDR4 devices	off	on
VCCAUX / AUX_IO / VCCO / ENET PHY	off	on
VCCO	off	on
VCCO / ENET PHY	off	on
VTERM	off	on
ENET PHY	off	on

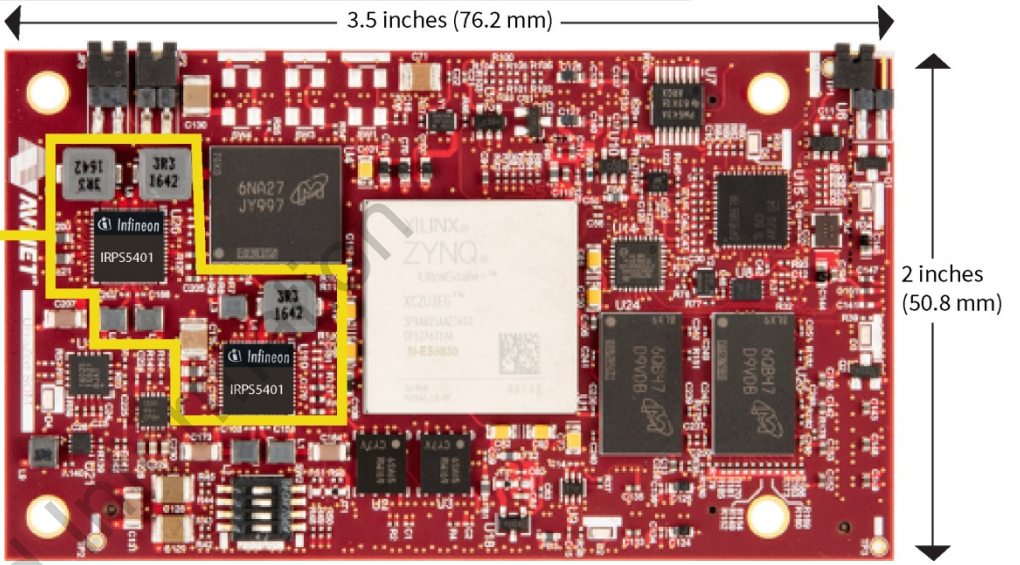
Power sequencing initiated by 5V Enable/Disabled to all IRPS5401's
All regulators and LDO is turned on/off via
internal settable timers integrated
into the IRPS5401 PMICs.
No external sequencing components are required.
Power Off is the reverse order.

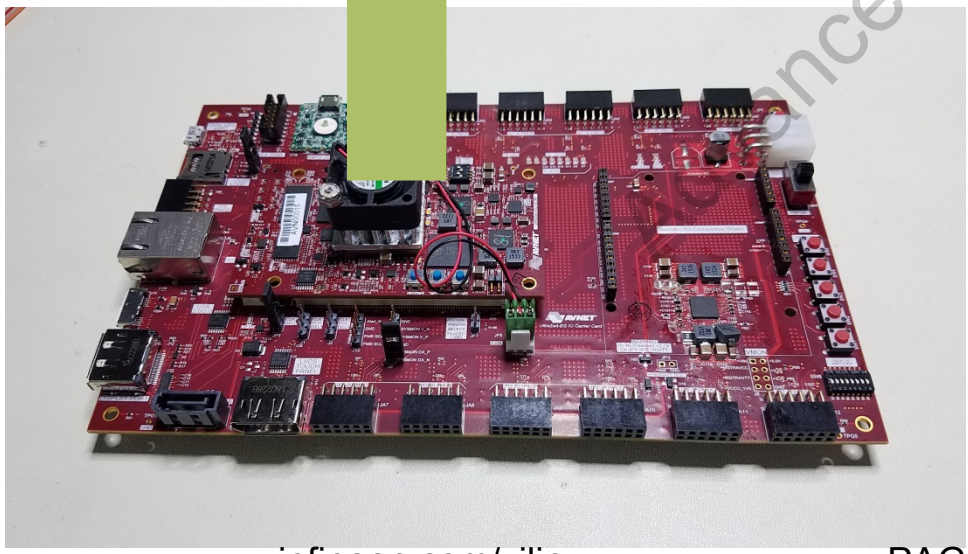
www.infineon.com/xilinx

Reference Design Example:

Zynq MPSoC Ultrascale+, Zu02/Zu03

http://zedboard.org/product/ultrazed-EG





DESIGN NOTES

1) 3 x IRPS5401 5 output PMICs
   PMBus Capable. 15 outputs.

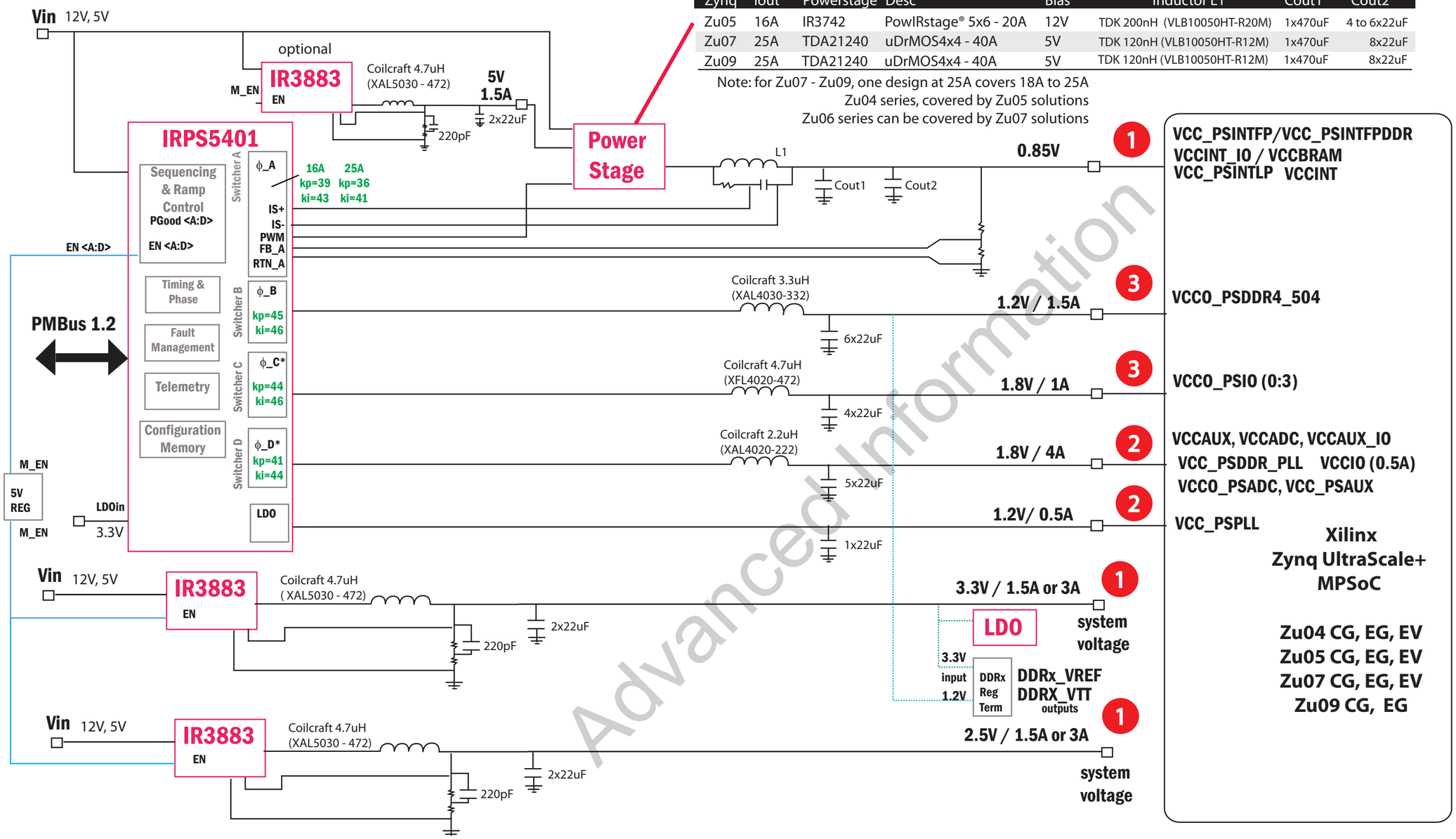
2) Zynq Ultra Scale SOM & Carrier Card

Lower current Zynq Ultra Scale+ Series examples: ZUEG2, ZEUG3

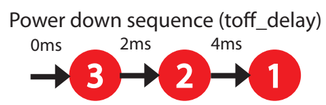
Infineon Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu04_Zu05_Zu07_Zu09 CG, EG, EV Series - No SERDES
Always On: Cost-Optimized Power Rail Consolidation

Zynq	Iout	Powerstage	Desc	Bias	Inductor L1	Cout1	Cout2
Zu05	16A	IR3742	PowIRstage® 5x6 - 20A	12V	TDK 200nH (VLB10050HT-R20M)	1x470uF	4 to 6x22uF
Zu07	25A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 120nH (VLB10050HT-R12M)	1x470uF	8x22uF
Zu09	25A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 120nH (VLB10050HT-R12M)	1x470uF	8x22uF

Note: for Zu07 - Zu09, one design at 25A covers 18A to 25A
Zu04 series, covered by Zu05 solutions
Zu06 series can be covered by Zu07 solutions



On start up condition of VCC and PVin and an external master enable (M_EN), Power sequencing can be adjusted by ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.



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internal settable timers integrated
into the IRPS5401 PMICs.
No external sequencing components are required.
Power Off is the reverse order.

The IRPS5401 regulators do not require external loop compensation components.
The digital compensation kp, ki listed are estimations for the target regulation and may require adjustment.

PCB space estimates:
IRPS5401 with Power Stage + L's, C's : 35mm x 40mm
IRPS5401 without Power Stage + L's, C's: 30mm x 30mm
IR3883 with L, C's : 15mm x 10mm

Infineon Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu04_Zu05_Zu07_Zu09 CG EG EV Series - with SERDES
Always On: Cost-Optimized Power Rail Consolidation

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Zu07	25A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 120nH (VLB10050HT-R12M)	1x470uF	8x22uF
Zu09	25A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 120nH (VLB10050HT-R12M)	1x470uF	8x22uF

Note: for Zu07 - Zu09, one design at 25A covers 18A to 25A
Zu04 series, covered by Zu05 solutions
Zu06 series can be covered by Zu07 solutions

Vin 12V, 5V

optional

IR3883
M_EN
EN
Coilcraft 4.7uH (XAL5030 - 472)
5V 1.5A
2x22uF
220pF

IRPS5401
Sequencing & Ramp Control
PGood <A:D>
EN <A:D>
Timing & Phase
Fault Management
Telemetry
Configuration Memory
Switcher A: ϕ_A — 16A kp=39 ki=43 — 25A kp=36 ki=41; IS+, IS-, PWM, FB_A, RTN_A
Switcher B: ϕ_B kp=45 ki=46
Switcher C: ϕ_C* kp=44 ki=46
Switcher D: ϕ_D* kp=41 ki=44
LDO

EN <A:D>
PMBus 1.2
M_EN
5V REG
LDOin
M_EN
3.3V
1.8V

Power Stage

L1
Cout1
Cout2

1 — 0.85V / 0.9V
VCC_PSINTFP/VCC_PSINTFPDDR
VCCINT_IO / VCCBRAM
VCC_PSINTLP VCCINT

Coilcraft 3.3uH (XAL4030-332)
6x22uF
3 — 1.2V / 1.5A
VCCO_PSDDR4_504

Coilcraft 4.7uH (XFL4020-472)
4x22uF
3 — 1.8V / 1A
VCCO_PSIO (0:3)
VCCAUX, VCCADC, VCCAUX_IO

Coilcraft 2.2uH (XAL4020-222)
5x22uF
2 — 1.8V / 4A
VCC_PSDDR_PLL VCCIO (0.5A)
VCCO_PSADC, VCC_PSAUX
VPS_MGTRAVTT

1x22uF
2 — 1.2V/ 0.5A
VCC_PSPLL

LDO
3.3V input
1.2V
DDRx Reg Term
DDRx_VREF
DDRX_VTT
outputs

Xilinx Zynq UltraScale+ MPSoC

Zu04 CG, EG, EV
Zu05 CG, EG, EV
Zu07 CG, EG, EV
Zu09 CG, EG

+ SERDES

IRPS5401
Sequencing & Ramp Control
PGood <A:D>
EN <A:D>
Timing & Phase
Fault Management
Telemetry
Configuration Memory
Switcher A: ϕ_A kp=46 ki=48; FB_A, RTN_A
Switcher B: ϕ_B kp=42 ki=44
Switcher C: ϕ_C* kp=44 ki=46
Switcher D: ϕ_D* kp=44 ki=45
LDO

Vin 12V, 5V
EN <A:D>
PMBus 1.2
LDOin
3.3V

Coilcraft 4.7uH (XFL4020-472)
4x22uF
scale factor divider
system voltage option
3.3V/ 1A
1

Coilcraft 4.7uH (XFL4020-472)
4x22uF
2.5V / 1A
1

Coilcraft 1.5uH (XAL4020-152)
8 to 10 x22uF
0.9V / 3A
1
VMGATAVCC,
VMGTYAVCC

Coilcraft 1.5uH (XAL4020-152)
8 to 10 x22uF
1.2V / 3A
3
VMGTAVTT, VMGTYAVTT,
VCC_PSPLL, VCC_VCU_PLL

1x22uF
0.85V / 0.4A
2
VPS_MGTRAVCC

system voltage option
(5V, 2.5V, 1V)

On start up condition of VCC and PVin and an external master enable (M_EN),
Power sequencing can be adjusted by
ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.

Power up sequence (ton_delay)
0ms 2ms 4ms
1 → 2 → 3

Power down sequence (toff_delay)
0ms 2ms 4ms
3 → 2 → 1

If the second IRPS5401 is not desired
the below are regulator options for SERDES:

1) IR3891 Dual 1.2V/1.8V or 0.9V/0.85V for VMGATAVCC, and VMGTAVTT
2) IR3823 for any SERDES < 3A

If more 3.3V system voltage and higher current: 1.5A/3A, 3.3V IR3883

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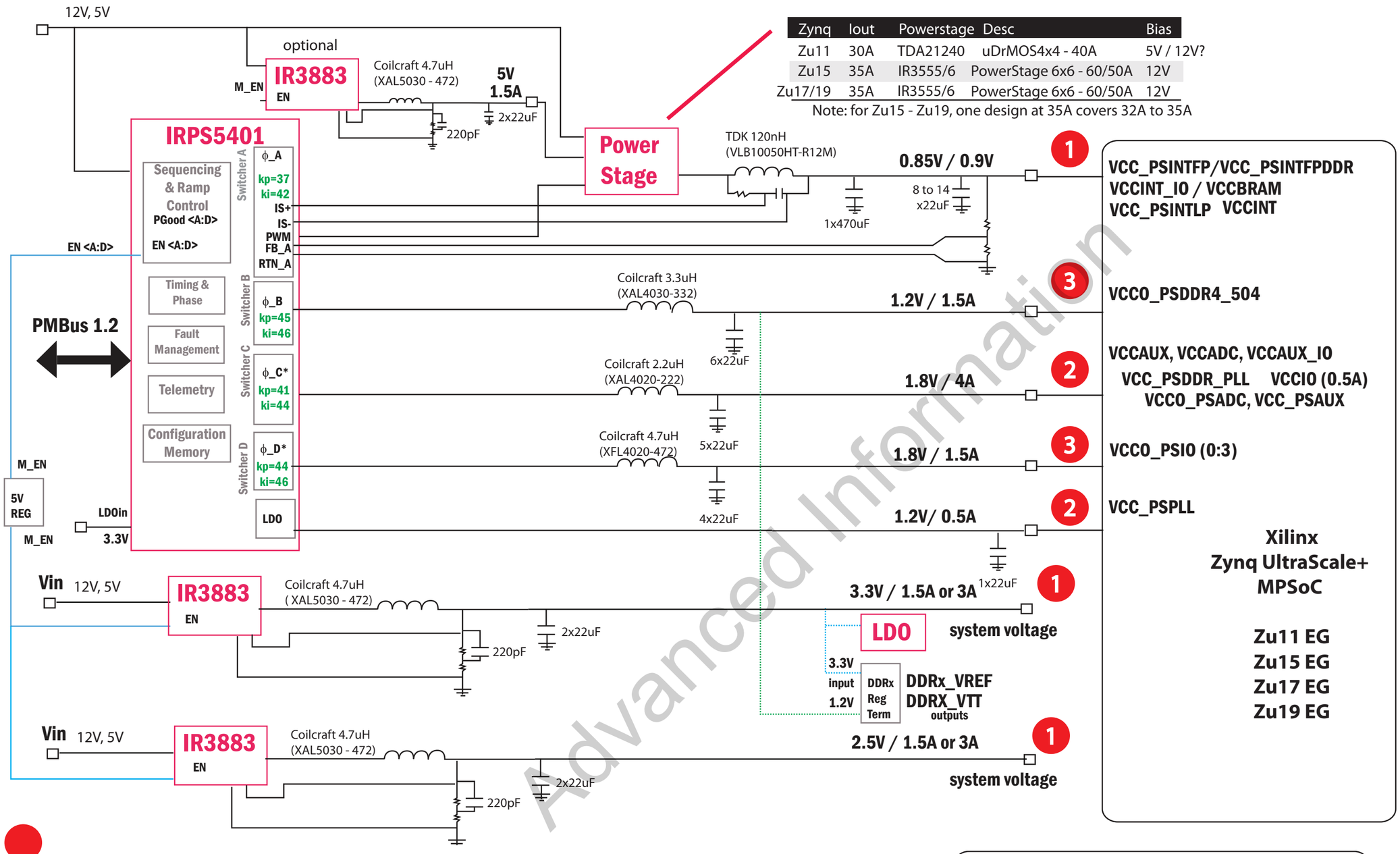
IR3883 with L, C's : 15mm x 10mm

Infineon Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu11_Zu15_Zu17_Zu19 EG Series - No SERDES
Always On: Cost-Optimized Power Rail Consolidation



Zynq	Iout	Powerstage	Desc	Bias
Zu11	30A	TDA21240	uDrMOS4x4 - 40A	5V / 12V?
Zu15	35A	IR3555/6	PowerStage 6x6 - 60/50A	12V
Zu17/19	35A	IR3555/6	PowerStage 6x6 - 60/50A	12V

Note: for Zu15 - Zu19, one design at 35A covers 32A to 35A

On start up condition of VCC and PVin and an external master enable (M_EN), Power sequencing can be adjusted by ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.

Power up sequence (ton_delay)

Power down sequence (toff_delay)

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Zu11_Zu15_Zu17_Zu19 EG Series - with SERDES
Always On: Cost-Optimized Power Rail Consolidation

Zynq	Iout	Powerstage	Desc	Bias
Zu11	30A	TDA21240	uDrMOS4x4 - 40A	5V / 12V?
Zu15	35A	IR3555/6	PowerStage 6x6 - 60/50A	12V
Zu17/19	35A	IR3555/6	PowerStage 6x6 - 60/50A	12V

Note: for Zu15 - Zu17/19, one design at 35A covers 32A to 35A

12V, 5V

optional

IR3883 EN

M_EN

Coilcraft 4.7uH (XAL5030 - 472)

5V 1.5A

2x22uF

220pF

IRPS5401

Sequencing & Ramp Control

PGood <A:D>

EN <A:D>

Timing & Phase

Fault Management

Telemetry

Configuration Memory

PMBus 1.2

Switcher A: ϕ_A kp=37 ki=42; IS+; IS-; PWM; FB_A; RTN_A

Power Stage

TDK 120nH (VLB10050HT-R12M)

0.85V / 0.9V

8 to 14 x22uF

1x470uF

1 VCC_PSINTFP/VCC_PSINTFPDDR
VCCINT_IO / VCCBRAM
VCC_PSINTLP VCCINT

Switcher B: ϕ_B kp=45 ki=46

Coilcraft 3.3uH (XAL4030-332)

1.2V / 1.5A

6x22uF

3 VCCO_PSDDR4_504

Switcher C: ϕ_C* kp=41 ki=44

Coilcraft 2.2uH (XAL4020-222)

1.8V / 4A

5x22uF

2 VCCAUX, VCCADC, VCCAUX_IO
VCCIO (0.5A)
VCCO_PSADC, VCC_PSAUX
VPS_MGTRAVTT

Switcher D: ϕ_D* kp=44 ki=46

Coilcraft 4.7uH (XFL4020-472)

1.8V / 1A

4x22uF

3 VCCO_PSIO (0:3)

LDO

2.5V/ 0.5A

1x22uF

3 USER I/O (1, 1.2, 1.35, 1.5 1.8, 2.5V)

Xilinx Zynq UltraScale+ MPSoC

Zu11 EG
Zu15 EG
Zu17 EG
Zu19 EG
+ SERDES

5V REG

LDOin 3.3V

EN <A:D>

M_EN

IRPS5401

Vin 12V, 5V

system voltage option

Coilcraft 4.7uH (XAL4030-472MEB)

3.3V/ 1.5A

1

4x22uF

scale factor divider

FB_A RTN_A

Switcher B: ϕ_B kp=44 ki=46

Coilcraft 4.7uH (XFL4020-472)

1.8V / 1A

4x22uF

2 VCC_PSDDR_PLL

Switcher C: ϕ_C* kp=44 ki=45

Coilcraft 1.5uH (XAL4020-152)

1.2 / 3A

8 to 10 x22uF

3 VMGTAVTT, VMGTYAVTT,
VCC_PSPLL, VCC_VCU_PLL
for Zu15 (for Zu11/17/19 see below)

Switcher D: ϕ_D* kp=44 ki=46

Coilcraft 1.5uH (XAL4020-152)

0.9V / 3A

8 to 10 x22uF

1 VMGATAVCC,
VMGTYAVCC
for Zu15 (for Zu11/17/19 see below)

LDO

0.85V / 0.4A

1x22uF

2 VPS_MGTRAVCC

LDO

3.3V input 1.2V

DDRx Reg Term

DDRx_VREF
DDRX_VTT
outputs

IR3892

Vin 12V, 5V

3.3V, can it be 5V?

EN2 EN1 SW1 SW2 PG2

1.2 / 5A 3 VMGTAVTT, VMGTYAVTT, VCC_PSPLL, VCC_VCU_PLL

0.9V / 5A 1 VMGATAVCC, VMGTYAVCC

SERDES for Zu11

IR3899 or IR38062

Vin 12V, 5V

M_EN

EN SW PG

0.9V / 8A 1 VMGATAVCC, VMGTYAVCC

SERDES for Zu17/19

IR3894 or IR38062

Vin 12V, 5V

EN SW PG

1.2 / 11A 3 VMGTAVTT, VMGTYAVTT, VCC_PSPLL, VCC_VCU_PLL

On start up condition of VCC and PVin and an external master enable (M_EN), Power sequencing can be adjusted by ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.

Power up sequence (ton_delay)

0ms 2ms 4ms

1 → 2 → 3

Power down sequence (toff_delay)

0ms 2ms 4ms

3 → 2 → 1

PCB space estimates:

IRPS5401 with Power Stage + L's, C's : 35mm x 40mm
IRPS5401 without Power Stage + L's, C's: 30mm x 30mm
IR3883 with L, C's : 15mm x 10mm

IR3892 with L, C's: 20mm x 20 mm

IR3899 or IR3894 with L, C's: 15mm x 20mm

IR38062 with L, C's: 16mm x 21mm

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Zu04_Zu05_Zu07_Zu09 CG EG Series - No SERDES
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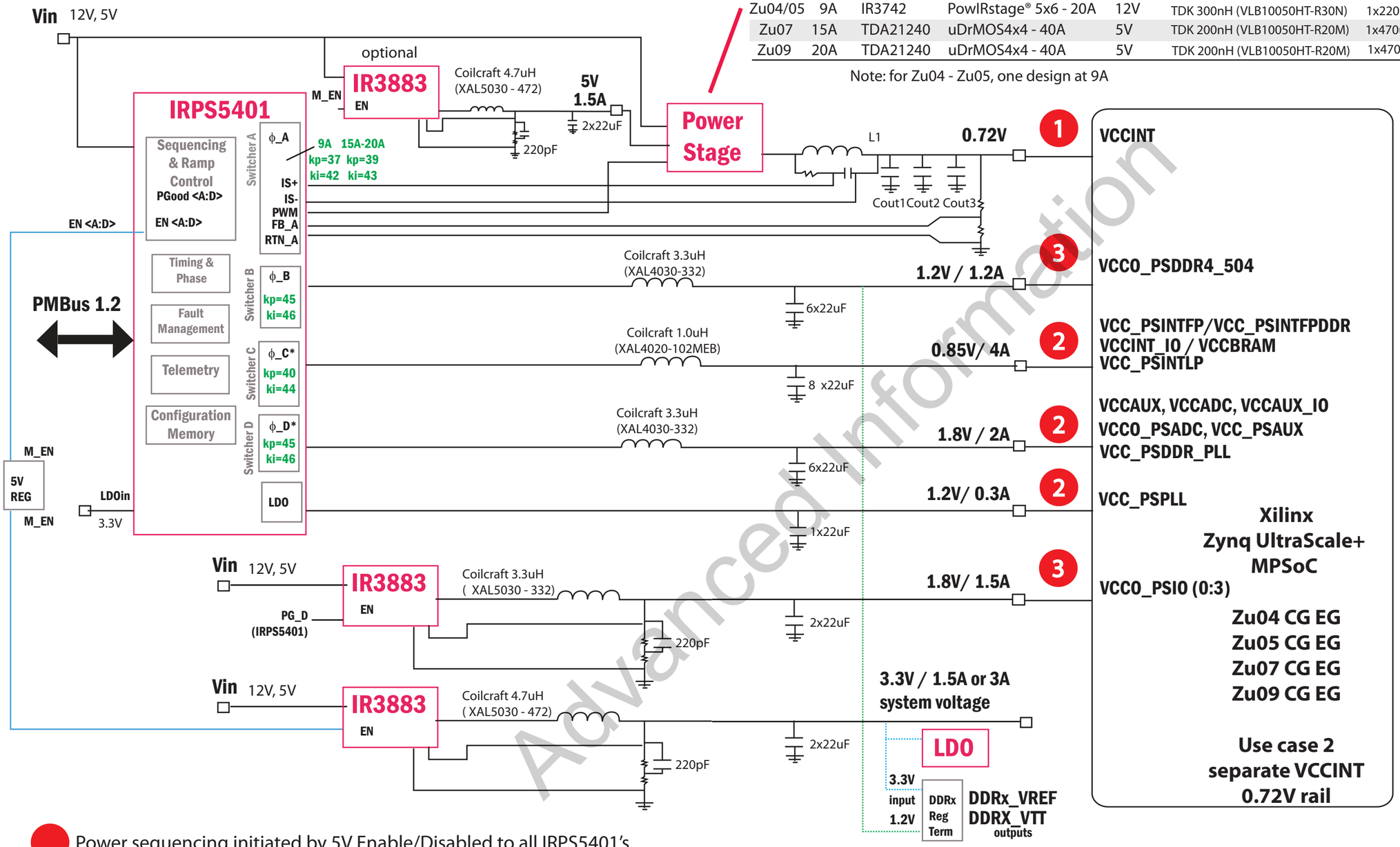
Zynq	Iout	Powerstage	Desc	Bias	Inductor L1	Cout1	Cout2	Cout3
Zu04/05	9A	IR3742	PowIRstage® 5x6 - 20A	12V	TDK 300nH (VLB10050HT-R30N)	1x220uF	2 to 4 x22uF	1x47uF
Zu07	15A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 200nH (VLB10050HT-R20M)	1x470uF	2 to 4 x22uF	1x47uF
Zu09	20A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 200nH (VLB10050HT-R20M)	1x470uF	2 to 4 x22uF	1x47uF

Note: for Zu04 - Zu05, one design at 9A



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Zu07	25A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 120nH (VLB10050HT-R12M)	1x470uF	8x22uF
Zu09	25A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 120nH (VLB10050HT-R12M)	1x470uF	8x22uF

Note: for Zu07 - Zu09, one design at 25A covers 18A to 25A
Zu04 series, covered by Zu05 solutions
Zu06 series can be covered by Zu07 solutions

Vin 12V, 5V

optional
IR3883
M_EN
EN
Coilcraft 4.7uH (XAL5030 - 472)
5V 1.5A
2x22uF
220pF

IRPS5401
Sequencing & Ramp Control
PGood <A:D>
EN <A:D>
Timing & Phase
Fault Management
Telemetry
Configuration Memory
Switcher A: ϕ_A — 16A kp=39 ki=43 — 25A kp=36 ki=41; IS+, IS-, PWM, FB_A, RTN_A
Switcher B: ϕ_B kp=45 ki=46
Switcher C: ϕ_C* kp=44 ki=46
Switcher D: ϕ_D* kp=41 ki=44
LDO

EN <A:D>
PMBus 1.2
M_EN
5V REG
LDOin
M_EN
3.3V
1.8V

Power Stage

L1
Cout1
Cout2

1 — 0.85V / 0.9V
VCC_PSINTFP/VCC_PSINTFPDDR
VCCINT_IO / VCCBRAM
VCC_PSINTLP VCCINT

Coilcraft 3.3uH (XAL4030-332)
6x22uF
3 — 1.2V / 1.5A
VCCO_PSDDR4_504

Coilcraft 4.7uH (XFL4020-472)
4x22uF
3 — 1.8V / 1A
VCCO_PSIO (0:3)
VCCAUX, VCCADC, VCCAUX_IO

Coilcraft 2.2uH (XAL4020-222)
5x22uF
2 — 1.8V / 4A
VCC_PSDDR_PLL VCCIO (0.5A)
VCCO_PSADC, VCC_PSAUX
VPS_MGTRAVTT

1x22uF
2 — 1.2V/ 0.5A
VCC_PSPLL

LDO
3.3V input
1.2V
DDRx Reg Term
DDRx_VREF
DDRX_VTT
outputs

Xilinx Zynq UltraScale+ MPSoC

Zu04 CG, EG, EV
Zu05 CG, EG, EV
Zu07 CG, EG, EV
Zu09 CG, EG

+ SERDES

IRPS5401
Sequencing & Ramp Control
PGood <A:D>
EN <A:D>
Timing & Phase
Fault Management
Telemetry
Configuration Memory
Switcher A: ϕ_A kp=46 ki=48; FB_A, RTN_A
Switcher B: ϕ_B kp=42 ki=44
Switcher C: ϕ_C* kp=44 ki=46
Switcher D: ϕ_D* kp=44 ki=45
LDO

Vin 12V, 5V
EN <A:D>
PMBus 1.2
LDOin
3.3V

Coilcraft 4.7uH (XFL4020-472)
4x22uF
scale factor divider
system voltage option
3.3V/ 1A
1

Coilcraft 4.7uH (XFL4020-472)
4x22uF
2.5V / 1A
1

Coilcraft 1.5uH (XAL4020-152)
8 to 10 x22uF
0.9V / 3A
1

Coilcraft 1.5uH (XAL4020-152)
8 to 10 x22uF
1.2V / 3A
3

1x22uF
0.85V / 0.4A
2

system voltage option
(5V, 2.5V, 1V)

VMGATAVCC,
VMGTYAVCC

VMGTAVTT, VMGTYAVTT,
VCC_PSPLL, VCC_VCU_PLL

VPS_MGTRAVCC

On start up condition of VCC and PVin and an external master enable (M_EN),
Power sequencing can be adjusted by
ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.

Power up sequence (ton_delay)
0ms 2ms 4ms
1 → 2 → 3

Power down sequence (toff_delay)
0ms 2ms 4ms
3 → 2 → 1

If the second IRPS5401 is not desired
the below are regulator options for SERDES:

1) IR3891 Dual 1.2V/1.8V or 0.9V/0.85V for VMGATAVCC, and VMGTAVTT
2) IR3823 for any SERDES < 3A

If more 3.3V system voltage and higher current: 1.5A/3A, 3.3V IR3883

● Power sequencing initiated by 5V Enable/Disabled to all IRPS5401's
All regulators and LDO is turned on/off via
internal settable timers integrated
into the IRPS5401 PMICs.
No external sequencing components are required.
Power Off is the reverse order.

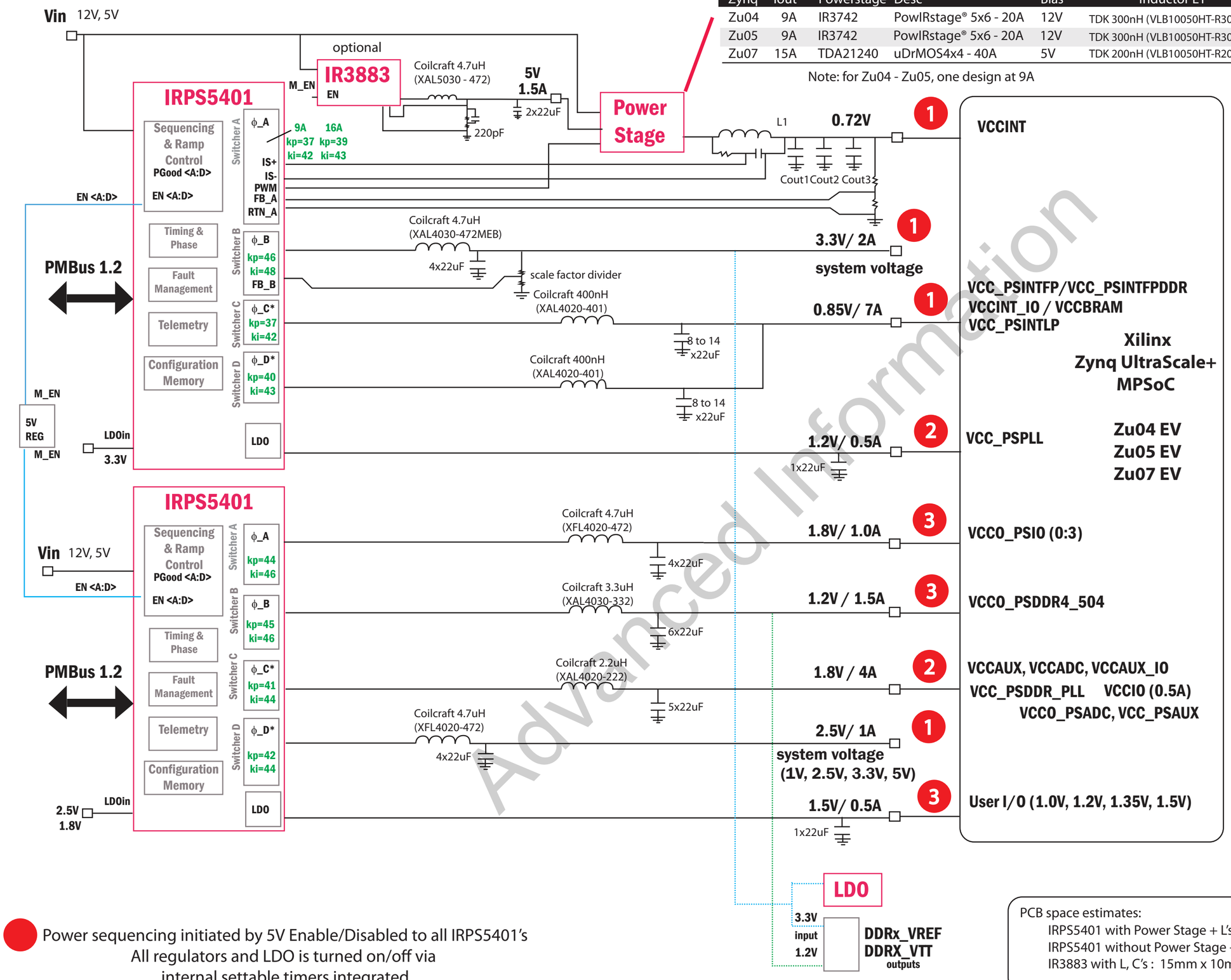
The IRPS5401 regulators do not require external loop compensation components.
The digital compensation kp, ki listed are estimations for the target regulation and may require adjustment.

PCB space estimates:
IRPS5401 with Power Stage + L's, C's : 35mm x 40mm
IRPS5401 without Power Stage + L's, C's: 30mm x 30mm
IR3883 with L, C's : 15mm x 10mm

Infineon Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu04_Zu05_Zu07 EV Series - without SERDES
Always On: Power and/or Efficiency-Optimized Power Rail Consolidation

Zynq	Iout	Powerstage	Desc	Bias	Inductor L1	Cout1	Cout2	Cout3
Zu04	9A	IR3742	PowIRstage® 5x6 - 20A	12V	TDK 300nH (VLB10050HT-R30N)	1x220uF	2 to 4 x22uF	1x47uF
Zu05	9A	IR3742	PowIRstage® 5x6 - 20A	12V	TDK 300nH (VLB10050HT-R30N)	1x220uF	2 to 4 x22uF	1x47uF
Zu07	15A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 200nH (VLB10050HT-R20M)	1x470uF	2 to 4 x22uF	1x47uF

Note: for Zu04 - Zu05, one design at 9A



On start up condition of VCC and PVin and an external master enable (M_EN), Power sequencing can be adjusted by ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.

Power up sequence (ton_delay)

Power down sequence (toff_delay)

Power sequencing initiated by 5V Enable/Disabled to all IRPS5401's
All regulators and LDO is turned on/off via
internal settable timers integrated
into the IRPS5401 PMICs.
No external sequencing components are required.
Power Off is the reverse order.

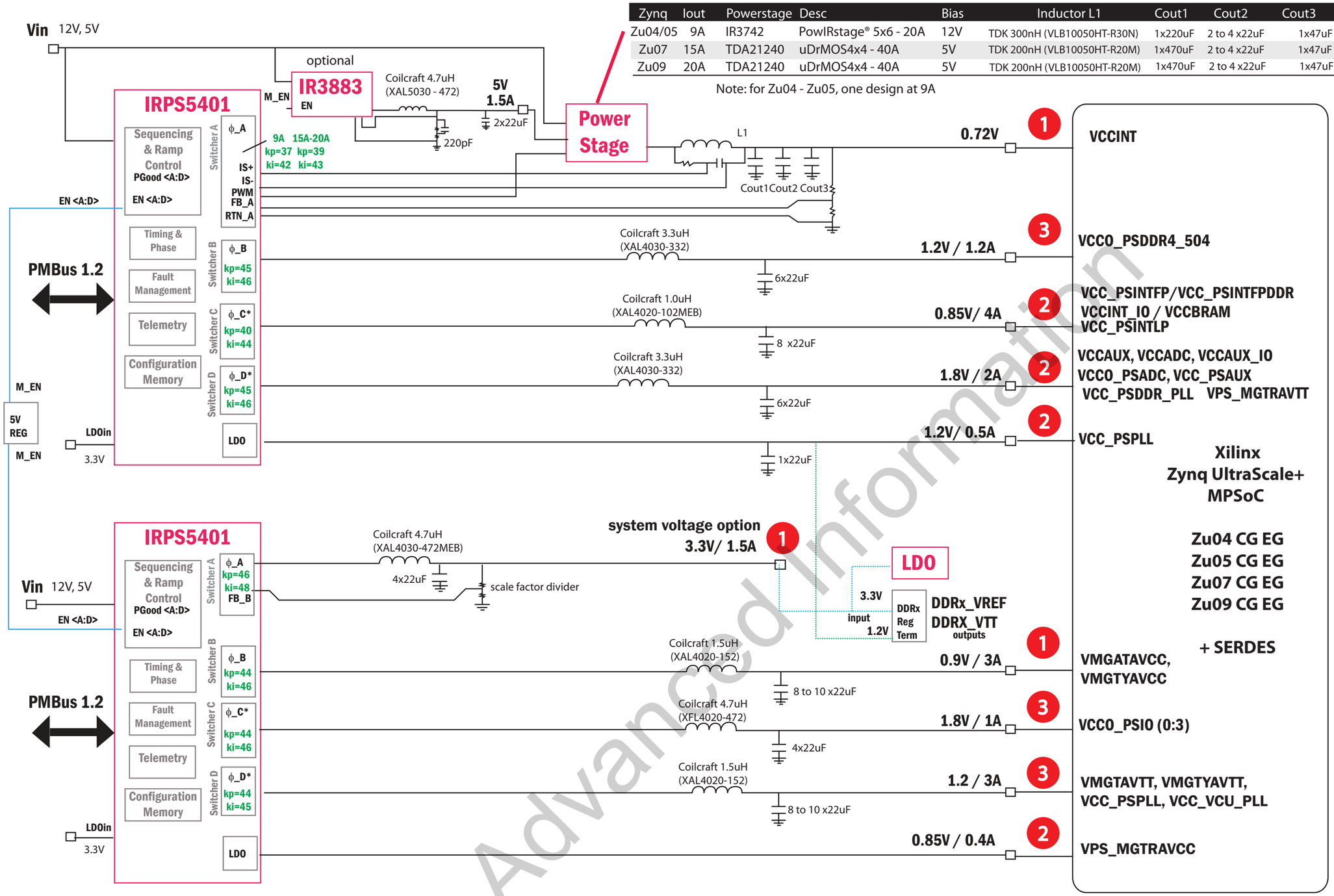
The IRPS5401 regulators do not require external loop compensation components.
The digital compensation kp, ki listed are estimations for the target regulation and may require adjustment.

PCB space estimates:
IRPS5401 with Power Stage + L's, C's : 35mm x 40mm
IRPS5401 without Power Stage + L's, C's: 30mm x 30mm
IR3883 with L, C's : 15mm x 10mm

Infineon Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu04_Zu05_Zu07_Zu09 CG EG Series - with SERDES
Always On: Power and/or Efficiency-Optimized Power Rail Consolidation

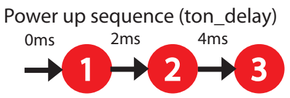
Zynq	Iout	Powerstage	Desc	Bias	Inductor L1	Cout1	Cout2	Cout3
Zu04/05	9A	IR3742	PowIRstage® 5x6 - 20A	12V	TDK 300nH (VLB10050HT-R30N)	1x220uF	2 to 4 x22uF	1x47uF
Zu07	15A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 200nH (VLB10050HT-R20M)	1x470uF	2 to 4 x22uF	1x47uF
Zu09	20A	TDA21240	uDrMOS4x4 - 40A	5V	TDK 200nH (VLB10050HT-R20M)	1x470uF	2 to 4 x22uF	1x47uF

Note: for Zu04 - Zu05, one design at 9A



On start up condition of VCC and PVin and an external master enable (M_EN), Power sequencing can be adjusted by ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.

Power up sequence (ton_delay)



Power down sequence (toff_delay)

Power sequencing initiated by 5V Enable/Disabled to all IRPS5401's
All regulators and LDO is turned on/off via
internal settable timers integrated
into the IRPS5401 PMICs.
No external sequencing components are required.
Power Off is the reverse order.

The IRPS5401 regulators do not require external loop compensation components.
The digital compensation kp, ki listed are estimations for the target regulation and may require adjustment.

If the second IRPS5401 is not desired
the below are regulator options for SERDES:

1) IR3891 Dual 1.2V/1.8V or 0.9V/0.85V for VMGATAVCC, and VMGTAVTT
2) IR3823 for any SERDES < 3A

For second IRPS5401, if board ambient >50C and no airflow consider external 3.3V Regulator (IR3883)

PCB space estimates:
IRPS5401 with Power Stage + L's, C's : 35mm x 40mm
IRPS5401 without Power Stage + L's, C's: 30mm x 30mm
IR3883 with L, C's : 15mm x 10mm

Infineon Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu11, Zu15 and Zu17, Zu19 EG Series - NO SERDES
Always On: Power and/or Efficiency-Optimized Power Rail Consolidation

Zynq	Iout	Powerstage	Desc	Bias	Cout1	Cout2
Zu11_Z15EG	25A	TDA21240	uDrMOS4x4 - 40A	5V?	1x470uF	8 to 14 x22uF
Zu17/19EG	30A	IR3555/6	PowerStage 6x6 - 60/50A	5V	2x470uF	8 to 14 x22uF

Note: for Zu15 - Zu17/19, one design at 35A covers 32A to 35A

Vin 12V, 5V

optional

IR3883 (EN, M_EN) — Coilcraft 4.7uH (XAL5030 - 472) — 220pF — 2x22uF — 5V 1.5A

IRPS5401

Sequencing & Ramp Control; PGood <A:D>; EN <A:D>; Timing & Phase; Fault Management; Telemetry; Configuration Memory

Switcher A: ϕ_A; IS+, IS-, PWM, FB_A, RTN_A — 25A kp=37 ki=42 — 30A kp=36 ki=41

Power Stage — TDK 120nH (VLB10050HT-R12M) L1 — Cout1 — Cout2 — **0.72V** (1) → **VCCINT**

Switcher B: ϕ_B kp=46 ki=48 FB_B — Coilcraft 4.7uH (XAL4030-472MEB) — 4x22uF — scale factor divider — **3.3V/ 2A** (1) → system voltage

Switcher C: ϕ_C* kp=37 ki=42 — Coilcraft 400nH (XAL4020-401) — 8 to 14 x22uF — **0.85V/ 7A** (1) → **VCC_PSINTFP/VCC_PSINTFPDDR, VCCINT_IO / VCCBRAM, VCC_PSINTLP**

Switcher D: ϕ_D* kp=37 ki=42 — Coilcraft 400nH (XAL4020-401) — 8 to 14 x22uF

PMBus 1.2

5V REG; M_EN; LDOin 3.3V; LDO — **1.2V/ 0.5A** (2) → **VCC_PSPLL**

Xilinx Zynq UltraScale+ MPSoC

Zu11 EG, Zu15 EG, Zu17 EG, Zu19 EG

IRPS5401

Vin 12V, 5V

Sequencing & Ramp Control; PGood <A:D>; EN <A:D>; Timing & Phase; Fault Management; Telemetry; Configuration Memory

Switcher A: ϕ_A kp=44 ki=46 — Coilcraft 4.7uH (XFL4020-472) — 4x22uF — **1.8V / 1A** (3) → **VCCO_PSIO (0:3)**

Switcher B: ϕ_B kp=45 ki=46 — Coilcraft 3.3uH (XAL4030-332) — 6x22uF — **1.2V / 1.5A** (3) → **VCCO_PSDDR4_504**

Switcher C: ϕ_C* kp=41 ki=44 — Coilcraft 2.2uH (XAL4020-222) — 5x22uF — **1.8V/ 4A** (2) → **VCCAUX, VCCADC, VCCAUX_IO, VCC_PSDDR_PLL, VCCIO (0.5A), VCCO_PSADC, VCC_PSAUX**

Switcher D: ϕ_D* kp=42 ki=44 — Coilcraft 4.7uH (XFL4020-472) — 4x22uF — **2.5V / 1.5A** (3) → system voltage (1V, 2.5V, 3.3V, 5V) → **USER I/O (0.5A) - (1.0, 1.2, 1.35, 1.5, 1.8, 2.5)**

1.8V 2.5V; LDOin; LDO — **1.0V / 0.4A** (2) → **User I/O (1.0V, 1.2V, 1.35V, 1.5V)**

LDO

3.3V input; 1.2V — **DDRx_VREF, DDRX_VTT** outputs

On start up condition of VCC and PVin and an external master enable (M_EN), Power sequencing can be adjusted by ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.

Power up sequence (ton_delay)

Power down sequence (toff_delay)

Power sequencing initiated by 5V Enable/Disabled to all IRPS5401's
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internal settable timers integrated
into the IRPS5401 PMICs.
No external sequencing components are required.
Power Off is the reverse order.

IRPS5401 with Power Stage + L's, C's : 35mm x 40mm
IRPS5401 without Power Stage + L's, C's: 30mm x 30mm
IR3883 with L, C's : 15mm x 10mm

The IRPS5401 regulators do not require external loop compensation components.
The digital compensation kp, ki listed are estimations for the target regulation and may require adjustment.

Infineon Power Solution for Xilinx
Zynq UltraScale+ MPSoC
Zu11, Zu15 and Zu17, Zu19 EG Series - with SERDES
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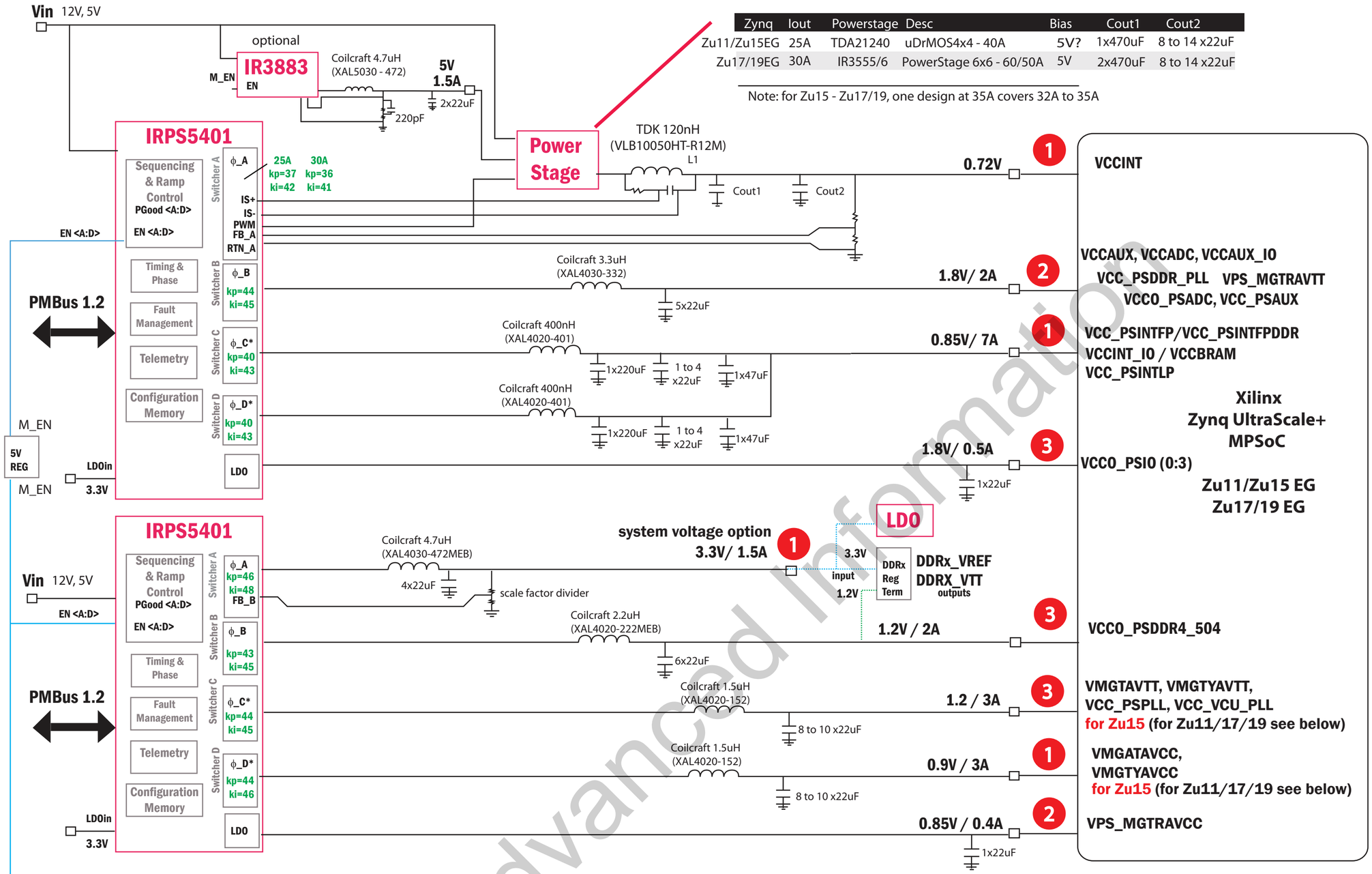
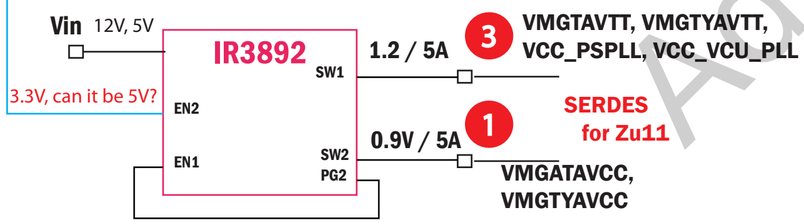
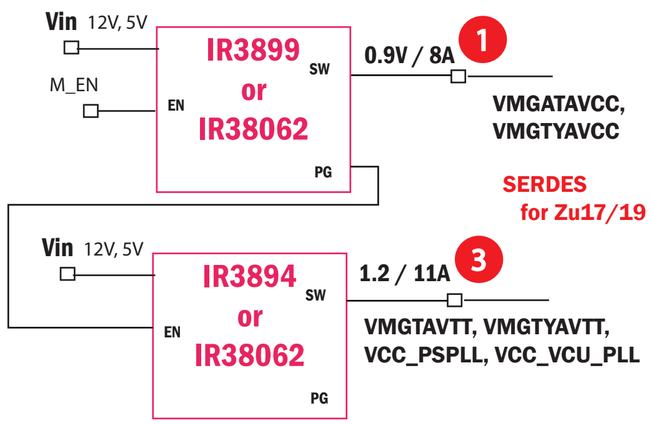
Zynq	Iout	Powerstage	Desc	Bias	Cout1	Cout2
Zu11/Zu15EG	25A	TDA21240	uDrMOS4x4 - 40A	5V?	1x470uF	8 to 14 x22uF
Zu17/19EG	30A	IR3555/6	PowerStage 6x6 - 60/50A	5V	2x470uF	8 to 14 x22uF

Note: for Zu15 - Zu17/19, one design at 35A covers 32A to 35A







If additional 3.3V required: 1.5A/3A - IR3883

On start up condition of VCC and PVin and an external master enable (M_EN), Power sequencing can be adjusted by ton_delay and toff_delay in 1ms increments from 0ms to 127ms for each regulator.

Power up sequence (ton_delay)

Power down sequence (toff_delay)

IRPS5401 with Power Stage + L's, C's : 35mm x 40mm
IRPS5401 without Power Stage + L's, C's: 30mm x 30mm
IR3883 with L, C's : 15mm x 10mm

IR3892 with L, C's: 20mm x 20 mm

IR3899 or IR3894 with L, C's: 15mm x 20mm

IR38062 with L, C's: 16mm x 21mm

Power sequencing initiated by 5V Enable/Disabled to all IRPS5401's
All regulators and LDO is turned on/off via
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into the IRPS5401 PMICs.
No external sequencing components are required.
Power Off is the reverse order.

The IRPS5401 regulators do not require external loop compensation components.
The digital compensation kp, ki listed are estimations for the target regulation and may require adjustment.

Part of your life. Part of tomorrow.