600 W FB-FB quarter brick using the XDPP1100 digital controller

48 V-to-12 V voltage mode control with flux balancing

Scope and purpose

This document describes the design and performance of a digitally controlled isolated 600 W full-bridge to full-bridge rectification converter with Voltage Mode Control (VMC). The quarter-brick has a main power stage that converts 42 V to 75 V to 12 V output and an auxiliary power supply to provide bias voltage for a primary gate driver, secondary gate driver and 3.3 V VDD. The XDPP1100 is a digital controller based on a 32-bit, 100 MHz ARM® Cortex™-M0 RISC microprocessor with analog/mixed-signal capabilities. It has 64 kB OTP, 32 kB RAM and 80 kB ROM memories. The digital controls provide the utmost flexibility in design, efficiency, optimization and flux balance (as an alternative to Peak Current Mode Control, PCMC) to avoid DC flux walk-away. This 600 W evaluation unit follows the DOSA mechanical outline for high-current quarter-bricks.

The main Infineon components used in the 600 W digital FB-FB quarter-brick are:

- XDPP1100 XDP™ IDC digital controller
- 100 V OptiMOS™ 5 BSC050N10NS5, 100 V 5 mΩ, SuperS08 power transistors
- 40 V OptiMOS™ 6 BSC010N04LS6, 40 V 1 mΩ, SuperS08 power transistors
- EiceDRIVER™ 2EDF7275K – Infineon's isolated dual gate driver

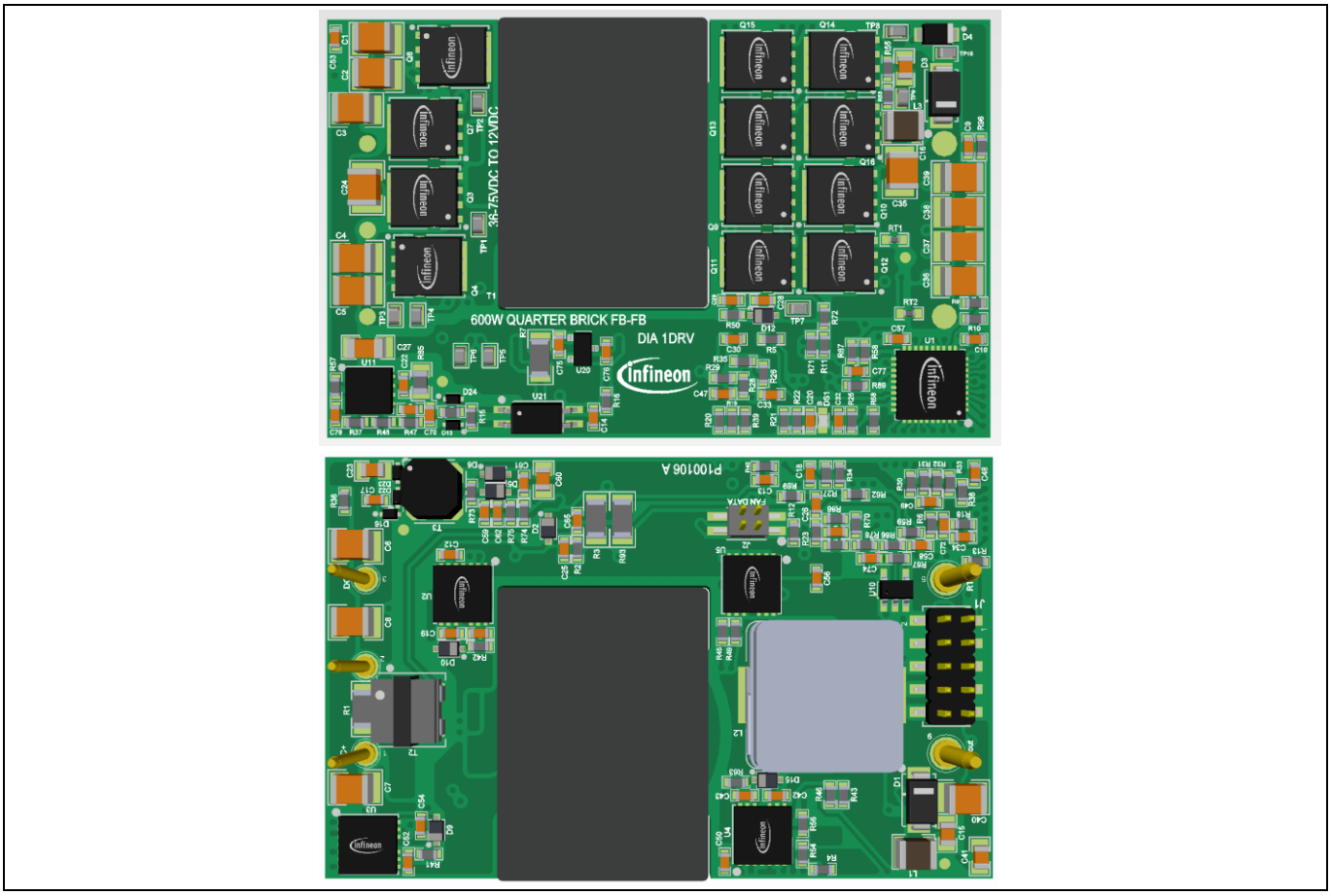

Figure 1 Infineon 600 W digital FB-FB quarter-brick evaluation unit outline

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1 Background and system description

The trend in SMPS in recent years has been toward increased power density with optimized cost. Table 1 shows the comparison of major topologies of the telecom bricks that convert 48 V input to 12 V output.

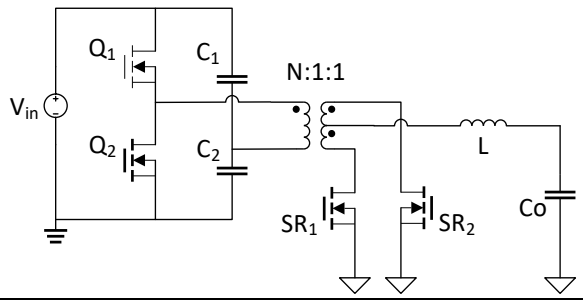
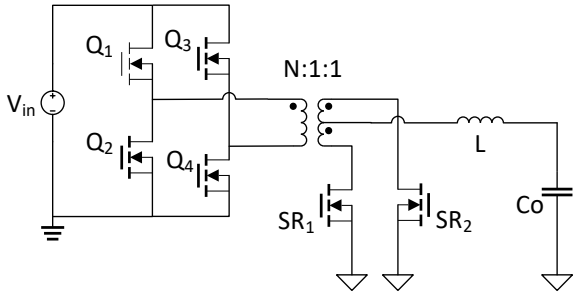
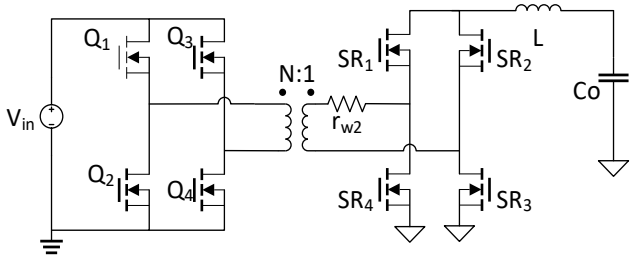
High efficiency is a key parameter in achieving this increasing power density, because heat dissipation must be minimized. Furthermore, higher efficiency directly impacts the ownership cost during the lifetime of the converter. Toward this goal, full-bridge to full-bridge topologies are often considered to be the best approach in the 600 W to 800 W power range.

This document describes the system and hardware of the digitally controlled isolated 600 W full-bridge to full-bridge quarter-brick. With the digital controller XDPP1100, the dead-time can be optimized for the best efficiency; the Feed-Forward (FF) is achieved with secondary Voltage Sensing; the flux balancing enables VMC without using DC blocking capacitors; the enhanced protection features eliminate external fault comparators; the active current sharing makes the system scalable for higher power with parallel modules.

For further information on Infineon semiconductors see the Infineon website, as well as the Infineon evaluation board search tool, and the different websites for the different implemented components:

- OptiMOS™ power MOSFETs
- Gate driver ICs
- XDP™ SMPS microcontrollers

Table 1 Major topologies of telecom bricks (quarter-brick and eighth-brick)

Topology	Circuit	Cost/complexity	Efficiency	Output power
HB_CT		Excellent, low component count on both primary and secondary	Medium	120 W to 300 W
FB_CT		Medium, the secondary driver is reference to ground	High	300 W to 600 W
FB_FB		High, both primary and secondary are HB type	The highest	600 W to 800 W

1.1 System description

The 600 W isolated FB-FB quarter-brick DC-DC converter is a new generation of digital controlled DC to DC power module designed to support telecom 12 V DC intermediate bus applications. The Infineon evaluation unit operates from an input voltage range of 36 to 75 V DC and provides up to 600 W output power. Note, below 42 V DC the converter will lose 12 V DC regulation and will drop to around 10.8 V at 36 V input. But it still provides the same output current. The output is fully isolated from the input, allowing versatile polarity configurations and grounding connections to the input and output terminals. The 600 W digital FB-FB quarter-brick design consists of a primary-side full-bridge converter with SR in full-bridge configuration switching at 250 kHz, with an Infineon-designed CDL lossless snubber used on the secondary side. The isolated gate driver 2EDF7275K is used on both the primary and secondary side to simplify the Bill of Materials (BOM) and reduce inventory management cost, as shown in the block diagram (**Figure 2**).

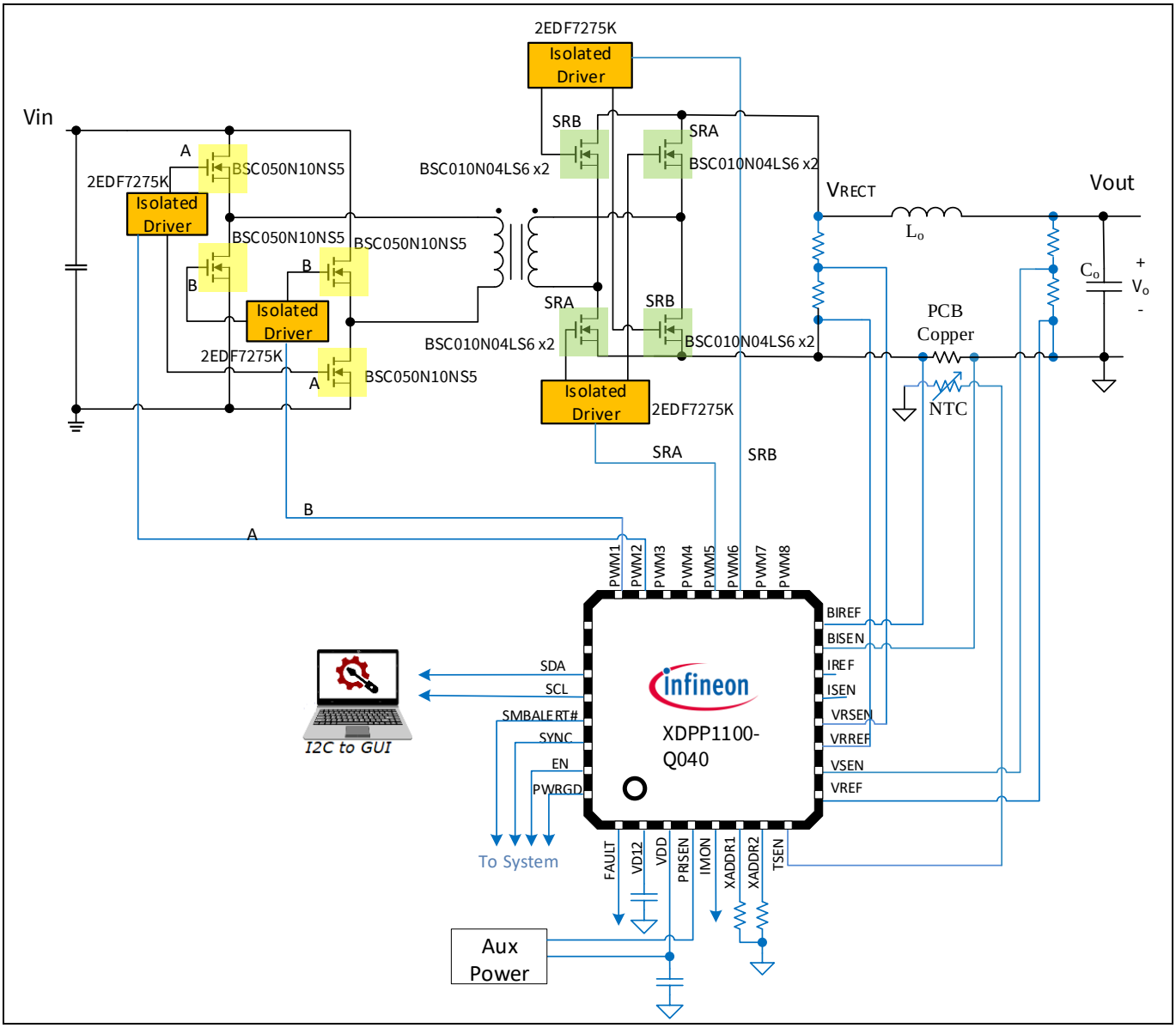


Figure 2 Infineon 600 W digital FB-FB evaluation board – simplified block diagram

The loop control is implemented with Infineon XDPP1100-Q040. The XDPP1100 is a digital power supply controller with analog/mixed-signal capabilities, on-chip memories and communication peripherals. The device is specifically optimized to enhance the performance of isolated DC-DC applications and reduce the

solution component count in the telecom brick converters. It has a -40°C to 125°C operational temperature range.

The XDPP1100 supports both VMC and PCMC. This 600 W demo board could be configured to operate in either VMC or PCMC. This document describes VMC. When configured to VMC, **flux balancing** is enabled.

The voltage sense ADC is an 11-bit ADC with 50 MHz sampling rate. The ADC resolution is 1.25 mV and enhanced with 3-bit digital modulation for output voltage regulation. This gives 156 µV resolution at the sense pin and 1.58 mV resolution at the 12 V output with a scale of 0.099. The hardware resolution limits the highest resolution the board can achieve. Hence, setting PMBus command VOUT_MODE to -10 (resolution 0.976 mV), -11 (resolution 0.488 mV) or -12 (resolution 0.244 mV) will give the same result. This design configures VOUT_MODE = -12.

The voltage ADC is also designed to sense a high-frequency switching signal and makes it perfectly suited to sensing the input voltage from the transformer secondary side at the switching node V_{rect}. This eliminates the use of an isolated op-amp or other types of isolator for input voltage sensing. The input voltage is computed based on the resistor-divider ratio and transformer turns ratio. The information is used for V_{IN} telemetry, protection and feed-forward compensation. When the voltage ADC is configured as V_{rect} sense mode, it senses both the amplitude of the voltage and the duration of the pulse. This feature is used for the volt-second flux balancing control.

The current sense ADC is 9-bit ADC with 25 MHz sampling rate. Exceptional noise immunity is achieved by the use of the internal current estimator. Based on the state of the PWM pulse, the controller continuously predicts DC and ripple current. The result of the prediction is combined with the actual measured current to be processed by the controller. Hence, the instantaneous noise in the measurement can be filtered out without losing the valuable ripple current information.

It can also sense input voltage through the telemetry ADC input (PRISEN pin) before switching starts up. In this design, the input voltage information is taken from the bias power supply. The gain and offset of the PRISEN voltage sense can be configured by two registers for accurate V_{IN} telemetry. The telemetry ADC is a 9-bit ADC with a sample frequency of 1 MHz. The telemetry ADC block consists of eight channels and can be configured to digitize voltages, currents, impedance and temperature.

The XDPP1100 has two temperature sense channels. In this design, ATSEN senses PCB shunt resistor temperature and is used for current sense temperature compensation. BTSEN senses SR MOSFET temperature and is used for over-temperature protection.

The XDPP1100 has two address pins. A resistor between the address pin and ground programs the address offset of the device. Each address pin supports an 8-valent or 16-valent address table. When more than one quarter-brick module is connected in parallel, the address offset enables the system to communicate and program multiple devices via the same I^2C bus. The address offset resistor is not populated on the brick board and it is usually programmed by the resistor on the system board.

Outstanding efficiency can be achieved by using a 100 V OptiMOS™ 5 in a SuperS08 package at the primary together with a 40 V OptiMOS™ 6 in a SuperS08 package for secondary sync FETs. The outstanding performance of these semiconductor technologies, and the planar magnetic construction, enables power density in the range of 22 W/cm^3 (360 W/in^3). The board was designed as a testing platform, with easy access to probe test points, and easy reworking/replacement of components.

1.2 Sync rectifier timing

The secondary sync rectifier timing is critical in telecom brick design for efficiency optimization. The isolator delay must be taken into account along with the propagation delays in drivers to make sure there is no shoot-through between the primary and the secondary opposite phases. The dead-time of the sync rectification should be set as small as possible, to have the highest efficiency and minimize body diode conduction losses.

The ideal gate timing diagram is shown in **Figure 3**, and the bad gate timing diagram is shown in **Figure 4** for reference.

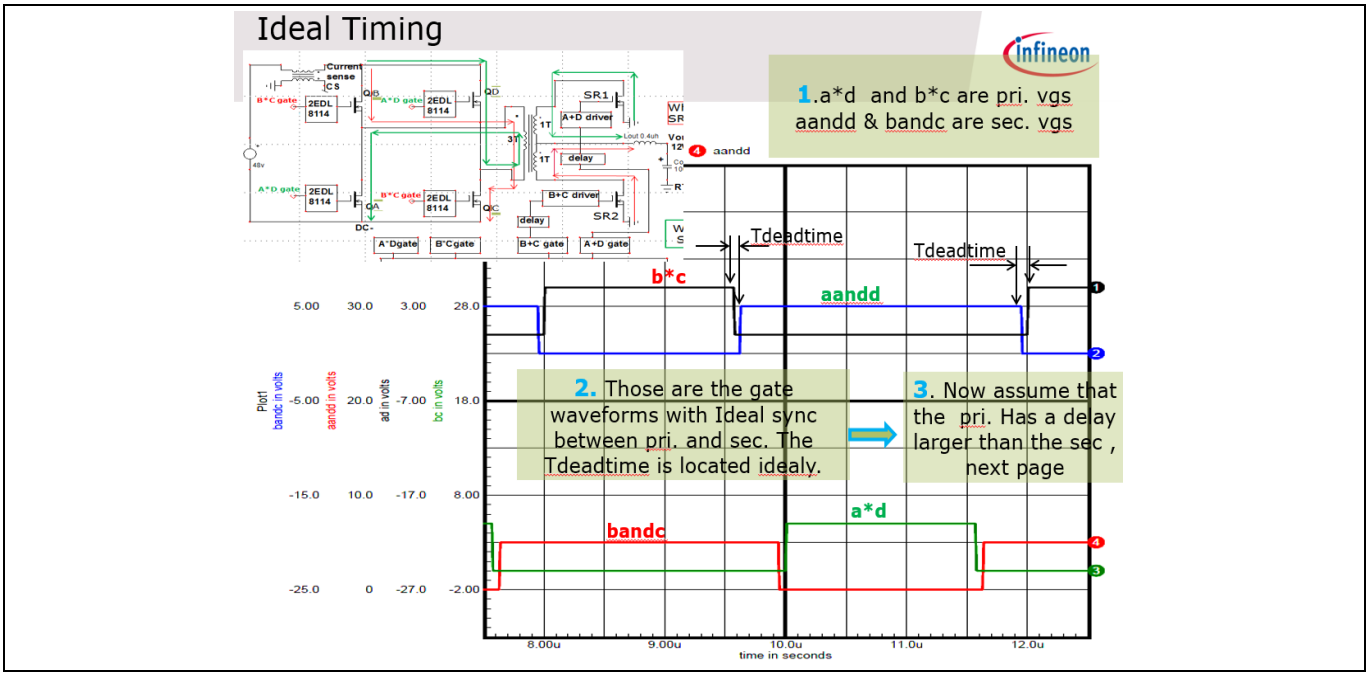


Figure 3 Ideal secondary gate timing example

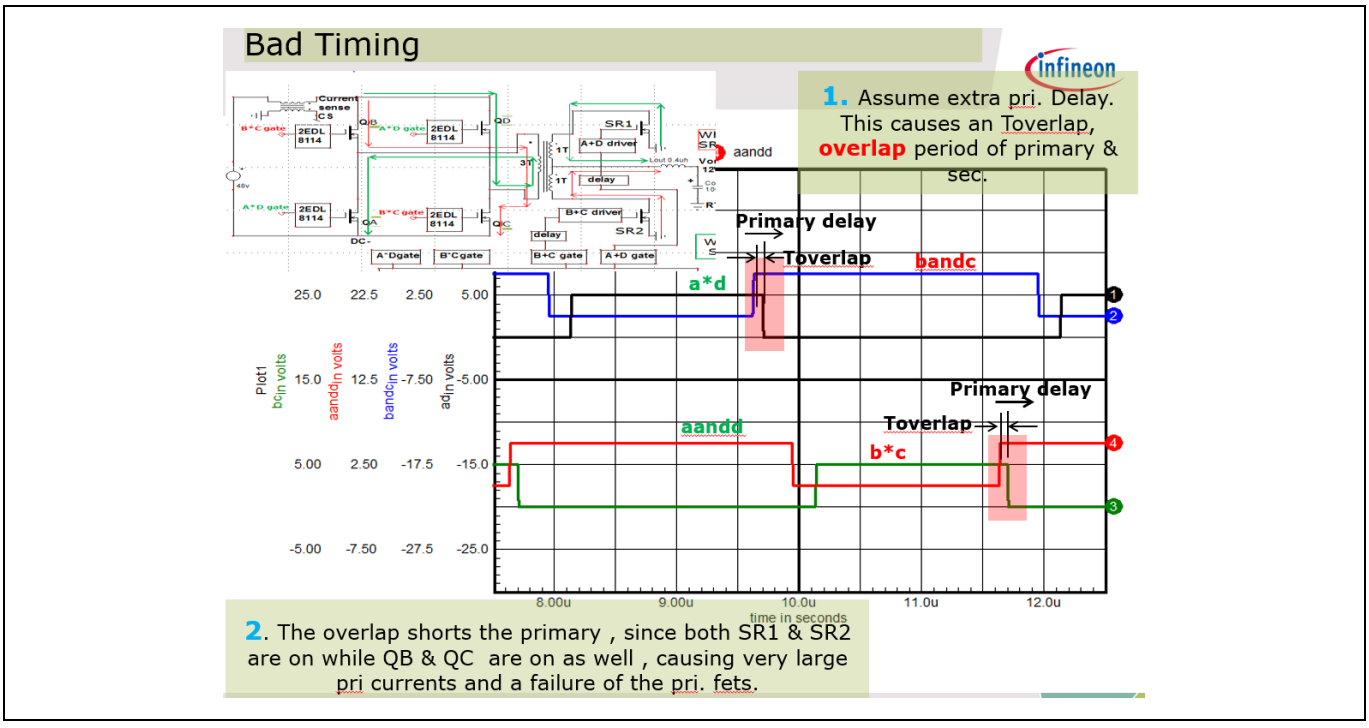


Figure 4 Bad gate timing example

The beauty of digital control is that the parameters can be fine-tuned after the board hardware is fixed. The XDPP1100 enables separate configuration of the dead-time for each PWM output. The rising edge and falling edge delay can be programmed independently. See section 3.1.6 for details. Dynamic dead-time can be implemented by firmware (FW) to further improve efficiency over the full load range.

2 Power board information

2.1 Specification

The specification of the 600 W FB-FB board is shown in **Table 2**.

Table 2 Specification

	Min.	Typ.	Max.	Unit
Input voltage range	36		75	V
V_{IN} turn-on threshold	33			V
V_{IN} turn-off threshold	32			V
Maximum input current (100 percent load, 42 V_{IN})			16	A
Output voltage (at V_{IN} = 42 V to 72 V)		12		V
Output current			50	A
Recommended output capacitor	1000		10000	µF
Output voltage load regulation (V_{IN} = 48 V)		±30	±80	mV
Output voltage line regulation (I_{OUT} = 0 A)		±50		mV
Output voltage regulation over-temperature (V_{IN} = 48 V, T_c = -40°C to 85°C)		±100		mV
Output voltage ripple (peak-to-peak at full load) With 1000 µF output capacitor			240	mV
Load transient (48 V_{IN}, 1000 µF and 10 µF, 1 A/µs) 50 percent to 75 percent load		±300		mV
Load transient settling time		100		µs
V_{OUT} over-voltage protection		13.2		V
Switching frequency		250		kHz
Frequency set-point accuracy	-1		1	%
External sync tolerance	-6		6	%
Logic output high	2.6			V
Logic output low			0.4	V
Logic input high	1.2			V
Logic input low			0.8	V
Efficiency at 48 V, half load		96.2		%
Operating temperature (ambient)	-40		80	°C
Isolation voltage		1500		V
Monitoring accuracy – READ_VIN	-0.5		0.5	V
Monitoring accuracy – READ_VOUT	-10		10	mV
Monitoring accuracy – READ_IOUT	-1		1	A
Monitoring accuracy – READ_TEMPERATURE	-5		5	°C

2.2 Schematic

Figure 5 is the schematic of the power stage of the 12 V/50 A FB-FB converter. Primary MOSFETs are 100 V/5 mΩ OptiMOS™ **BSC050N10NS5ATMA**. Infineon isolated gate driver **2EDF7275K** is used to drive primary MOSFETs. The 2EDF7275K provides 1.5 kV functional isolation and 4 A/8 A gate driver capability. The secondary SR uses two 40 V/1 mΩ **BSC010N04LS6** in parallel at each location. The SR MOSFETs are also driven by **2EDF7275K** to simplify the BOM.

A planar transformer is used for the lowest board profile. The transformer core is ML95S EQ25 + plate from Hitachi Metals. The transformer turns ratio is 3:1. Transformer construction is shown in **Figure 12**.

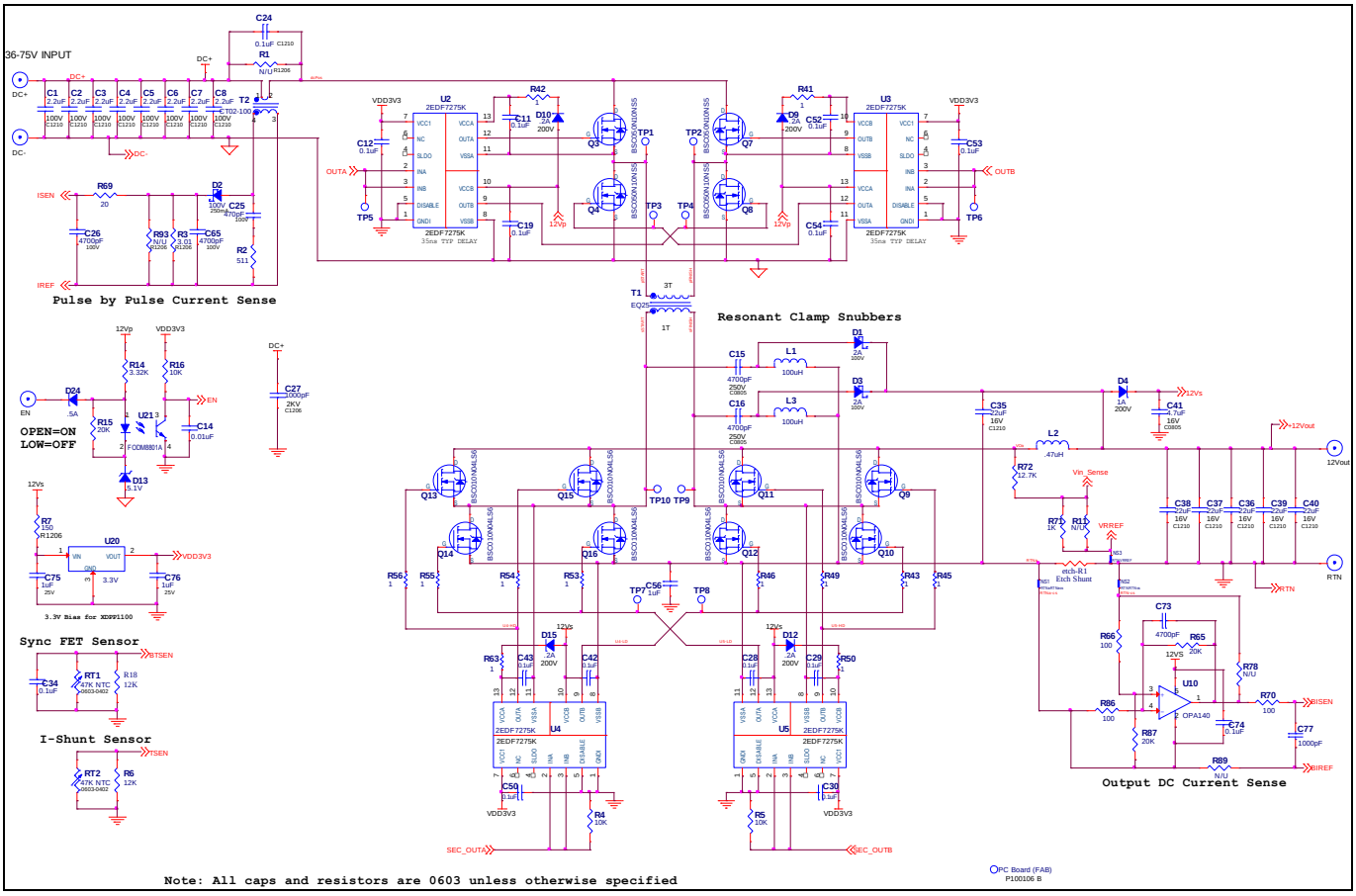


Figure 5 600 W 12 V/50 A FB-FB power stage schematic

The schematic of control circuit and auxiliary power supply is shown in **Figure 6**.

In this reference design, the **XDPP1100-Q040** digital controller enables one loop in VMC. The output voltage is sensed by VSEN/VREF ADC. The other ADC VRSEN/VRREF is used to sense the input voltage through the transformer secondary winding. There are two high-speed current ADCs. AISEN is used to sense primary current, BISEN is used to sense the output current. For the VMC, only BISEN of the secondary current sense is enabled. The same power board also can be configured as PCMC, which enables both AISEN and BISEN. This will be described in another document.

XDPP1100 devices can be configured with an easy-to-use Graphical User Interface (GUI). The software can be downloaded from the Infineon website.

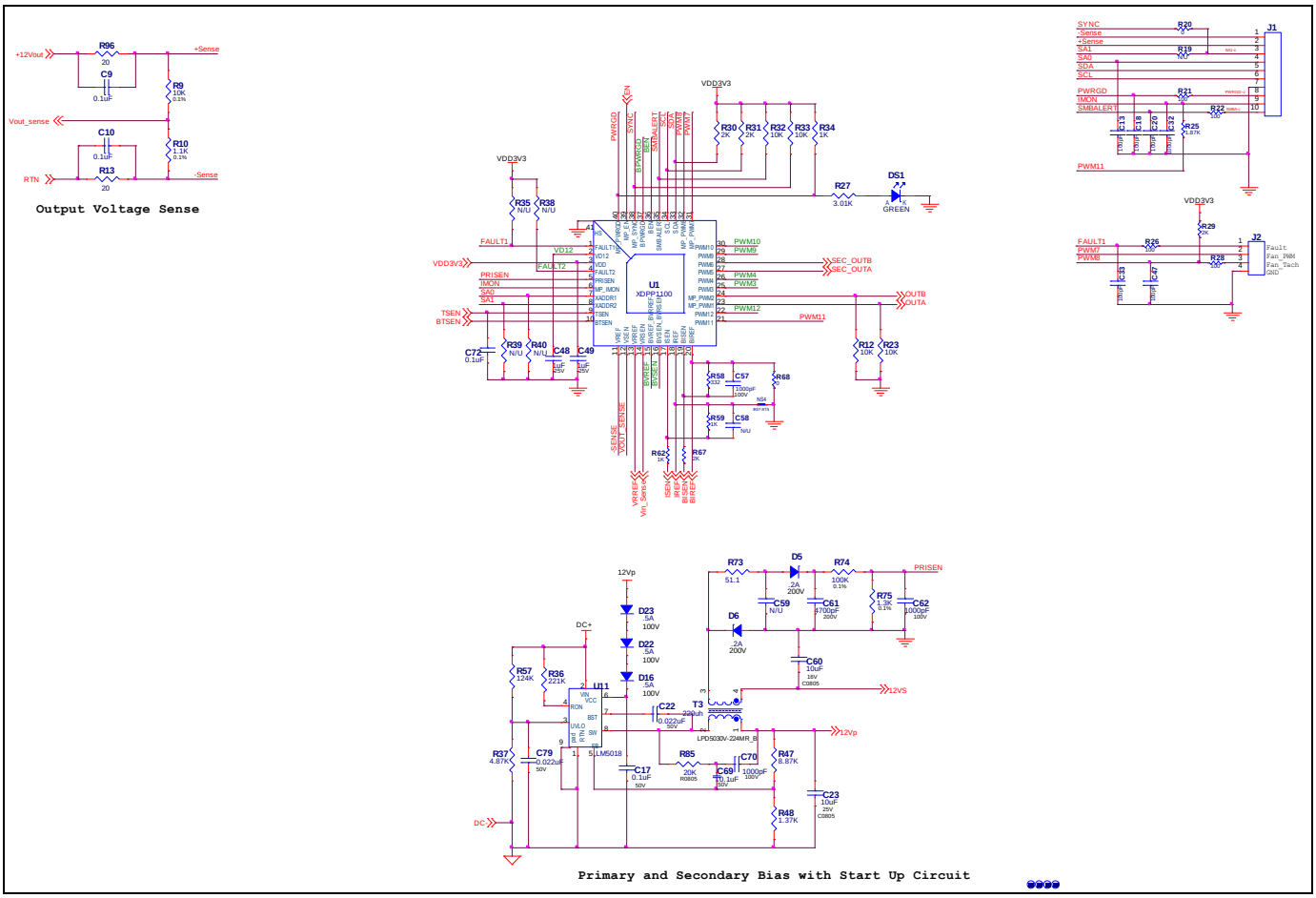


Figure 6 XDPP1100 control circuit schematic

2.3 Test fixture

The quarter-brick test fixture is the test platform for the quarter-brick. It provides power connection terminals, communication and debugging ports, as well as a cooling fan.

Figure 7 shows the schematic of the test fixture. It has an I²C connector for I²C and PMBus communication, and a SWD debugger port for FW debugging. The fan should be biased with external DC power supply, in the 5 V to 12 V range for different airflow. This bias is necessary to enable communication with the XDPP1100 to the USB dongle.

The switch SW1 at the primary is the enable switch to turn on the quarter-brick. Please pay attention that the polarity of the enable can be configured by PMBus command ON_OFF_CONFIG. If EN “active low” is preferred, the user should write PMBus command ON_OFF_CONFIG and choose the polarity to be “active low”. When “active low” is selected, the on/off label on the test fixture aligns with the actual on/off status. If “active high” is selected, the on/off label shows opposite status.

A 3.3 V LDO regulator on the test fixture provides pull-up voltage to the SDA/SCL I²C communication bus when 5 to 12 V is applied to the external bias connector.

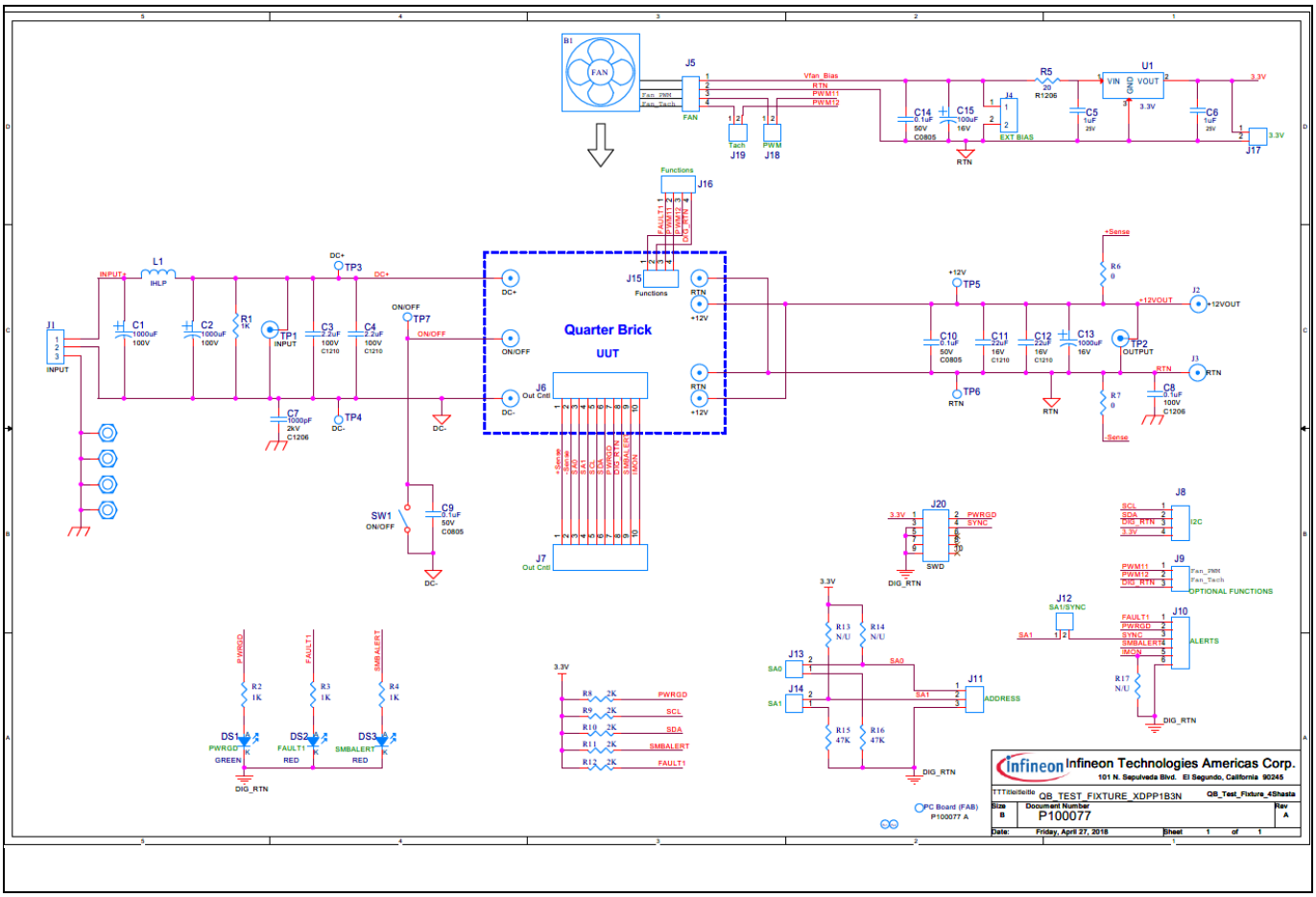


Figure 7 Test fixture schematic

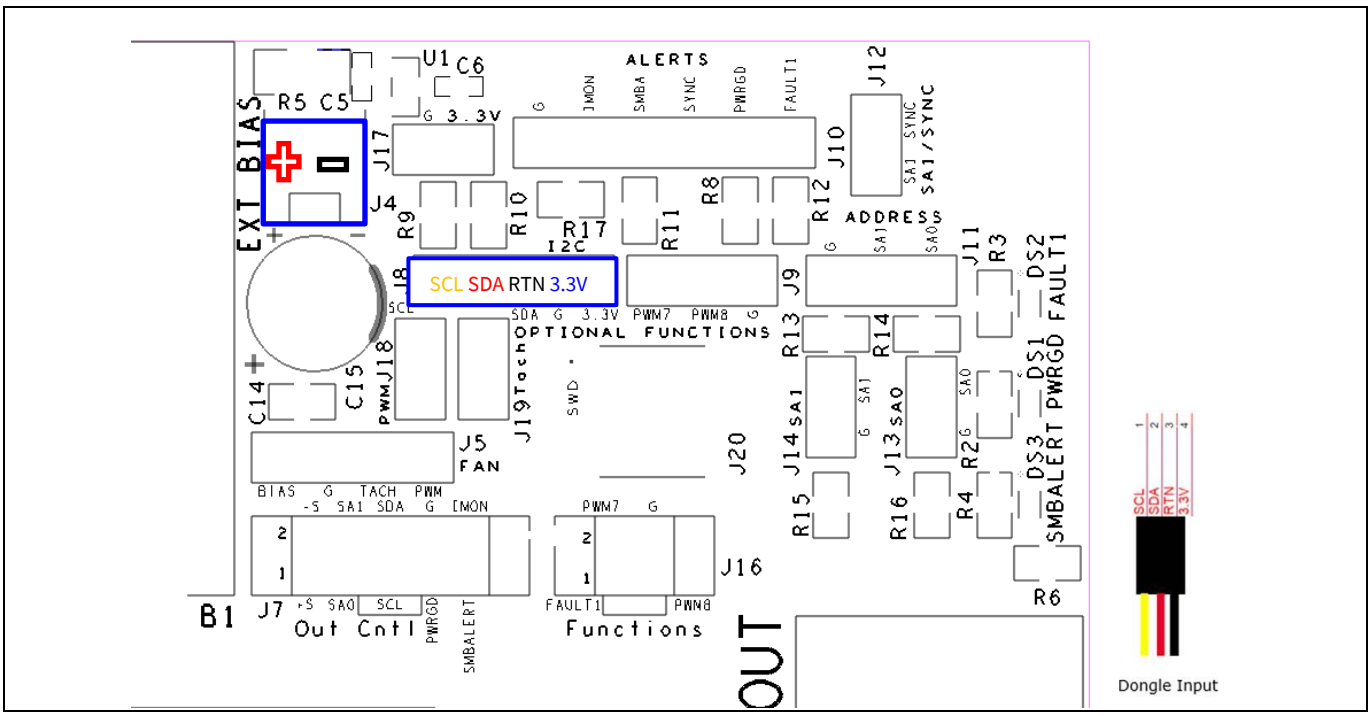


Figure 8 Test fixture external bias connector and I2C connection

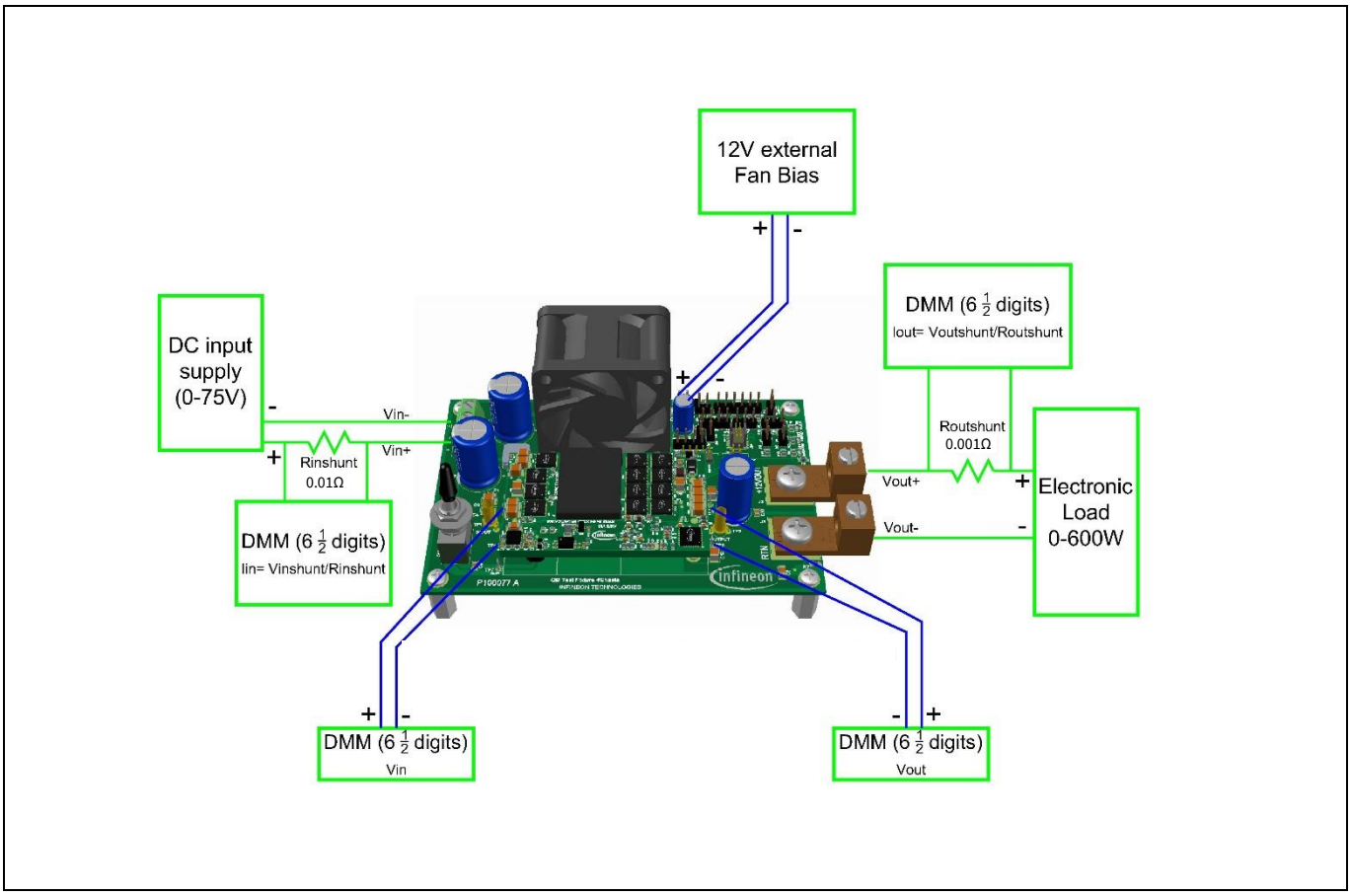


Figure 9 Test fixture board connection

Necessary connections to operate the board:

- Connect the quarter-brick to the test fixture. Make sure the DC input, 12 V output and signal connector J6 have good contact.
- Connect input voltage to J1.
- Connect E-load to J2 and J3.
- Connect the bias fan with 5~12 V DC power supply at J4 (EXT BIAS).
- Connect XDPP1100 USB dongle (USB007 revA) to J8. Find the direction by identifying the ground pin G (black wire). The blue wire of USB007A is not used and can be left floating. If using the isolated dongle USB007 revB, the blue wire should be connected to the 3.3 V pin of J8.
- Make sure the switch SW1 is in the off position
- Turn on the 48 V input power supply. Minimum 35 V voltage is required to enable the auxiliary power supply.
- When the auxiliary power supply is in operation, the 12 VS should have 10 V ±1 V voltage.
- This demo board comes with a default patch and configuration stored in non-volatile memory (OTP) and can be turned on once the operation command is asserted from the XDPP1100 GUI.
- In order to assert the operation command, open XDPP1100 GUI and click on “Auto populate”. The auto populate option is in the top-left corner just below the File option. Once auto populated, the GUI reads the configuration from the device.
- Check if the PMBus commands are configured properly by reading VOUT_COMMAND. It should read 12 V.
- Write “ON” to PMBus command 0x01 OPERATION, and turn SW1 to the on position (the sequence is not critical). The converter should regulate 12 V output for an input voltage range of 42 to 75 V.

2.4 Board layout

The following layout guideline is recommended for the XDPP1100 controller.

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they carry large amounts of energy and tend to generate high levels of noise. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized.

Critical small-signal components including the VDD and VD12 decoupling capacitors, ISEN resistors, TSEN capacitors and voltage feedback RC filters should be placed near the controller.

For each voltage sense and current sense input, i.e. VSEN/VREF, ISEN/IREF, route the signal and its reference in differential pairs (Kelvin connection).

Avoid routing the VRSEN/VRREF, BVRSEN/BVRREF lines near any switching nodes, especially in dual-loop or two-phase applications. Unlike output voltage sensing, VRSEN measures pulse signal, so it can't use a large filter to reduce noise. Keeping the trace shielded by ground plane is recommended.

Avoid putting the current sense resistor or copper shunt next to any switching node. In high-gain current sense mode, put the XDPP1100 as close as possible to the sense resistor. One good practice is putting the XDPP1100 on top of the sense resistor on the other side of the PCB. If a copper shunt is used for current sense, put the temperature sense NTC or sense diode close to the copper shunt for accurate temperature compensation.

If low-gain mode is selected for current sense, put the current sense amplifier as close as possible to the shunt resistor. This method is best when used in noisy environments.

Figure 10 and **Figure 11** show the top and bottom of the 600 W FB-FB demo board.

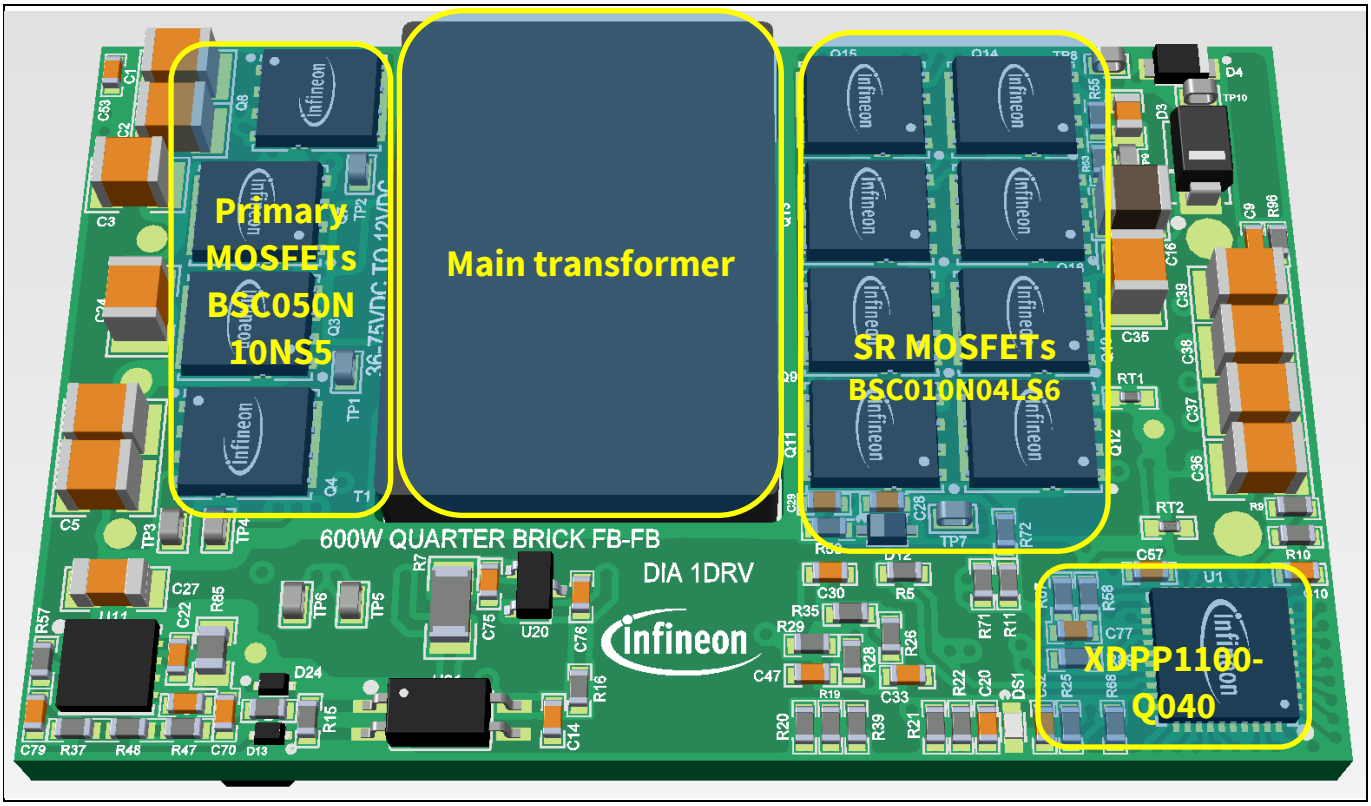


Figure 10 Assembly – top

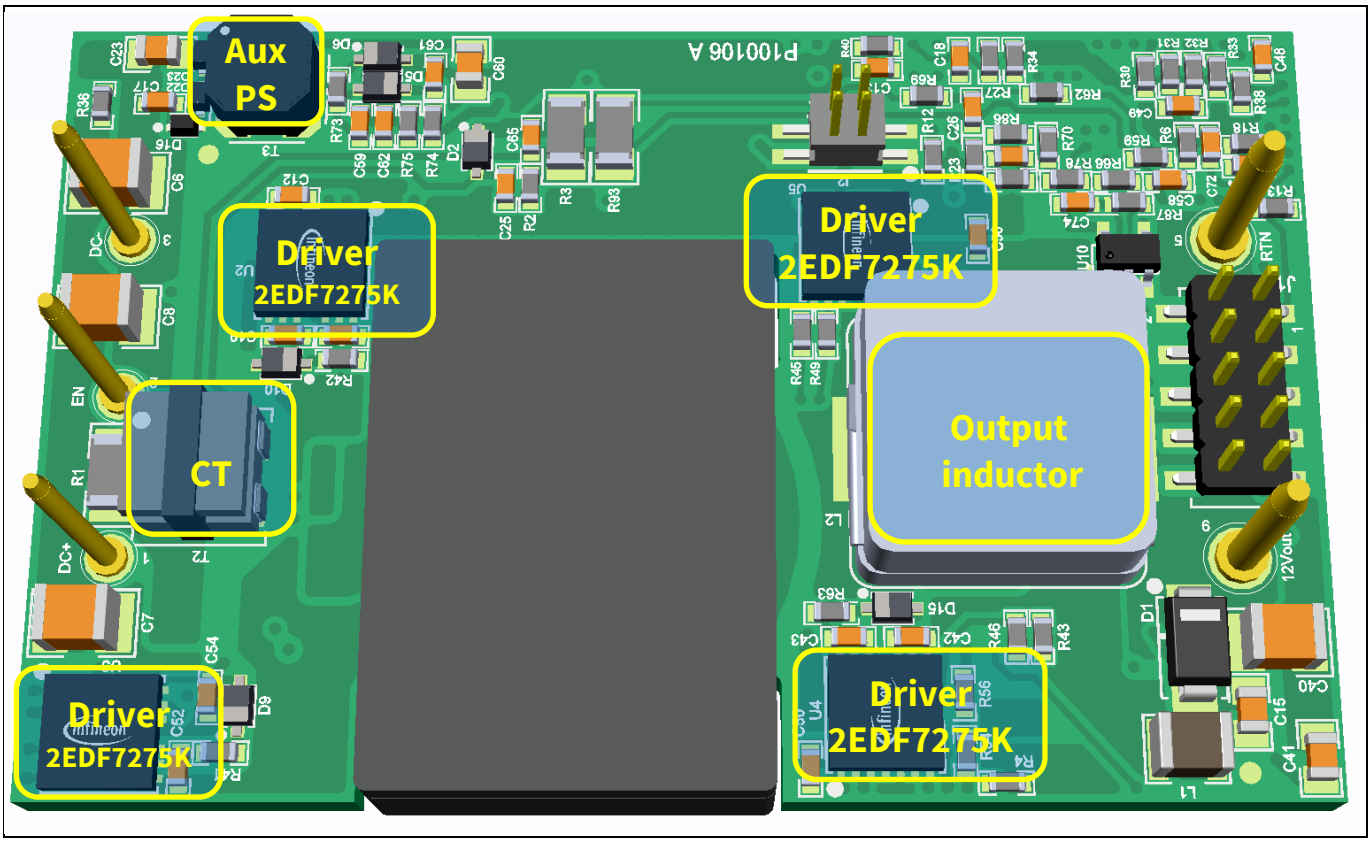


Figure 11 Assembly – bottom

2.5 Main transformer

The planar transformer has three turns in primary and one turn in secondary. The primary winding takes layers 1, 2, 5, 6, 9 and 10, one turn per layer. The secondary winding takes layers 3, 4, 7 and 8, one turn per layer. The middle layer has 5 oz. copper and the top and bottom layer has 4 oz. thickness.

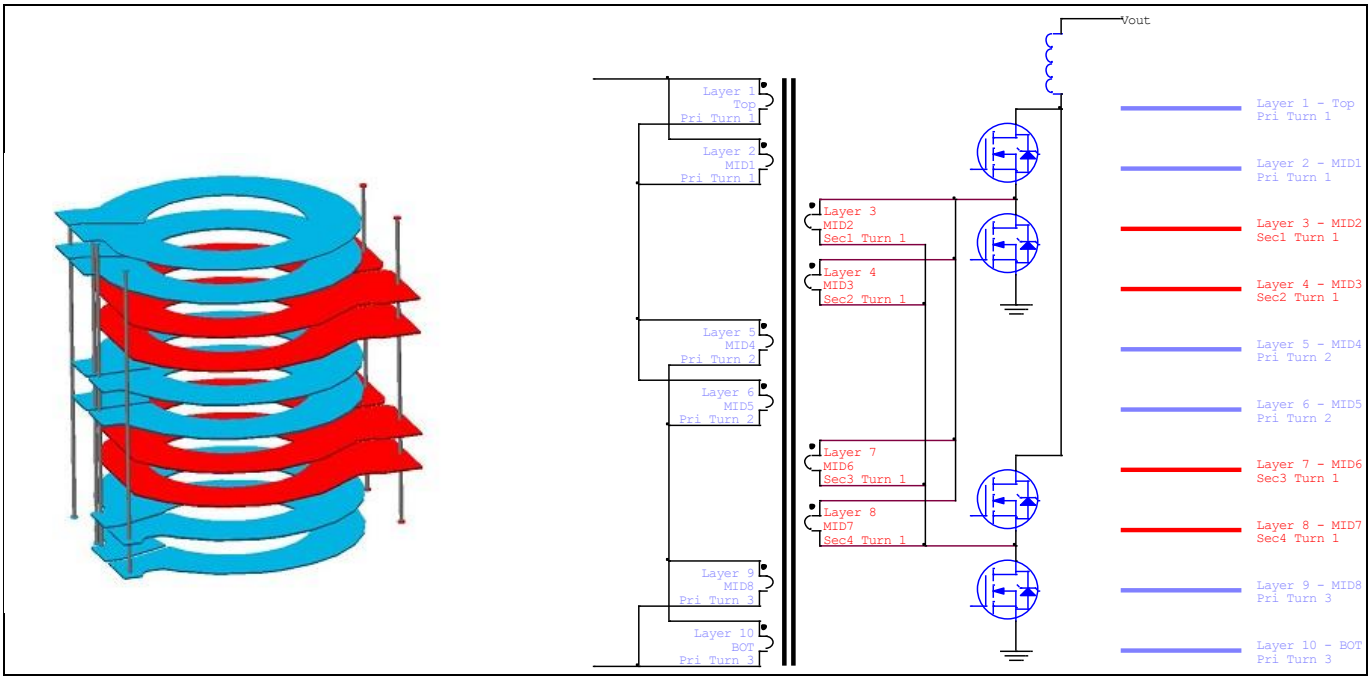


Figure 12 Planar transformer drawing

2.6 Bill of Materials (BOM)

Table 3 BOM

Item	Qty.	Ref.	Manufacturer	Part number
1	1	BRD1		P100106 A
2	8	C1,C2,C3,C4,C5,C6,C7,C8	TDK	C3225X7R2A225K230
3	19	C9,C10,C11,C12,C17,C19,C28,C29,C30,C34,C42,C43, C50,C52,C53,C54,C69,C72,C74	TDK	C1608X7R1H104K080
4	5	C13,C18,C20,C33,C47	TDK	C1608C0G2A101K
5	1	C14	TDK	C1608X7R1H103K080
6	2	C15,C16	TDK	C2012C0G2E472J125AA
7	2	C22,C79	TDK	C1608X7R1H223K080
8	1	C23	TDK	C2012X5R1E106K125AB
9	1	C24	TDK	C3225C0G1H104J
10	1	C25	TDK	C1608C0G2A471K
11	3	C26,C65,C73	TDK	C1608C0G2A472K
12	1	C27	Kemet	C1206C102JGR
13	5	C32,C57,C62,C70,C77	TDK	C1608C0G2A102J
14	6	C35,C36,C37,C38,C39,C40	TDK	C3225X7R1C226K250
15	1	C41	TDK	C2012X7R1C475K125
16	5	C48,C49,C56,C75,C76	TDK	C1608X7R1E105K
17	1	C58		Not used
18	1	C59		Not used
19	1	C60	Samsung	CL21B106KOQNNNE
20	1	C61	TDK	C0603C472K2RACTU
21	1	DS1	Wurth	150060GS75000
22	2	D1,D3	Diodes	B2100A-13-F
23	1	D2	NXP	BAT46WJ,115
24	1	D4	Toshiba	CRH01(TE85L,Q,M)
25	6	D5,D6,D9,D10,D12,D15	On	BAS20HT1G
26	1	D13	On	MM5Z5V1T1G
27	4	D16,D22,D23,D24	NXP	BAS516,135
28	1	J1	Harwin	M22-5320505
29	1	J2	Samtec	FTSH-102-05-L-DV
30	2	L1,L3	Taiyo Yuden	CBC3225T101KR
31	1	L2	Wurth	744355147
32	4	Q3,Q4,Q7,Q8	Infineon	BSC050N10NS5ATMA1
33	8	Q9,Q10,Q11,Q12,Q13,Q14,Q15,Q16	Infineon	BSC010N04LS6
34	2	RT1,RT2	Murata	NCP15WB473F03RC
35	2	R1,R93	Panasonic	Not used
36	1	R2	Panasonic	ERJ-3EKF5110V
37	1	R3	Yageo	RC1206FR-073R01L
38	7	R4,R5,R12,R16,R23,R32,R33	Panasonic	ERJ-3EKF1002V

Item	Qty.	Ref.	Manufacturer	Part number
39	2	R6,R18	Panasonic	ERJ-3EKF1202V
40	1	R7	Panasonic	ERJ-8ENF1000V
41	1	R9	Panasonic	ERA-3AEB103V
42	1	R10	Panasonic	ERA-3AEB112V
43	8	R11,R19,R35,R38,R39,R40,R78,R89	Panasonic	Not used
44	3	R13,R69,R96	Panasonic	ERJ-3EKF20R0V
45	1	R14	Panasonic	ERJ-3EKF3321V
46	3	R15,R65,R87	Panasonic	ERJ-3EKF2002V
47	2	R20,R68	Panasonic	ERJ-3GEY0R00V
48	7	R21,R22,R26,R28,R66,R70,R86	Panasonic	ERJ-3EKF1000V
49	1	R25	Panasonic	ERJ-3EKF1871V
50	1	R27	Panasonic	ERJ-3EKF3011V
51	4	R29,R30,R31,R67	Panasonic	ERJ-3EKF2001V
52	4	R34,R59,R62,R71	Panasonic	ERJ-3EKF1001V
53	1	R36	Panasonic	ERJ-3EKF2213V
54	1	R37	Panasonic	ERJ-3EKF4871V
55	12	R41,R42,R43,R45,R46,R49,R50,R53,R54,R55,R56, R63	Panasonic	ERJ-3RQF1R0V
56	1	R47	Panasonic	ERJ-3EKF8871V
57	1	R48	Panasonic	ERJ-3EKF1371V
58	1	R57	Panasonic	ERJ-3EKF1243V
59	1	R58	Panasonic	ERJ-3EKF3320V
60	1	R72	Panasonic	ERJ-3EKF1272V
61	1	R73	Panasonic	ERJ-3EKF51R1V
62	1	R74	Panasonic	ERA-3AEB104V
63	1	R75	Panasonic	ERA-3AEB132V
64	1	R85	Panasonic	ERJ-6ENF2002V
65	10	TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10	Harwin	S2761-46R
66	1	T1	Ferroxcube	EQ25-3F36 and PLT25/18/2-3F36
67	1	T2	Ice	CT02-100
68	1	T3	Coilcraft	LPD5030V-224MR_B
69	1	U1	Infineon	XDPP1100-Q040
70	4	U2,U3,U4,U5	Infineon	2EDF7275K
71	1	U10	TI	OPA140AIDBVT
72	1	U11	TI	LM5018SD/NOPB
73	1	U20	LT	LT1460KCS3-3.3#TRMPBF
74	1	U21	Fairchild	FODM8801A
75	3	1,2,3	Mil Max	3104-3-00-15-00-00-08-0
76	2	5,9	Mil Max	4357-0-00-15-00-00-03-0

3 Configuration

The FW patch and optimized configuration are stored in the non-volatile memory OTP. The user could run the demo board without needing additional configuration by following the instructions in section 2.3. To evaluate the XDPP1100, the user could change configurations such as fault thresholds or response. Most of the configurations can be changed on the fly. The modified configurations are stored in the RAM and can be modified unlimited times. On the other hand, the modifications will be lost and reset to the default OTP settings once the input voltage and 3.3 V VDD are removed. To keep the new configuration, the user could store the customized configuration to the OTP. Please refer to the XDPP1100 configuration guide. The “Force i2c/PMBus OK” is not mandatory, as the demo board is shipped with a stored product ID that recognizes the device by using “Auto populate”. Loading the design file QB_FBFB_VMC_XDPP1100 is recommended if the user want to verify the design tool “PID – Bode Plot”. This is because the load models are not stored in OTP and won’t be read by the “Auto populate”. The design file will provide the information of the load model (such as the output capacitance and ESR) for bode plot emulation.

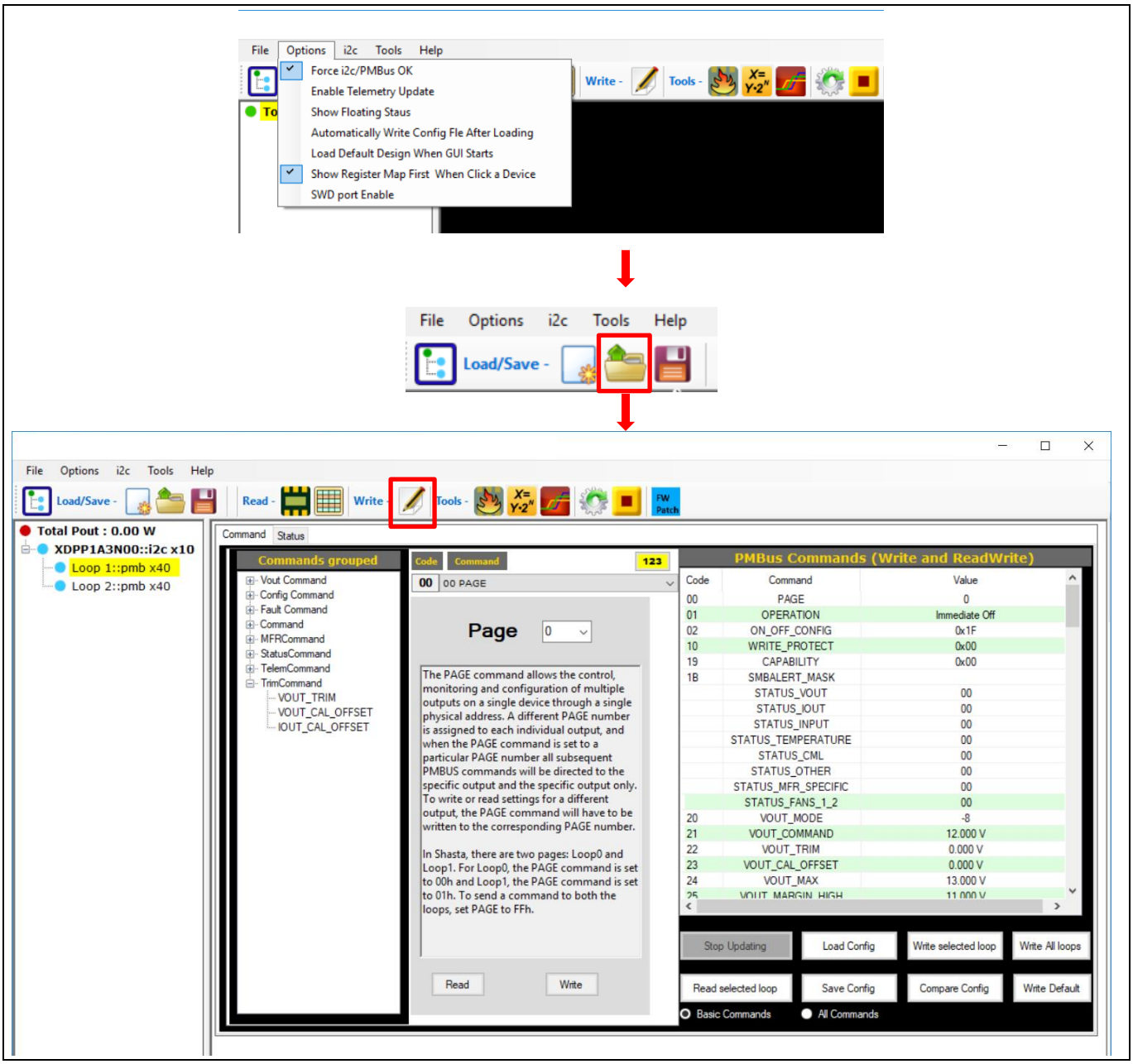


Figure 13 Load design file through GUI and write to the device

The key PMBus commands are listed in **Table 4**. The output voltage is sensed at the VSEN pin through resistor-divider R9, R10. The set-point of VSEN is recommended to be set equal or higher than 1.2 V for the highest accuracy. This demo board sets the divider ratio to 0.099 to get 1.2 V at the VSEN pin.

3.1 PMBus configuration

Table 4 Basic PMBus configuration (Loop0, except command 0xEA)

Command	Name	Data	Meaning
00	PAGE	00	0
01	OPERATION	00	Immediate off
02	ON_OFF_CONFIG	1F	Respond to operation and EN pin, EN polarity active high
20	VOUT_MODE	14	-12
21	VOUT_COMMAND	0C00	12,000 V
24	VOUT_MAX	0D00	13,000 V
27	VOUT_TRANSITION_RATE	E850	10,000 mV/µs
29	VOUT_SCALE_LOOP		0.09961
32	MAX_DUTY	F180	96.00 percent
33	FREQUENCY_SWITCH	087D	250 kHz
34	POWER_MODE	03	0x03
61	TON_RISE	F050	20.000 ms
CD	MFR_VRECT_SCALE		0.07227
CE	MFR_TRANSFORMER_SCALE		0.333
EA (Loop0)	MFR_IOUT_APC (defines ISEN gain for I_{IN})		0.0996 A (not used in VMC)
EA (Loop1)	MFR_IOUT_APC (defines BISEN gain for I_{OUT})		0.359375 A

The XDPP1100 is compliant with PMBus Power System Management Protocol Specification, revision 1.3.1. The standard PMBus commands are not going to be explained here. The Infineon MFR PMBus commands are described in this section.

3.1.1 0xC5 FW_CONFIG_REGULATION

FW_CONFIG_REGULATION (**Figure 14**) configures multi-segment droop parameters and flexible start-up/shutdown functions.

The function of flexible start-up and shutdown includes:

- CURRENT_DOUBLE_ENABLE: Enable secondary current doubler configuration
- EN_BOOST_FEED_FORWARD: Enables feed forward calculation from firmware for buck-boost topology, reserved for future use and not recommended for current designs
- EN_DE_SHUTDOWN: Enable diode emulation mode (disable SR) during soft-off
- EN_IOUT_APC_TEMP_COMP: Enable temperature compensation of current sense
- INTERLEAVE_ENABLE: Enable interleave
- EN_DEADTIME_ADJ: Enable change dead-time per load current (not implemented in ROM code, but could be implemented by FW patch. Example patch code is available on request)

Configuration

- EN_VSEN_OPEN_PROTECT: Enable voltage sense pin short/open protection at start-up (not implemented; the open sense fault is enabled by setting the open sense threshold vspX_osp_thresh to non-zero value)
- EN_L_ESTIMATE: Enable inductance estimation at start-up (not implemented)
- EN_C_ESTIMATE: Enable output capacitance estimation at start-up (not implemented)
- EN_ILIM_STARTUP: Enable current limit at start-up
- EN_PID_ADJ: Enable PID adjustment at start-up (not implemented)
- EN_PRIM_ISENSE: Enable BISEN on top of ISEN current sense. It should be enabled in this design to use BISEN in Loop0. In this design, BISEN is used to sense output current. The output current sense gain and offset should be configured in Loop1 by using MFR_IOUT_APC and IOUT_CAL_OFFSET
- EN_DE_STARTUP: Enable diode emulation mode (disable SR) during soft-start

Note that “not implemented” indicates the function or feature is not implemented in the ROM code. The features are reserved to be implemented via FW patch.

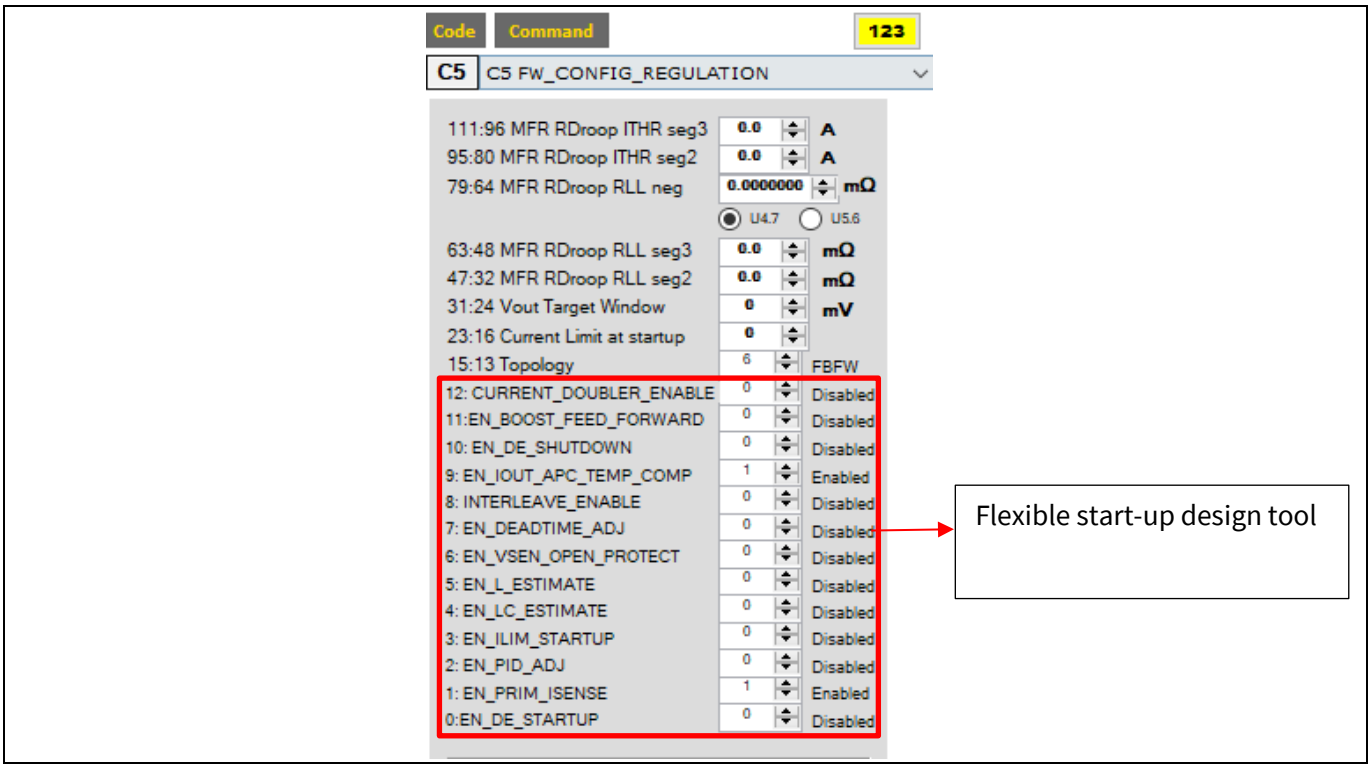


Figure 14 FW_CONFIG_REGULATION

Vout Target Window (bit 31:24): Defines the SR enabling threshold during DE start-up. If EN_DE_STARTUP is set to 1, the SR gate will be held low during soft-start until output voltage approaches target V_{OUT}. The SR gate will be enabled at VOUT_COMMAND minus Vout Target Window.

Current limit at start-up (bit 23:16): defines start-up clamping current in amps.

This demo board uses PCB copper trace to sense output current. To compensate for the temperature drift of the copper resistance, set bit [9] to 1. This enables the adjustment of IOUT_APC (see 3.1.7) based on the temperature that is obtained by READ_TEMPERATURE_1 (see 3.1.8). The temperature is compensated with a fixed coefficient 0.0039. User-defined temperature coefficient is possible by FW patch.

3.1.2 0xCA MFR_IOUT_OC_FAST_FAULT_RESPONSE

The MFR_IOUT_OC_FAST_FAULT_RESPONSE command instructs the device on what action to take in response to a fast output over-current fault (when exceeding 0xD1 MFR_IOUT_OC_FAST_FAULT_LIMIT). Unlike the regular I_{OUT} OC fault response, the I_{OUT} OC fast fault response only supports two types of response: “continuous to operate (constant current)” and “shut down and retry”.

3.1.3 0xD1 MFR_IOUT_OC_FAST_FAULT_LIMIT

This command defines the threshold of fast over-current protection. Similar to the regular over-current protection, this protection is also based on output average current, but with no filter to the signal, so it could act faster. This limit should be set higher than the regular OC fault threshold IOUT_OC_FAULT_LIMIT for short-circuit protection.

The fast over-current fault response is configured by PMBus command 0xCA MFR_IOUT_OC_FAST_FAULT_RESPONSE.

3.1.4 0xCD MFR_VRECT_SCALE

MFR_VRECT_SCALE is calculated based on V_{rect} resistor-divider (R71, R72, R11).

$$MFR\_VRECT\_SCALE = \frac{1\ k\Omega}{(12.7\ k\Omega + 1\ k\Omega)} = 0.07299$$

3.1.5 0xCE MFR_TRANSFORMER_SCALE

MFR_TRANSFORMER_SCALE is the transformer turns ratio, equal to Ns/Np. Here Np = 3, Ns = 1.

3.1.6 0xCF PWM_DEADTIME

Dead-time can be set in the device Topology tool (**Figure 15**) or by PMBus command 0xCF PWM_DEADTIME (**Figure 16**). Dead-time is set by adding a delay to the rising edge or falling edge of each PWM output. The dead-time of PWM rise and fall time can be configured separately. In most situations only dead-time at the rising edge needs to be set. The maximum dead-time can be set to 318.75 ns with a resolution of 1.25 ns. When setting dead-time, please consider the isolator delay that will be added to the primary PWMs, making the real gate waveform shift to the right.

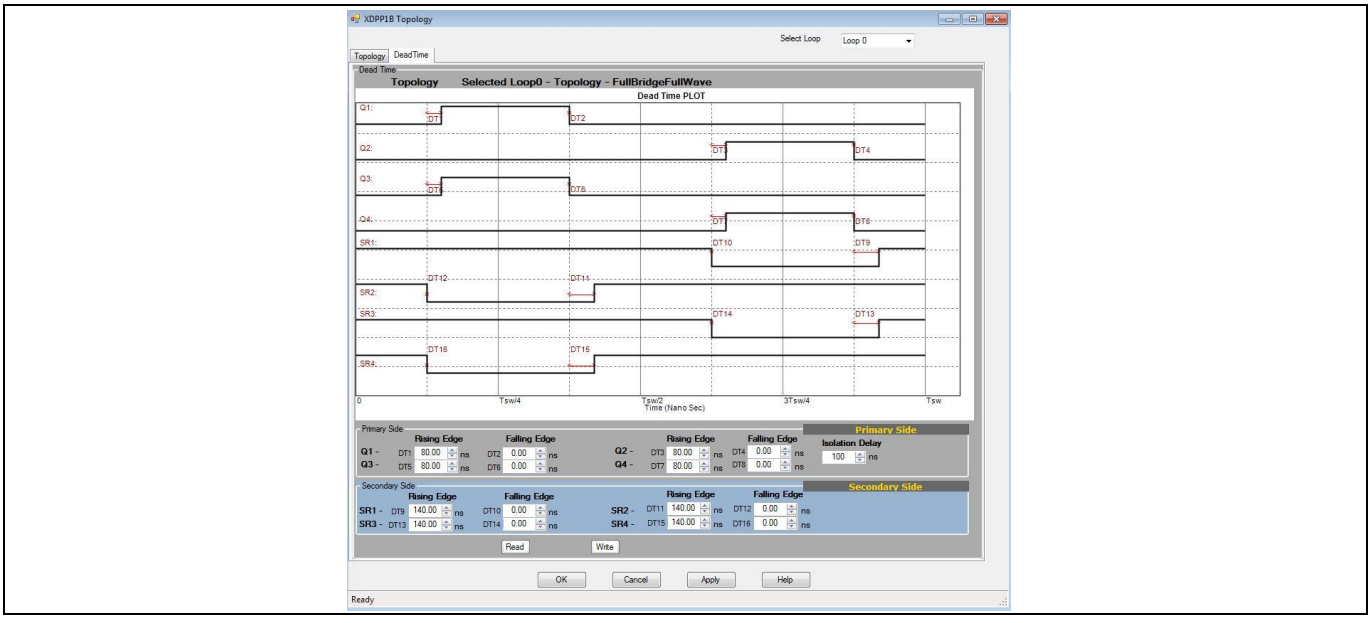


Figure 15 Topology tool – set dead-time

Figure 16 shows using PMBus command 0xCF PWM_DEADTIME to configure dead-time. Only the active PWMs in the selected loop can be configured and they are highlighted by a different color.

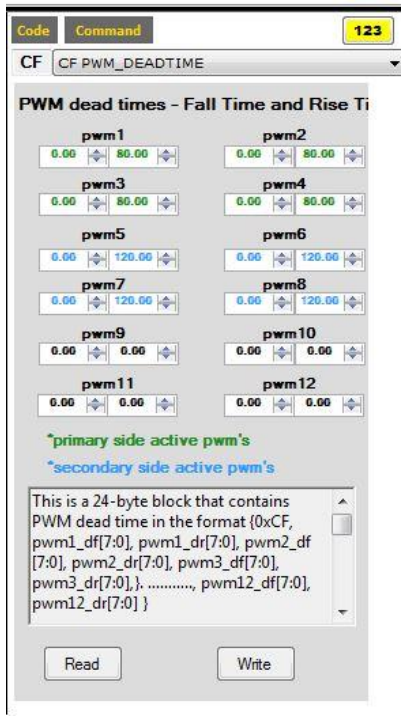


Figure 16 PWM_DEADTIME command

3.1.7 0xEA MFR_IOUT_APC

MFR_IOUT_APC (Amps Per Code) defines the current sense gain. The calculation of MFR_IOUT_APC:

MFR_IOUT_APC = ISEN_LSB/Rsns

The ISEN_LSB is the resolution of IADC which is determined by the isenX_gain_mode register. XDPP1100 offers two levels of gain: 100 µV and 1.45 mV, which reference to ground (GND); and one IPS mode, which has a resolution of 1.45 mV and references to a DC bias range from 1.11 V to 1.6 V. The gain mode is configured by register isen_gain_mode. In this demo, the ISEN_LSB is set to 1.45 mV (isen1_gain_mode=2).

The secondary current is sensed by PCB copper trace (0.13 mΩ). The signal is very small and an external op-amp (U10) is used to amplify the signal with a gain of 201. The signal is then divided by R67, R58 at the input of XDPP1100 with a ratio of 0.1423. Thus the equivalent secondary sense resistor is 0.13 x 201 x 0.1423 = 3.72 mΩ. The secondary IOUT_APC = 1.45 mV/3.72 mΩ = 0.389 A.

Please note that the PCB trace resistance varies from board to board across a wide range. The IOUT_APC of each board should be calibrated per the actual measurement, and the value varies from board to board.

3.1.8 0xDC MFR_SELECT_TEMPERATURE_SENSOR

Use MFR_SELECT_TEMPERATURE_SENSOR to configure the temperature sensor. The XDPP1100 supports both external temperature sensing and internal temperature sensing for protection and monitoring. External temperature sensing is performed with a 47 kΩ NTC thermistor, in parallel with a 12 kΩ resistor connected between ATSEN or BTSEN and ground.

This demo uses ATSEN to sense PCB temperature near the CS copper shunt. It is used to compensate for the current sense resistor value changing with temperature. This temperature sensor must be mapped to READ_TEMPERATURE_1 for temperature compensation.

The board uses BTSEN to sense the PCB copper temperature near the SR MOSFET for over-temperature protection. Use the “Fault source select” drop-down menu to choose tempb as the fault source.

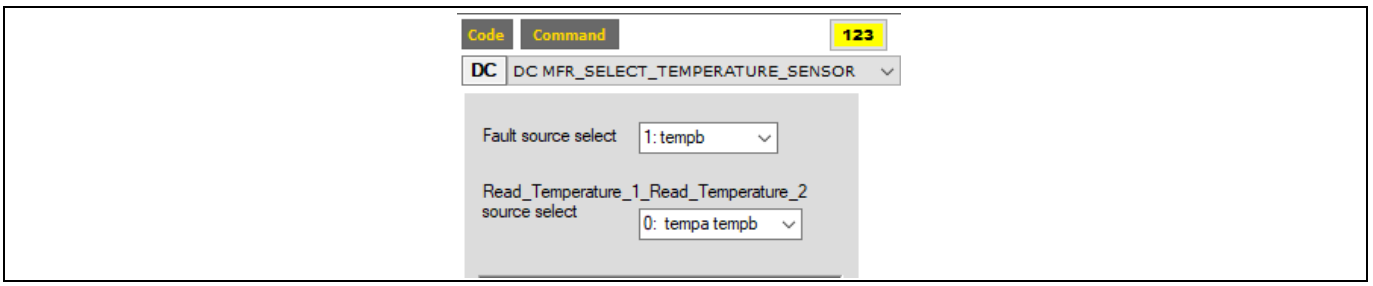


Figure 17 MFR_SELECT_TEMPERATURE_SENSOR

3.2 Register configuration

The XDPP1100 GUI provides the necessary design tools for the user to configure the registers. In the XDPP1100 GUI, go to the “Design Tools” tab and follow the design tool steps from 1 to 7 (**Figure 18**).

Some key parameters are configured as follows.

Table 5 FBFB_VM register set-up

Register name	Value	Register name	Value
ce1_ktrack_hiz	1	ramp0_m_flavor	2 (trailing-edge modulation)
ce1_ktrack_off	4	ramp0_half_mode	1
ce1_ktrack_on	4	ramp0_min_pw_state	0
ce1_kslope_didv	659	mode_control_loop0	0 (VMC)
ce1_pwmwin_dly	3	ramp0_dutyc_lock	1 (enable flux balancing)
ce1_ladj_en	1	ramp0_dc_max_nom	0
ce1_ps_current_emu	0	vsp1_vrs_sel	1
ce1_dt_l_slope	7	vrs_cmp_ref_sel	0
ce1_blank_ne_dly	0	vrs_cmp_wdt_thr	25
ce1_blank_pe_dly	0	vrs_track_start_thr	50
ce1_kslope_lm	0	vrs_voltage_init	58
pid0_kfp1_index_1ph	36	ki_fbal	30
pid0_kfp2_index_1ph	35	kp_fbal	8
pid0_kp_index_1ph	39	fbal_max	20
pid0_ki_index_1ph	25	fbal_time_only	0
pid0_kd_index_1ph	60	fbal_dcm_thresh	26
pid0_ff_vrect_override	924	ical_en	1
pid0_ff_override_sel	0	tlm0_iout_src_sel	1
pid0_ff_vrect_sel	0	tlm0_iin_src_sel	2

The design file that comes with the demo board has the optimized configuration. To verify or change the parameters, the user can go to each design tool and modify the registers. This section shows examples of the design tools. For more details please refer to the XDPP1100 configuration user guide.

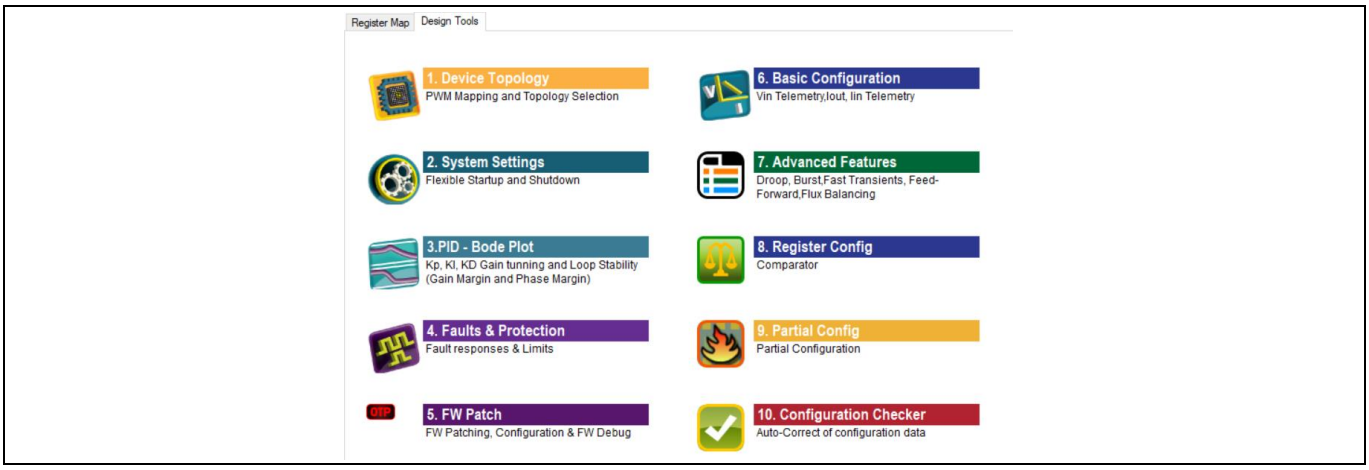


Figure 18 GUI design tools

3.2.1 Loop PID configuration

The loop PID coefficient should be configured by using the number 3 PID – bode plot design tool.

Figure 19 shows the PID design tool and parameters of the demo board in VMC. The user can tune Kp, Ki, Kd and the two low-pass filter bandwidths to obtain the desired gain and phase margin. The design tool shows the bode plot based on the load model and the compensation. The tool also helps the user determine the PID parameters if the load model is provided. Please note that an accurate load model is required for the correct bode plot. The critical parameters are output inductor value L, output capacitor value and ESR, input voltage V_{IN}, output voltage V_{OUT} and output current I_{OUT}. Once the load models are entered, go to the bode plot page and place the desired poles and zeroes in the right-hand side table, then click <== to calculate the PID compensation parameters.

In general, the two zeroes could be placed at the double-pole of the output LC filter, and pole 1 can be placed at half of the switching frequency. Once the tool has calculated the PID, use the ==> to view the adjusted poles and zeroes.

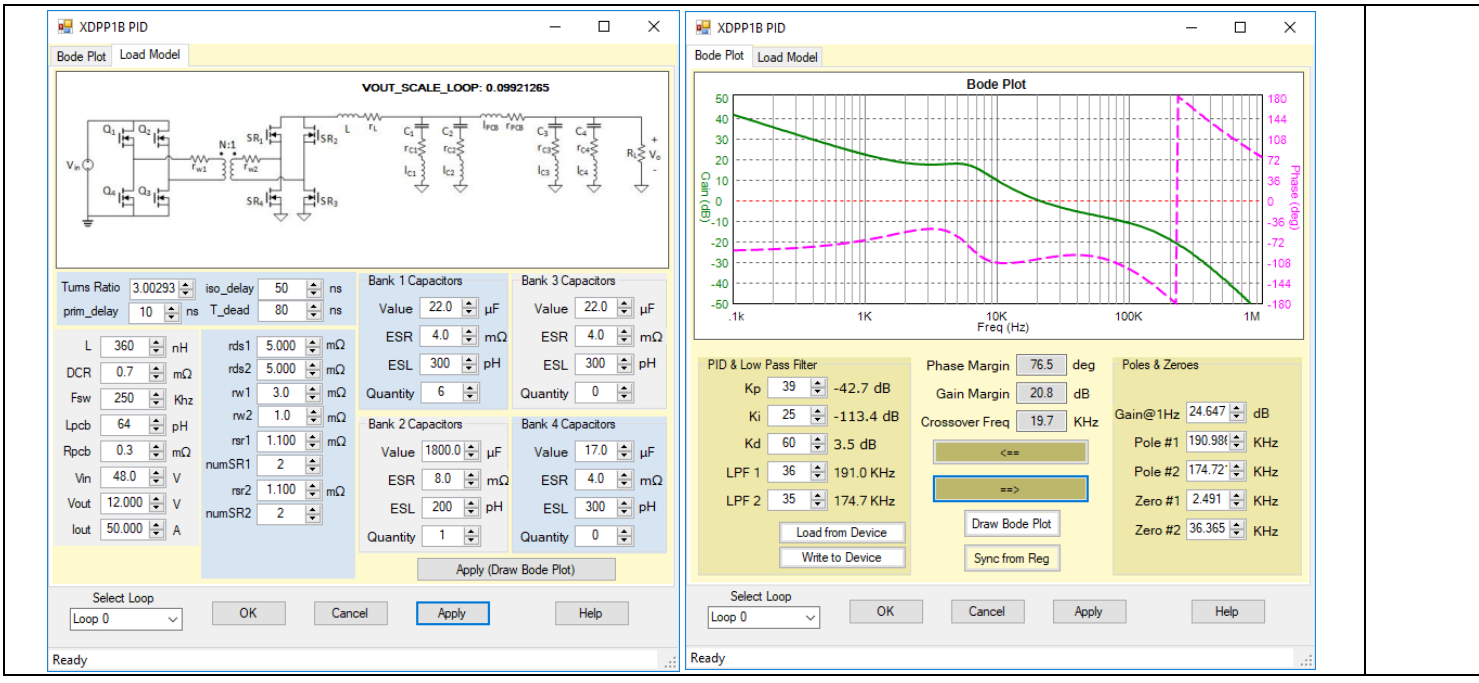


Figure 19 PID – bode plot design tool

3.2.2 Output and input current sense configuration

Output current, input current, input voltage and PWM/ramp are configured by design tool 6, Basic Configuration. **Figure 20** shows the output current sense configuration. Please select the source of current sense to start. For example, in this design the output current is sensed by BISEN, therefore “ISP2 (BISEN)” is selected.

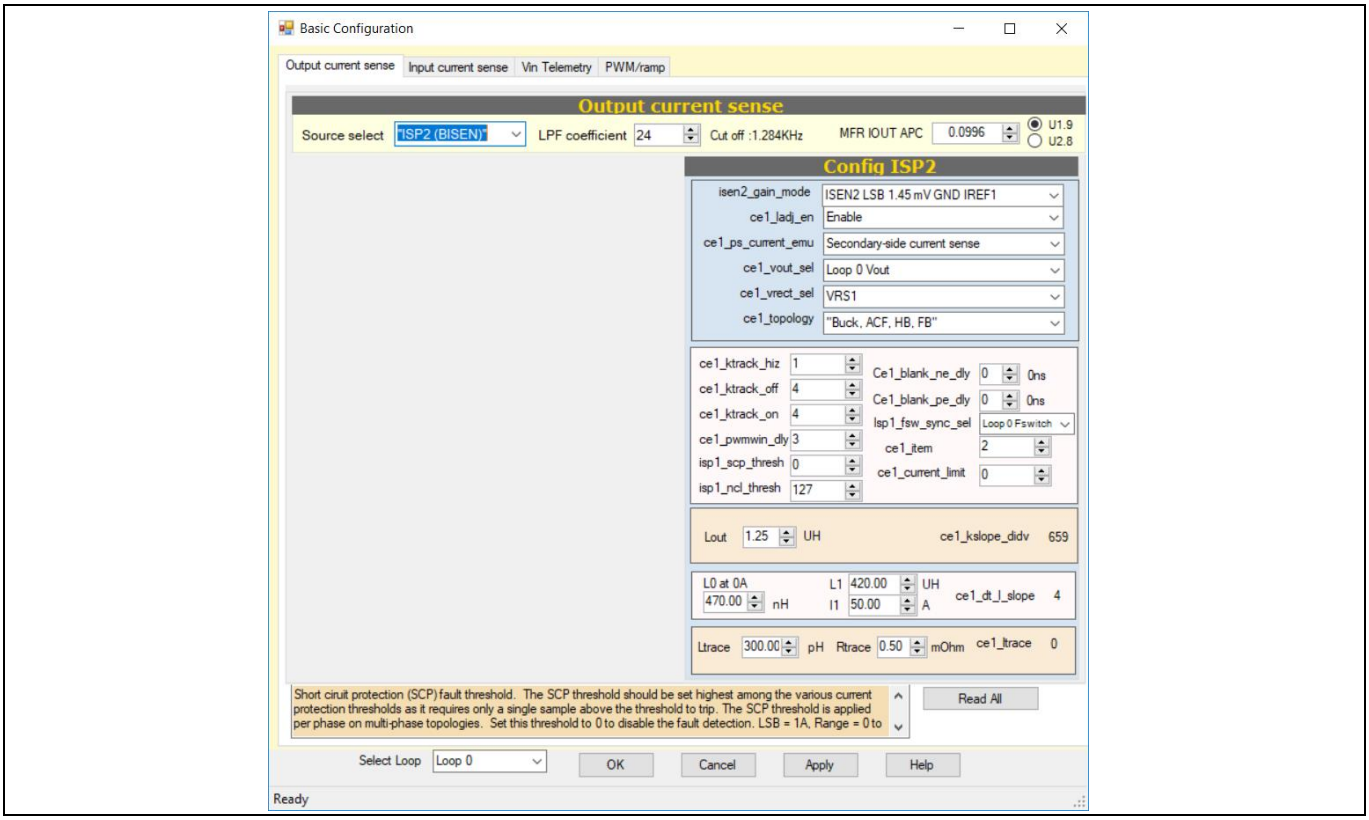


Figure 20 Output current sense configuration tool

- The ktrack registers are used to set the track gain of the current estimator. The value of ktrack gain can be set in a range of 0 to 15. When set to 0, the current estimator will not track to ADC sensed current but will fully rely on estimation, which is calculated based on voltage and inductor value (ce_kslope_didv). When ktrack gain is set to 15, the current estimator uses the actual sensed current. Other values set the weight of sensed current over the estimated current with a ratio of x/15.
- kslope_didv defines the output inductor current slope. It is calculated based on I_{OUT_APC} and L_{OUT} value.

  For output current sense:

  $$ce0\_kslope\_didv = \frac{1(V)\cdot 10(ns)}{Lout(nH)\cdot APC\ (\mathrm{A})} \times 2^{13}$$

- kslope_lm defines the primary magnetizing current slope. It should be 0 for secondary current sense. Thus it is not listed in the “Output current sense” tool. For the primary PCMC, this register is configured in the “Input current sense” tool.

  $$ce0\_kslope\_lm = \frac{1(V)\cdot 10(ns)\cdot \frac{Np}{Ns}}{Lm(nH)\cdot APC\ (A)} \times 2^{13}$$

  $ce0\_kslope\_didv = \frac{1(V)\cdot 10(ns)}{Lout(nH)\cdot APC\ (A)\cdot \frac{Np}{Ns}} \times 2^{13}$, for primary current sense, the secondary current ripple is mapped to primary with a ratio of Np/Ns, configured by the “Input current sense” tool.

- ce0_pwmwin_dly defines the PWM window delay, used to align the internal PWM signal to incoming current sense waveform. Delay time is defined by (ce0_pwmwin_dly + 1) * 10 ns.
- ceX_blank_ne_dly and ceX_blank_pe_dly defines the leading-edge blanking time for the current sense at the negative edge and positive edge of PWM. The blanking time can be set between 0 ns and 280 ns.
- ceX_dt_l_slope defines the output inductor derating slope. If the inductance droops with instantaneous current, the current estimator adjusts the di/dt slope accordingly.
- ceX_ltrace compensates for the parasitic inductance of the current sense resistor.

When the converter is configured in VMC, the input current telemetry can only be selected as “estimated input current” based on I_{OUT}. The register tlm0_iin_src_sel should set to 2.

3.2.3 Input voltage sense and feed-forward configuration

The XDPP1100 uses VRSEN/VRREF ADC to sense the input voltage from the secondary side of transformer V_{rect} through the resistor-divider R71, R72. The input voltage is calculated based on the sensed VRSEN voltage, the V_{rect} resistor divider ratio, and the transformer turns ratio.

Figure 21 shows how the sampling of the V_{rect} waveform work. Noise has been added to the ideal VRSEN waveform to highlight the importance of sampling window timing.

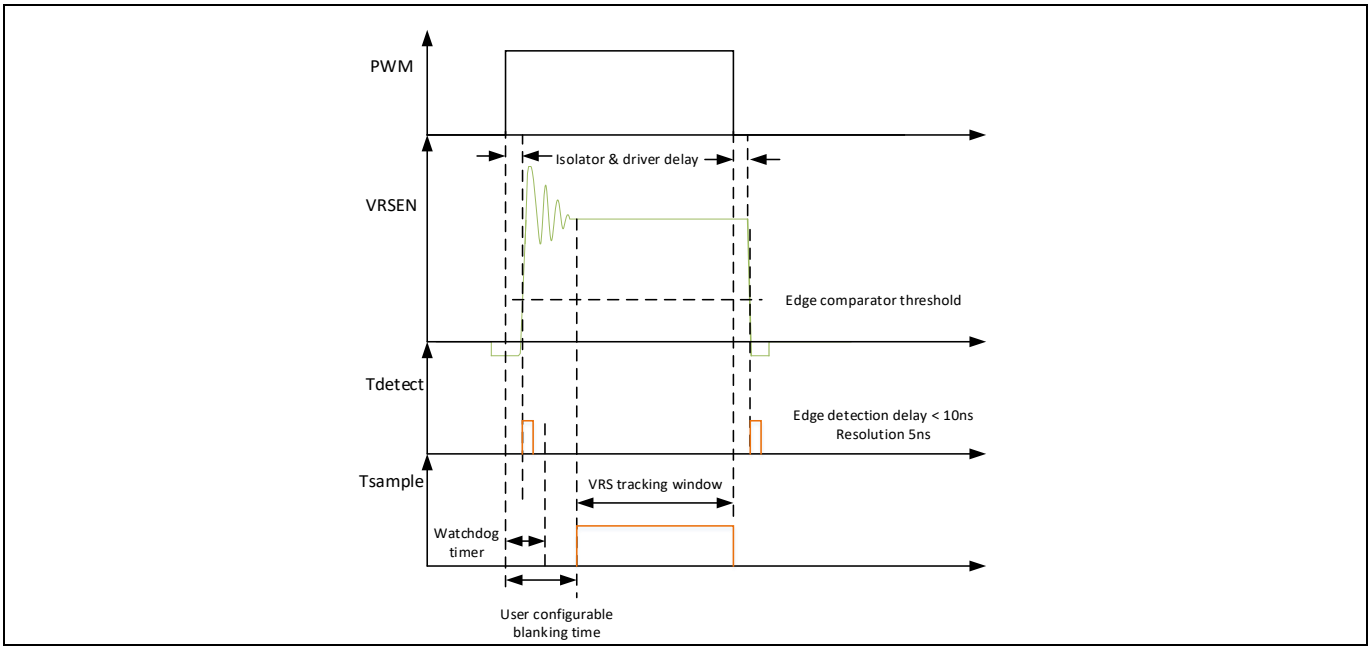


Figure 21 Timing of V_{rect} sensing by VRSEN

The VRS edge detector works at 200 MHz clock. It senses the rising and falling edges of V_{rect} waveform with delay less than 10 ns. T_{detect} waveform is the output of edge detector logic. The rising edge of the rectified voltage waveform is detected and a programmable blanking window is added to it. The blanking time should be configured as longer than the voltage spike and ringing duration. The blanking time should also be set longer than 250 ns for the tracking ADC to settle (vrs_track_start_thr register).

The edge comparator has two configurable reference voltage thresholds: 500 mV and 300 mV, defined by register vrs_cmp_ref_sel. The user can choose a proper threshold based on the VRSEN signal level. To optimize VRSEN accuracy, it is recommended to scale V_{rect} voltage to VRSEN in the 600 mV to 2.1 V range. In this design, the V_{IN} under-voltage fault threshold is 30 V, V_{IN} over-voltage fault threshold is 80 V; transformer turns ratio is 3:1. V_{rect} amplitude spans from 10 V to 27 V between the two V_{IN} fault limits. Setting the V_{rect} resistor-divider ratio to 0.07 scales V_{rect} to 0.7 V~1.89 V, nicely fitting into the VRSEN input voltage range.

Configuration

After the blanking window, sampling of the rectified voltage can occur (shown as the T_{sample} waveform). The sampling window ends when the associated PWM signal goes low. If input voltage changes during this period, VRS ADC tracks the change. At the end of a sampling window, VRS ADC remembers the value of the last ADC sample and uses this value for the feed-forward computation for the next switching cycle.

At start-up, prior to PWM switching, the FF is computed with an initial voltage that is configured by the register vrs_voltage_init. The initial input voltage is typically set to nominal input voltage per application.

The FF computation is implemented in hardware and thus offers the fastest response. The XDPP1100 computes FF duty-cycle based on input voltage and output voltage, and the result is added to the feedback loop PID filter output to resolve PWM duty-cycle (**Figure 22**).

$$computed\_feed\_forward = \frac{Vout,target}{Vin \times trans\_scale\_loop}$$

Here, trans_scale_loop is the transformer turns ratio, defined by N_S/N_P in full-bridge or active clamp forward topologies, and $N_S/(2N_P)$ in a half-bridge topology. Wherein N_P is the transformer primary turns number, and N_S is the transformer secondary turns number. The user can define the transformer scale by PMBus command MFR_TRANSFORMER_SCALE (N_S/N_P) for all isolated topologies. The XDPP1100 FW will calculate the trans_scale_loop based on MFR_TRANSFORMER_SCALE command and device topology. FW takes care of factor 2 for the half-bridge topology, and the user should not be concerned with setting it manually.

The register pid_ff_vrect_sel selects the FF input source. In this demo board, VRSEN is used for the FF computation.

$$computed\_feed\_forward = \frac{Vout,target}{Vrect}$$

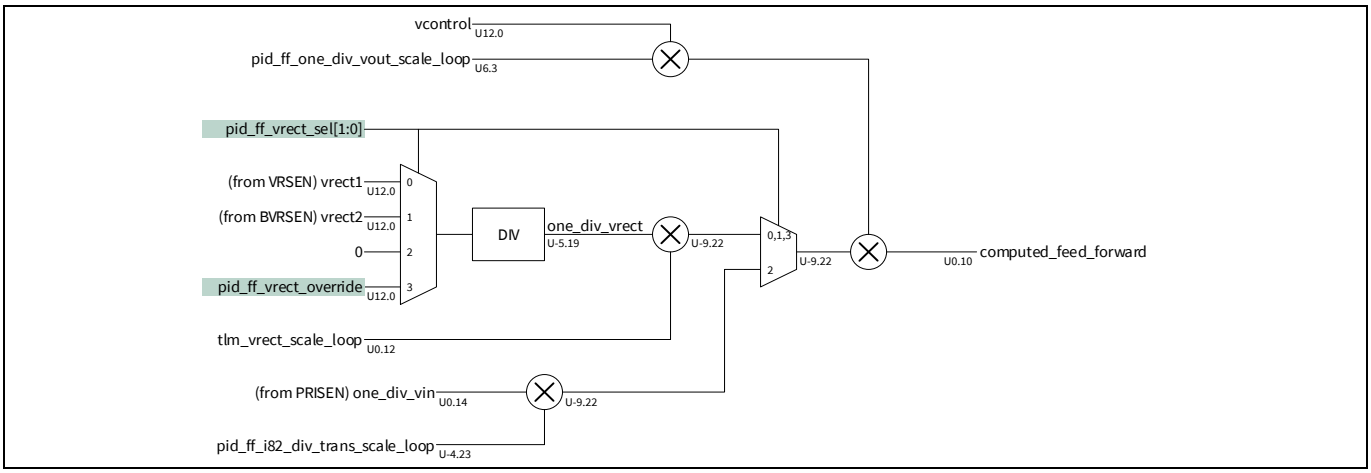


Figure 22 XDPP1100 FF computation

The user could configure the FF registers by using GUI design tool 7 “Advanced features”, “Feed-forward” tab (**Figure 23**).

More details of input voltage sensing and feed-forward can be found in the XDPP1100 application note.

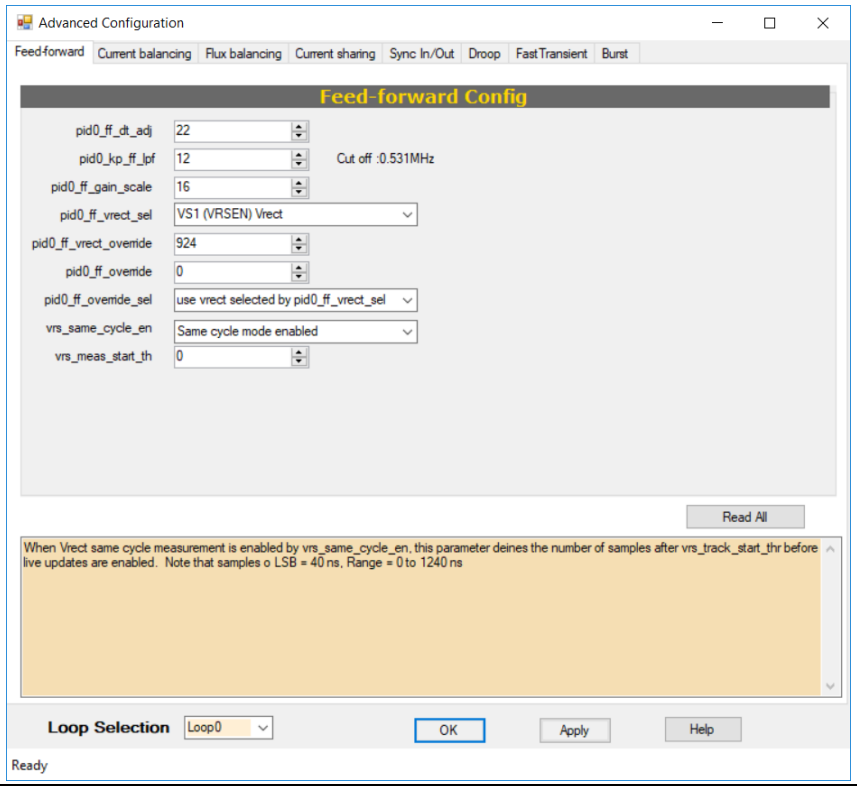


Figure 23 Feed-forward configuration tool

In a pre-bias start-up situation, the error between the initial voltage and the actual input voltage could cause small glitch on the output voltage at start-up, especially at low-line (36 V) or high-line (72 V). This is because the FF duty-cycle is computed based on the initial voltage, not the actual input voltage. When the input voltage is higher than the initial voltage, output voltage has overshoot. **Figure 45** shows pre-bias start-up waveform at 72 V input while the initial voltage is set to 48 V; 1.7 V overshoot is observed on the V_{OUT} waveform.

To reduce the voltage glitch, this demo board added another channel to sense the input voltage. The input voltage is sensed at the output of the auxiliary transformer and is fed to the PRISEN pin and TS ADC input (**Figure 24**). The voltage at the PRISEN pin is proportional to the input voltage as long as the bias power supply is regulated. The PRISEN input voltage sensing is configured by register vin_pwl_slope and vin_trim.

The vin_pwl_slope can be calculated by the following equation:

$$vin\_pwl\_slope = \frac{\Delta Vin \times 1.2 \times 2^5}{\Delta VPRISEN}$$

Transformer T3 in **Figure 24** has a 1:1 turns ratio. The voltage across capacitor C61 equals the input voltage. The ΔV_{PRISEN} /ΔV_{IN} is the resistor scale of the PRISEN resistor-divider (R74, R75). To utilize the full input voltage range of TS ADC (1.2 V), it is recommended to set the scale of V_{IN} resistor divider by:

$$\frac{1.2V}{Vin\_max}$$

For example, for maximum 95 V input the V_{IN} resistor-divider ratio is set to 1.2 V/95 V = 0.0126 V/V. To get this ratio, select R74 = 100 kΩ, R75 = 1.3 kΩ; the actual divider ratio is 0.01283.

$$vin\_pwl\_slope = \frac{1.2 \times 2^5}{0.01283} = 2993$$

The vin_trim configures the offset of the input voltage that is sensed by PRISEN.

With the PRISEN circuit, the XDPP1100 could sense input voltage prior to enabling the main power stage. The FW is patched to write vrs_voltage_init based on the PRISEN sensed input voltage at the time when the converter is enabled; the FF duty-cycle is calculated with actual input voltage, and thus eliminates the glitch on V_{OUT}.

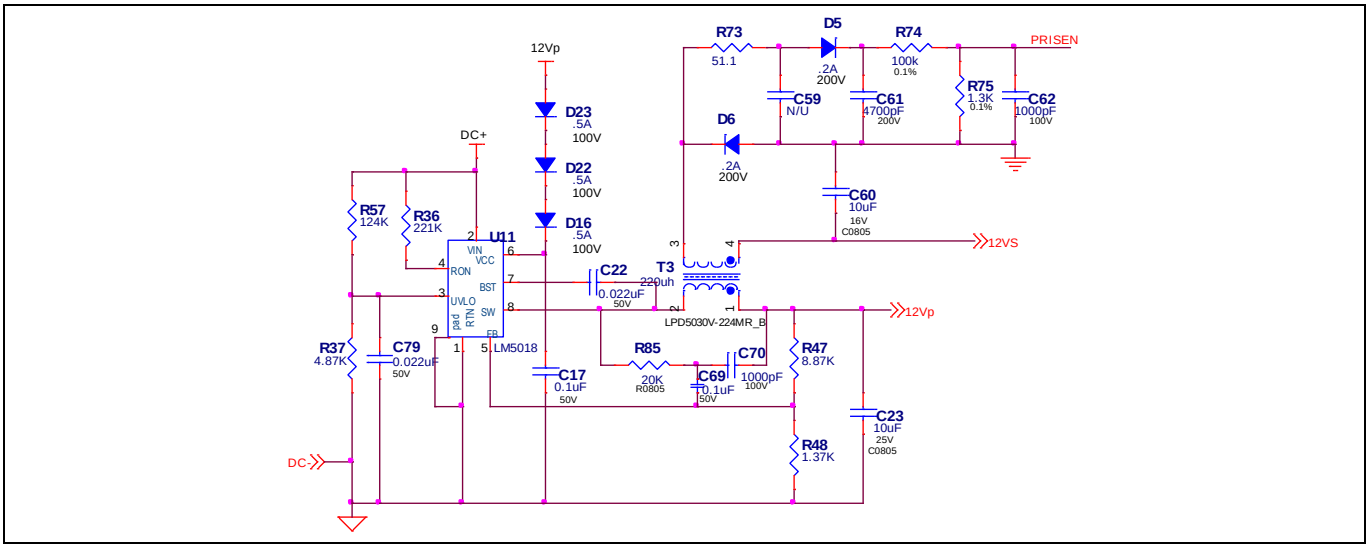


Figure 24 Input voltage sensing by PRISEN pin

During regulation, the input voltage telemetry and protection are sensed by VRSEN. VRSEN ADC has much higher performance than the TS ADC (PRISEN), provides greater accuracy and much faster FF response and fault protection. PRISEN telemetry is only activated before switching starts or after shutdown.

Table 6 VRSEN vs. PRISEN

	ADC	Sample rate (Msps)	Resolution (mV)	Range (V)
VRSEN	11-bit	50	1.25	0 to 2.1
PRISEN	9-bit	1	2.344	0 to 1.2

The user can use the GUI design tool 6 “Basic configuration”, “Vin Telemetry” tab to configure the input voltage sensing. Please note, the input voltage souce tlm0_vin_src_sel is set to 3 (TS ADC V_{IN}) for pre-start-up V_{IN} telemetry and protection. Once the converter starts switching, FW switches the input voltage source to VRSEN (tlm0_vin_src_sel = 0). It switches back to TS ADC V_{IN} sense when the converter shuts down.

3.2.4 Flux balancing configuration

The flux balancing should be configured in design tool 7 “Advanced features”, as shown in (**Figure 25**). The XDPP1100 implements flux balancing by maintaining volt-second balance in each half-cycle. The voltage and timing are measured from the transformer secondary winding by the VRSEN pin. The error between the volt-second product of each half-cycle is fed to a PI compensation network for duty-cycle adjustment.

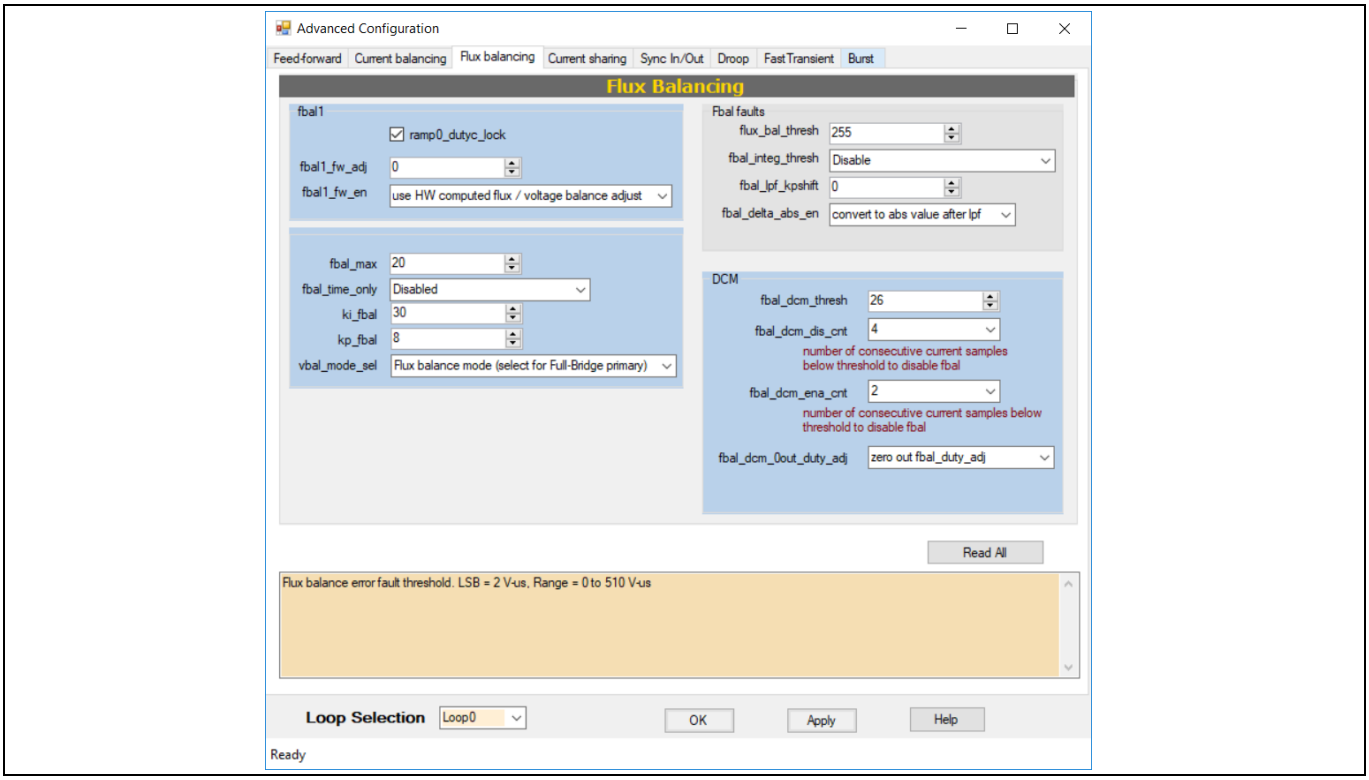


Figure 25 Flux balancing configuration

The XDPP1100 allows the user to select balance mode per the following configuration. The “voltage balance” adjusts the odd duty-cycle only based on the voltage of the odd and even cycles. The “time only balance” will adjust odd duty-cycle only based on the pulse width of the odd and even cycles. To enable flux balance (volt-second balance), vbal_model_sel and fbal_time_only should be set to 0.

The “voltage balance” can be selected in half-bridge applications. The “time only balance” is useful when the voltage sense is not accurate due to parasitic ringing that appears on the V_{rect} waveform. It could ignore the voltage mis-match and only corrects the timing mis-match.

Table 7 Volt-second balance mode

Balance mode	Register name	Value
Voltage balance	vbal_mode_sel	1
Flux balance (volt-second balance)	vbal_mode_sel	0
	fbal_time_only	0
Time only balance	vbal_mode_sel	0
	fbal_time_only	1

3.2.4.1 Maximum limit of duty-cycle correction

The fbal_max register limits the maximum duty-cycle correction applied by the flux balance filter. The LSB of this register is 2^-10, and the range is from 0 to 24.902 percent.

For example, a full-bridge converter has a switching frequency of 250 kHz. The estimated maximum timing mis-match is 40 ns. Expected maximum timing correction is 80 ns, which is 2 percent duty-cycle. Then fbal_max should be set to 20 for 2 percent maximum limit.

$$f\_bal\_max = \frac{2\%}{2^{-10}} = 20$$

Please note, setting fbal_max = 0 will block duty-cycle adjustment from the fbal function.

3.2.4.2 Flux balancing PI filter

The flux balancing PI filter is defined by kp_fbal, ki_fbal. It consists of a proportional term that works on the instantaneous magnitude of the error, and an integral term that works on the magnitude and the duration of the error. The integral term is the sum of the instantaneous error over time, and it gives the accumulated error. The integral term sets how strongly the loop will respond to the "past" information. The integral term sets the low-frequency gain, and the proportional term sets the high-frequency gain. The magnitude response of the PI filter is defined by:

$$\sqrt{kp^2 + \left(\frac{ki}{2\pi \cdot Ts \cdot f}\right)^2}$$

Here, Ts is the converter switching period.

Table 8 Flux balancing PI filter register

Register	Description	Equation
kp_fbal	Flux/voltage balancing PI filter proportional coefficient index	kp_exp = kp_fbal [5:3] kp_man = 8 + kp_fbal [2:0] kp = kp_man * 2^(kp_exp – 18)
ki_fbal	Flux/voltage balancing PI filter integral coefficient index	ki_exp = ki_fbal [5:3] ki_man = 8 + ki_fbal [2:0] ki = ki_man * 2^(ki_exp – 22)

Design example:

kp_fbal = 8_D = 001000_B, kp = 8 * 2^ (1-18) = 6.1*10^-5

ki_fbal = 30_D = 011110_B, ki = (8+6) * 2^ (3-22) = 2.67*10^-5

The PI filter magnitude over frequency can be plotted as in **Figure 26**, at F_{sw} = 250 kHz.

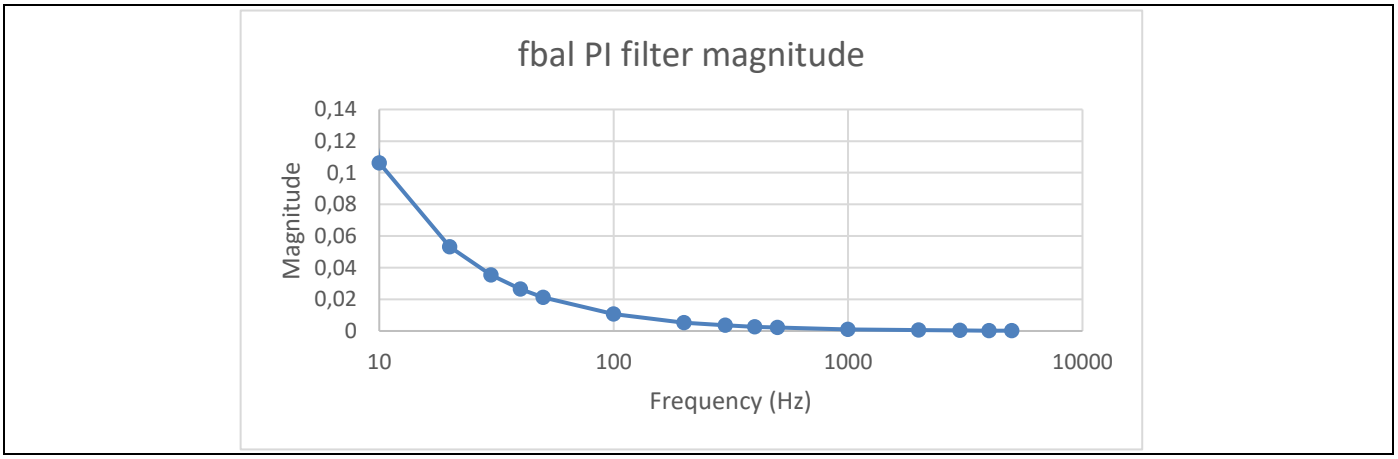


Figure 26 fbal PI filter example

Note: Subscript #$_D$ means the data is in decimal format; #$_B$ means the data is in binary format.

3.2.4.3 DCM operation

At light load, output inductor current flows in a negative direction. If the secondary rectifier is not an SR MOSFET but a diode, the output current is discontinuous. It can be termed Discontinuous Conduction Mode (DCM) to indicate that the inductor current is discontinuous (diode mode) or negative (SR mode).

In DCM operation, the VRS rising edge happens before the primary PWM rising edge because the negative current in the inductor drives the VRS high as soon as the opposite SR turns off. That means the V_{rect} pulse width could not indicate primary PWM mis-match. Disabling flux balance in DCM is recommended. Flux balance DCM control registers are listed in **Table 9**.

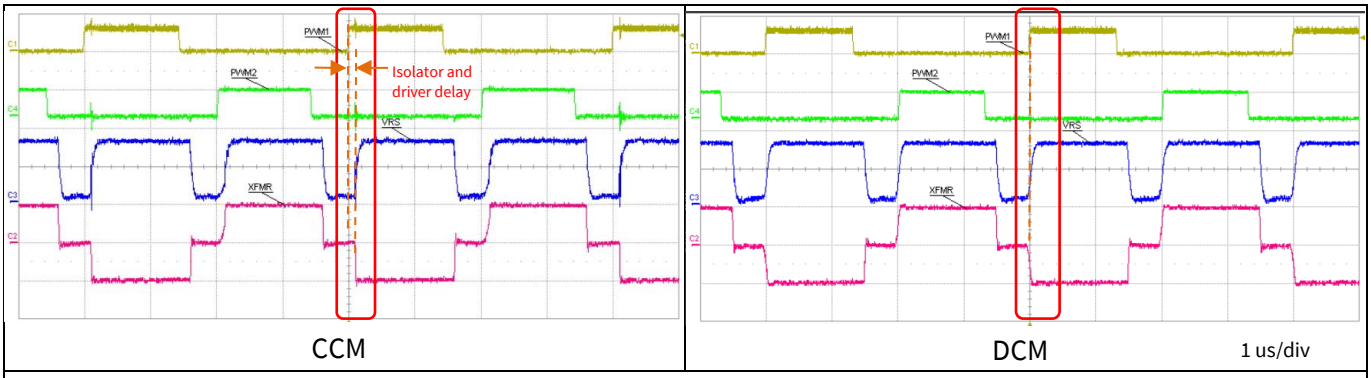


Figure 27 Full-bridge VRS voltage waveform in Continuous Conduction Mode (CCM) and DCM

Table 9 Registers to disable flux balance in DCM

Register name	Description	Example
fbal_dcm_thresh	Determines where the fbal duty adjust will be removed in DCM mode Index of 63 disables feature LSB 0.5 A, range 0 to 31 A	Set to 20 for 10 A DCM threshold
fbal_dcm_dis_cnt	1 to 4, number of consecutive current samples below threshold to disable fbal	Set to 2, flux balance will be disabled after three consecutive current samples lower than fbal_dcm_thresh
fbal_dcm_ena_cnt	1 to 4, number of consecutive current samples above threshold to enable fbal	Set to 2, flux balance will be enabled after three consecutive current samples higher than fbal_dcm_thresh
fbal_dcm_0out_duty_adj	Determines whether in DCM mode to zero out fbal_duty_adj or freeze the current duty adjust	0 = freeze the current fbal_duty_adj 1 = zero out fbal_duty_adj Set to 1 is recommended

The DCM threshold varies with input voltage. Setting the fbal_dcm_thresh based on high-line operation could cover both low-line and high-line situations. A variable fbal_dcm_thresh per input voltage is also possible by FW patch.

Setting fbal_dcm_dis_cnt, fbal_dcm_ena_cnt to a higher number helps reduce jittering at the threshold boundary.

More details of flux balancing can be found in the XDPP1100 application note.

4 Regulation and telemetry

4.1 Line and load regulation

Line and load regulation was tested at 36 V, 48 V and 75 V input, at 0 A/5 A/10 A/25 A/30 A/40 A/50 A load. The FB-FB board is designed to work in open-loop condition at low-line (less than 42 V), when output voltage drops with V_{IN}. Thus at 36 V input, the output voltage is set to 10 V for regulation.

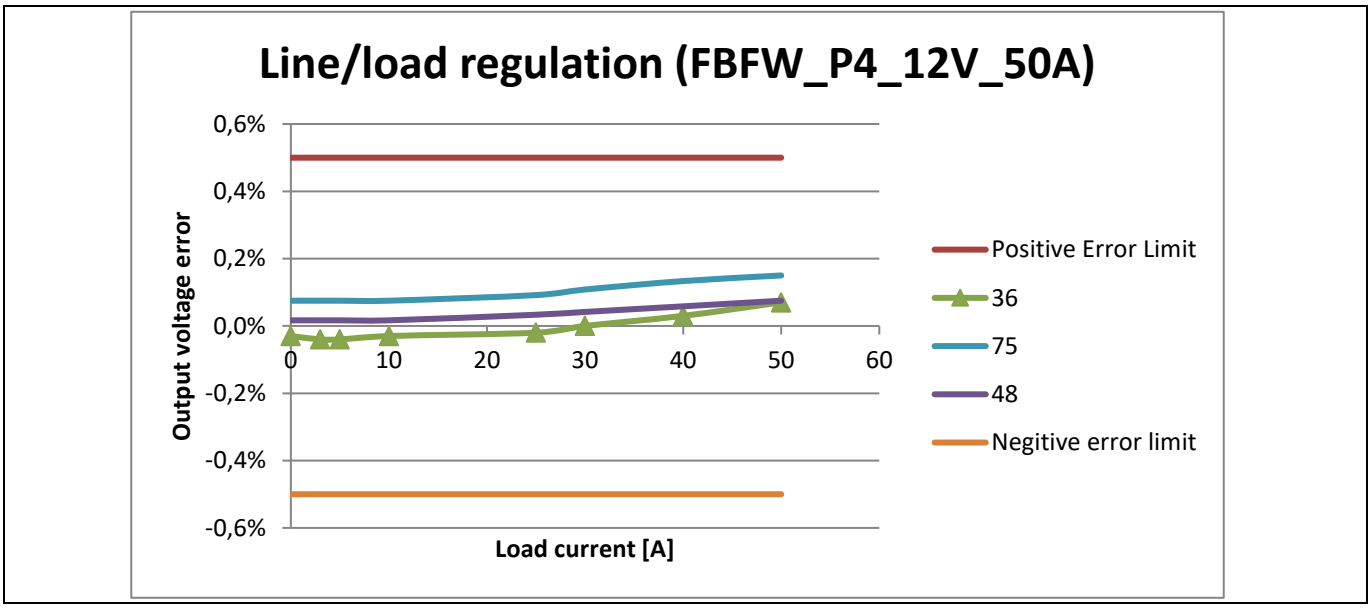


Figure 28 600 W FB-FB line and load regulation

4.2 Output voltage ripple and stability

Output voltage ripple was measured at the tip-and-barrel test point at 20 MHz BW. Output voltage ripple and stability results are shown below, with a 240 mV limit. Ripple and stability is output PARD measured over a wider time base while only ripple is measured on a cycle-by-cycle timeframe.

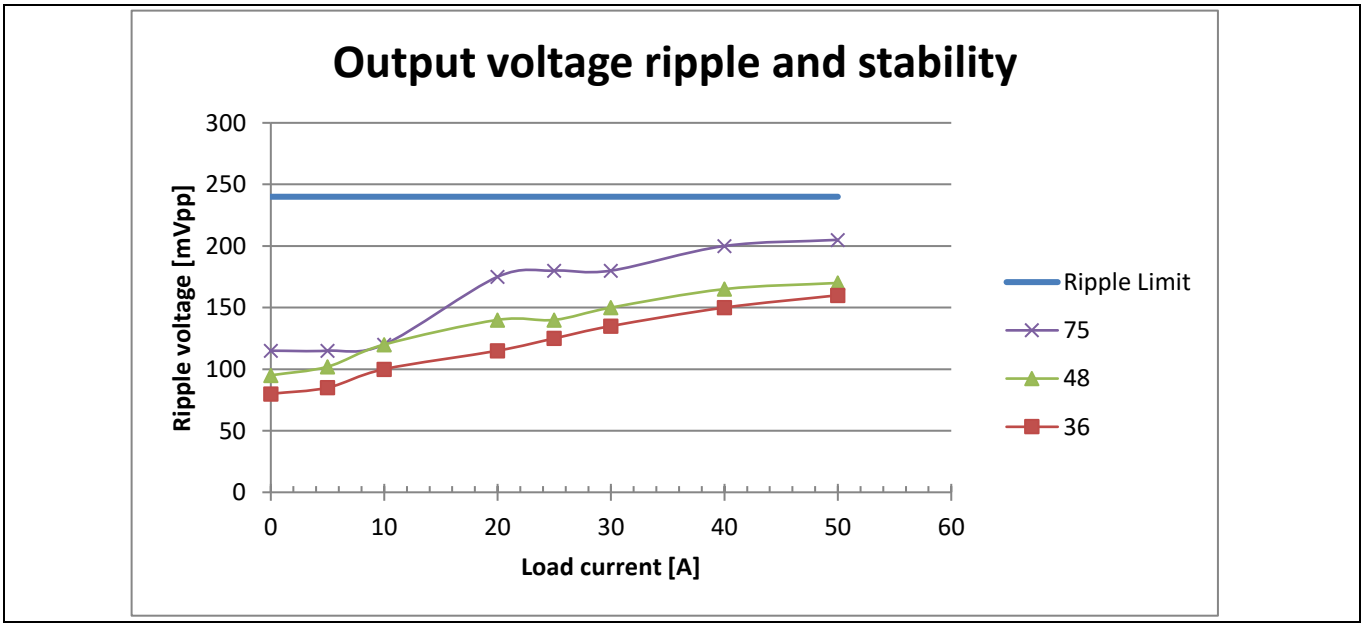


Figure 29 Output voltage ripple and stability

Output ripple and stability waveforms are shown in **Figure 30**. Ch3: output voltage AC coupled, 50 mV/div.

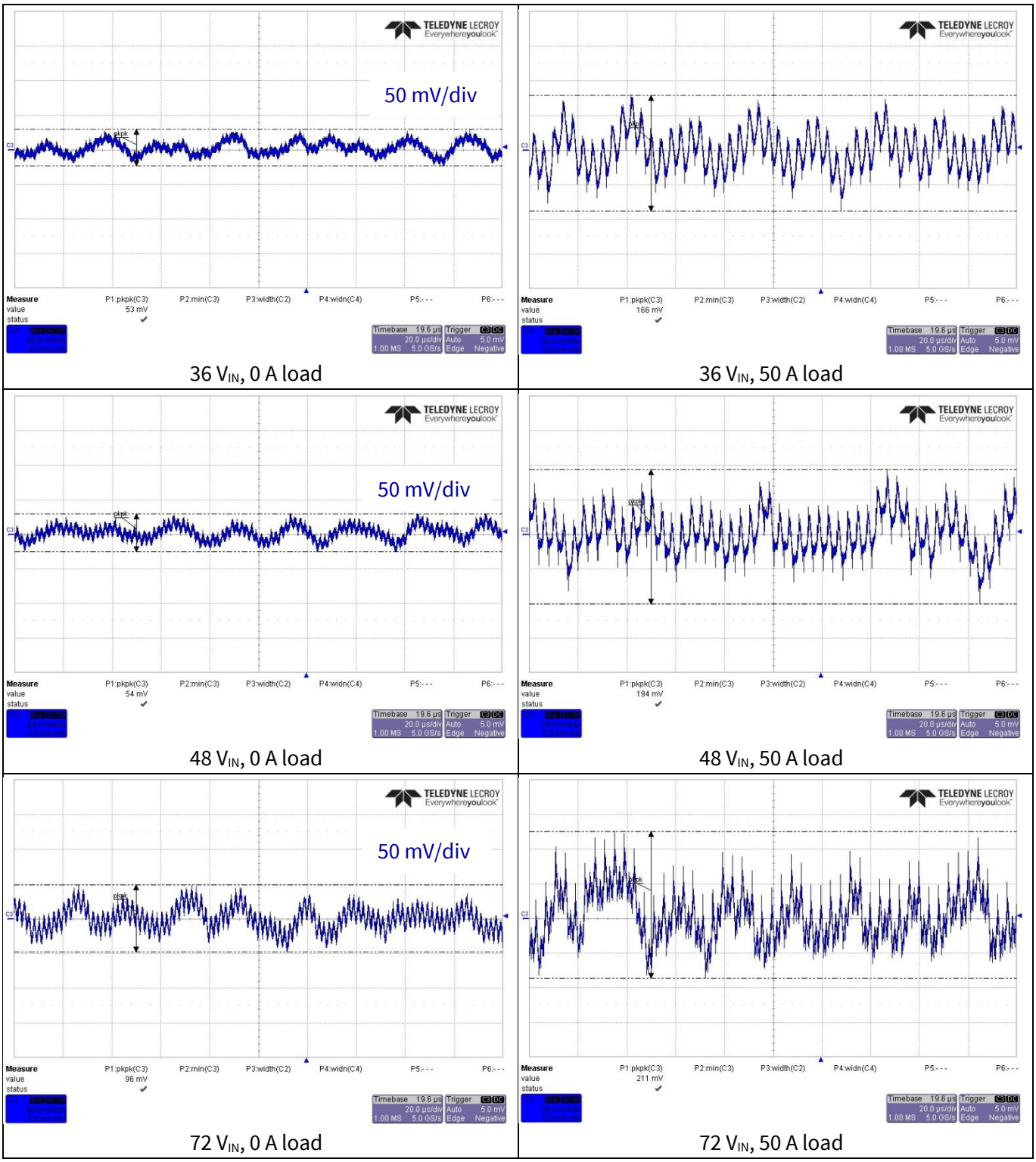


Figure 30 Output ripple and stability waveforms

Output ripple only waveforms are shown in **Figure 31**. Ch3: output voltage AC coupled, 50 mV/div.

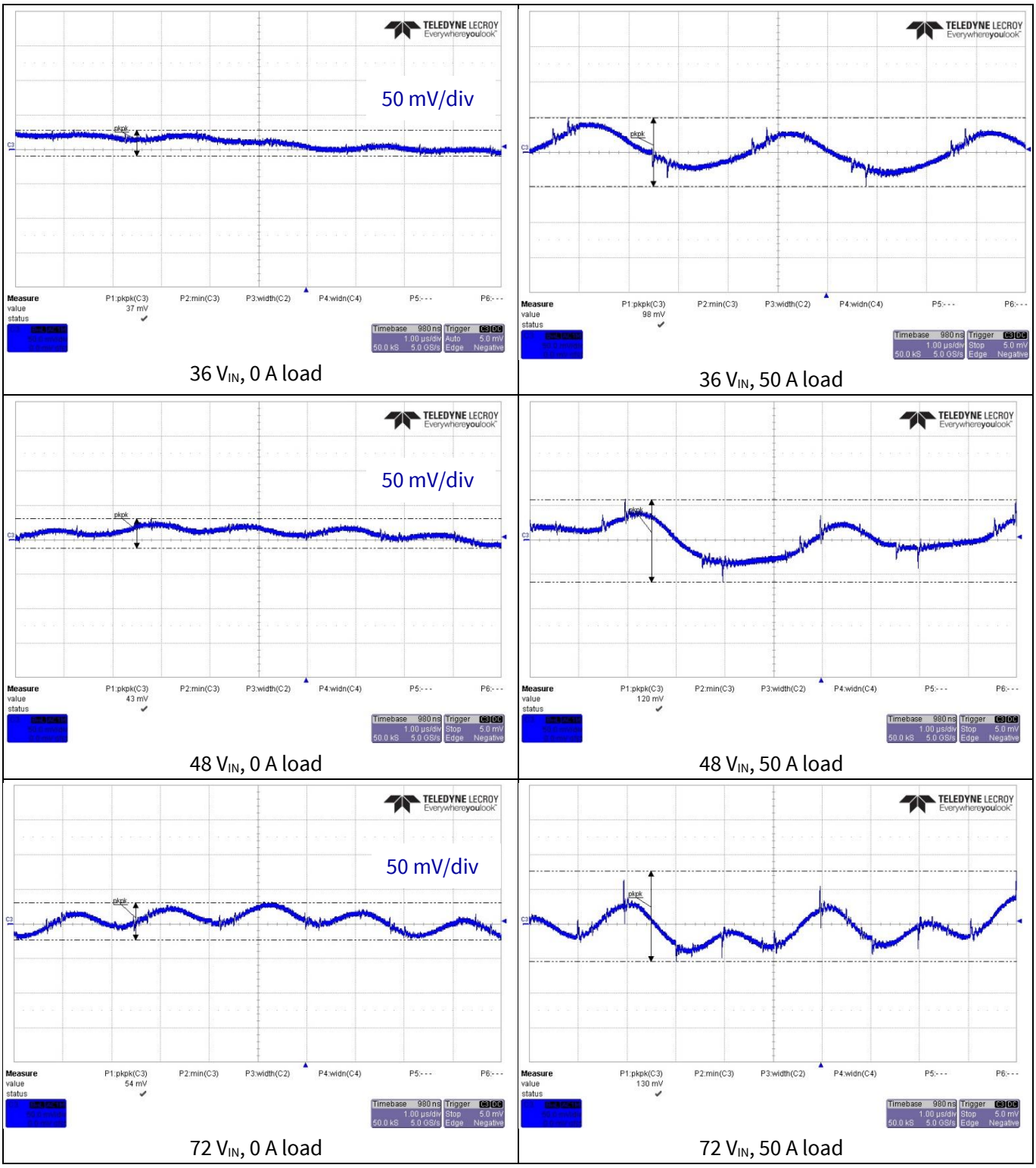


Figure 31 Output ripple waveforms

4.3 V_{IN} telemetry

XDPP1100 senses input voltage from the secondary side of the transformer through V_{rect} sensing. It can also sense the input voltage through the PRISEN on the XDPP1100 taken from the bias winding, before the main converter switching starts. Once the main converter starts switching, the input voltage sense changes to V_{rect}

sensing. See descriptions in 3.2.3. **Figure 32** shows the input voltage sensed by V_{rect} in regulation. At heavy load, the voltage drop on power path resistance could introduce READ_VIN error. XDPP1100 enables resistive compensation, which is set by register tlm0_vrect_rcorr (LSB=3.90625 m Ω). Setting this register to 8 (31.2 m Ω) gave a good compensation result. The error of V_{IN} telemetry is within +/-2 percent. The absolute error is less than 0.5 V, when tested with flux balancing set to "time only" mode.

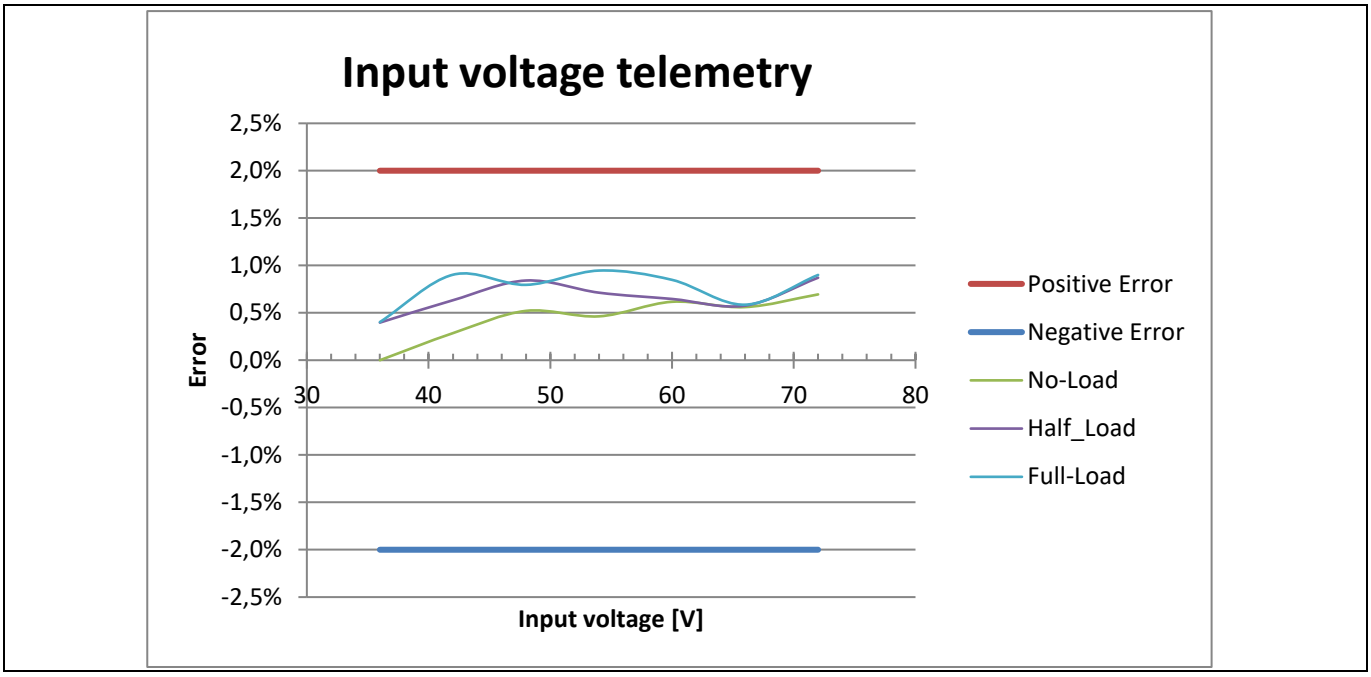


Figure 32 READ_VIN accuracy

The input voltage telemetry sensed on the PRISEN input is taken from the bias supply while the main converter is not switching. **Figure 33** shows the telemetry result with PRISEN.

Settings used for PRISEN to sense input voltage on 600 W FB-FB quarter-brick:

- prisen_meas_en = 1
- vin_pwl_slope = 2993
- vin_trim = 28
- tlm0_vin_src_sel = 3

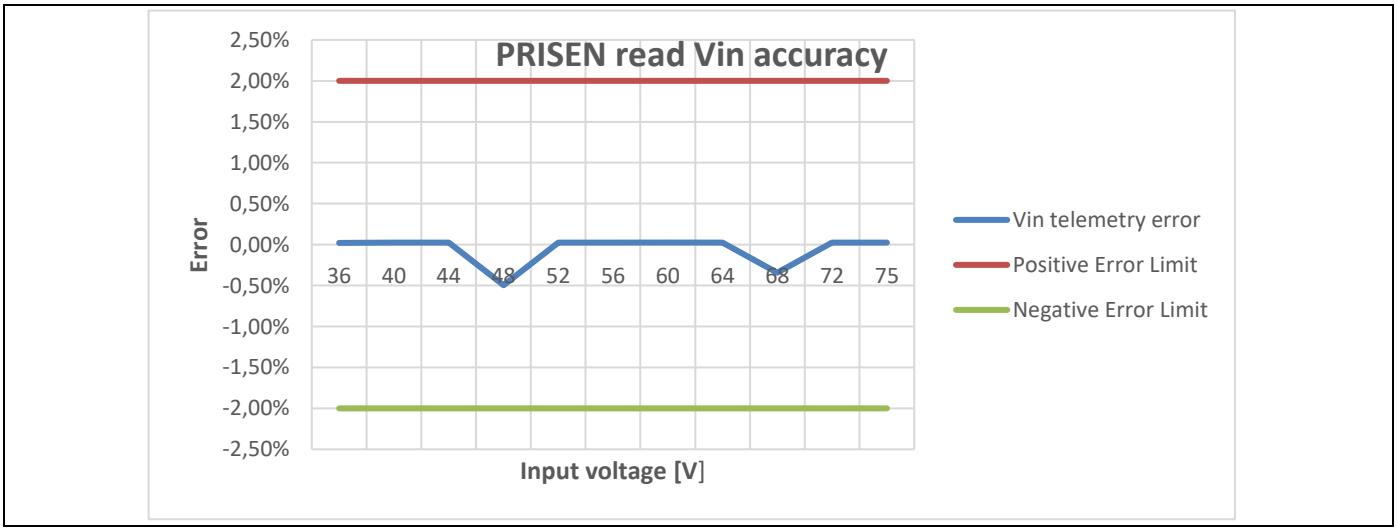


Figure 33 PRISEN READ_VIN accuracy

4.4 I_{OUT} telemetry

Output current telemetry has less than 1 A error over all input lines at loads from 3 A to 50 A. The error at light load is due to the CS op-amp being clamped when current is negative, thus the IC sees a larger error. Current read with temperature compensation is enabled. The temperature sensor assigned to READ_TEMPERATURE_1 is used to compensate I_{OUT} telemetry.

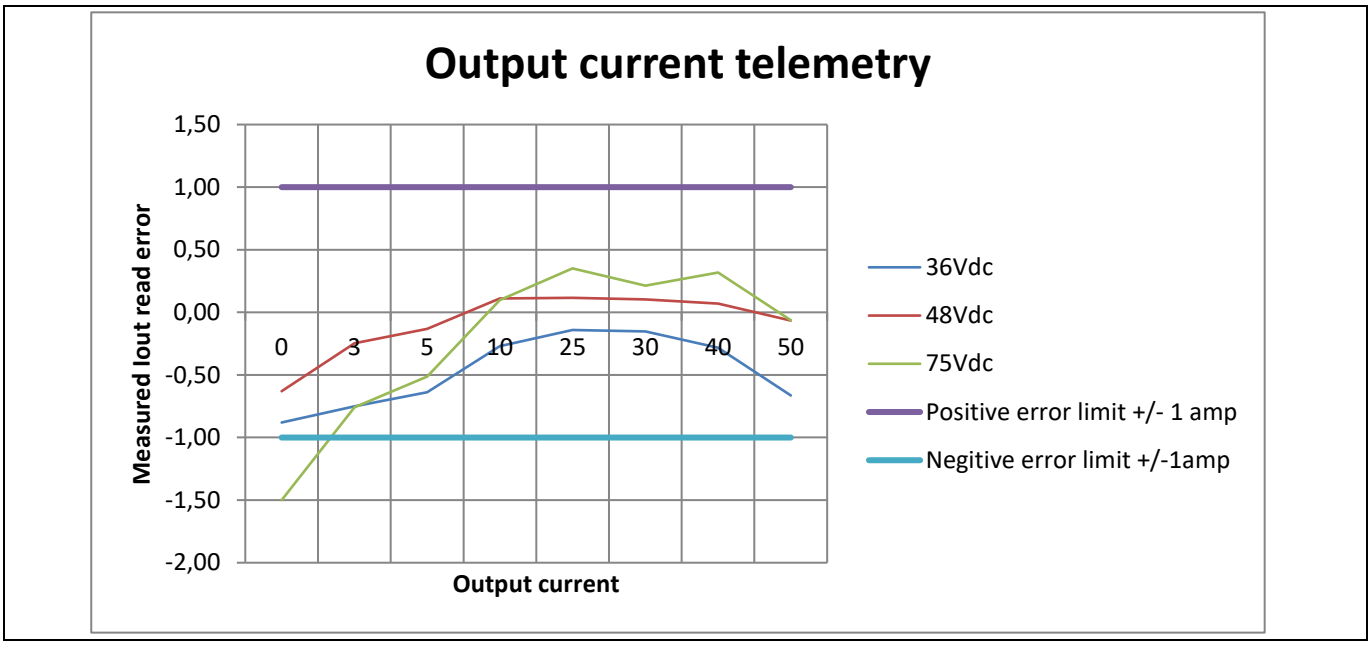


Figure 34 READ_IOUT accuracy

4.5 I_{IN} telemetry

Input current is estimated based on I_{OUT} and V_{IN} (tlm0_iin_src_sel=2). The accuracy of I_{OUT} telemetry directly impacts I_{IN} telemetry. READ_IIN accuracy is within +/-10 percent at loads of 10 A and above.

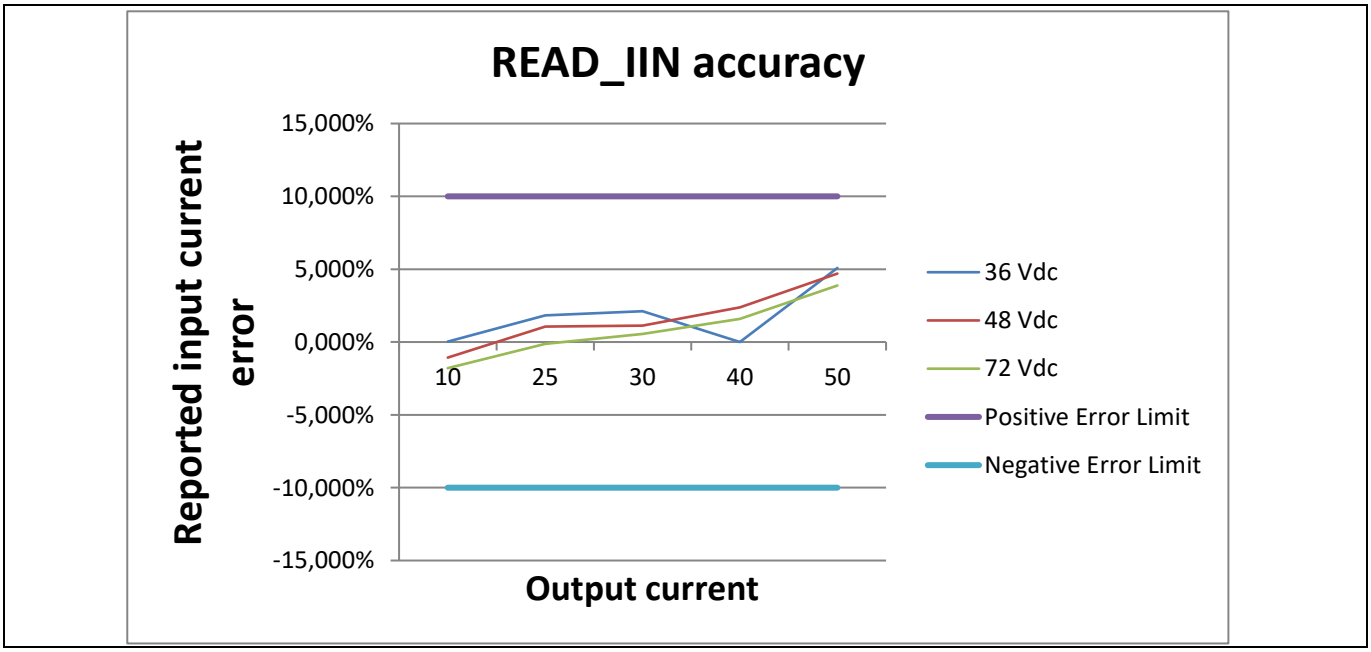


Figure 35 READ_IIN accuracy

4.6 Efficiency

The efficiency is measured over line and load. At 36 V input, V_{OUT} is set to 10.7 V for regulation, thus the maximum output power is 535 W at 36 V input. Gate dead-time is minimized to increase quarter-brick efficiency (**Figure 36**). In the efficiency test, the output voltage is measured at the power pin 12 V_{OUT} and RTN to exclude voltage drop loss due to contact resistance. Thus output voltage in the table shows a small drift. The actual output voltage at the remote sense point is constant without drift.

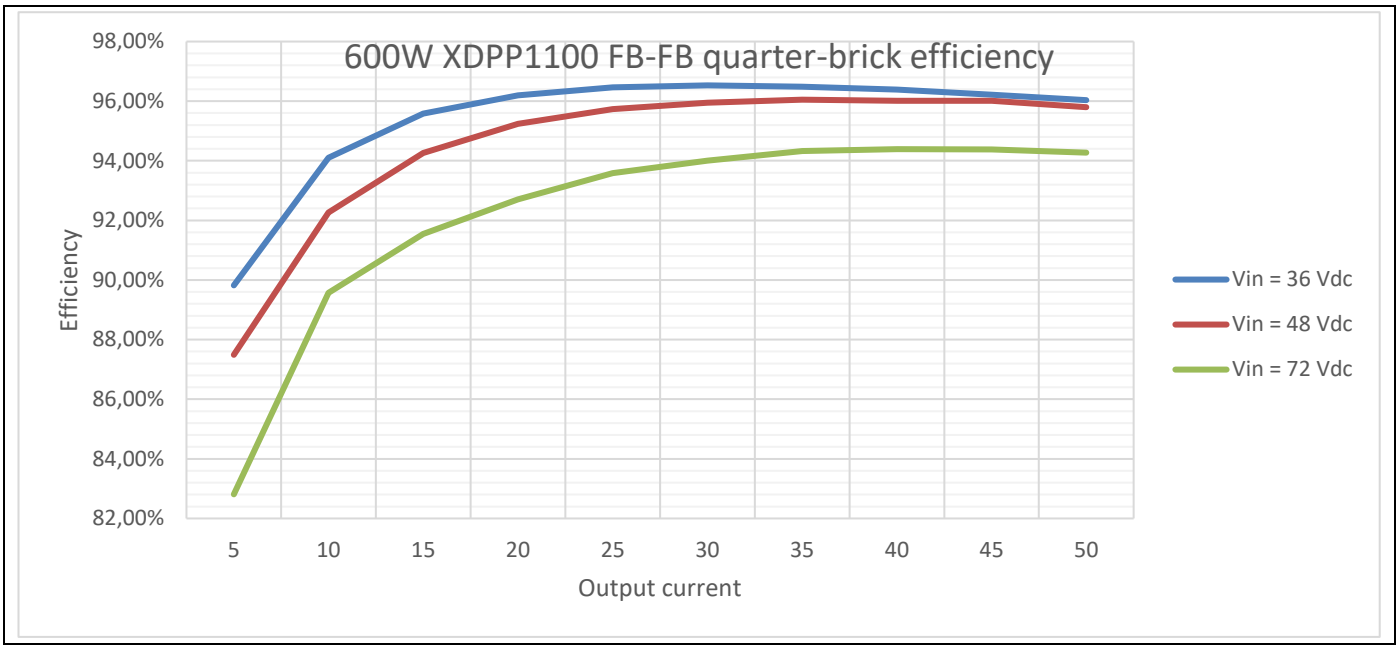


Figure 36 Efficiency of 600 W quarter-brick FB-FB with digital controller XDPP1100

Table 10 600 W QB efficiency table

Testing done at 36 V DC input

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
36.019	0.157	5.654	10.698	–	–	–
36.054	3.158	113.85	10.716	9.997	107.13	94.10%
36.083	6.189	223.31	10.736	20.008	214.81	96.19%
36.097	9.257	334.14	10.754	29.994	322.56	96.53%
36.080	12.385	446.85	10.773	39.981	430.72	96.39%
36.023	15.497	558.24	10.727	49.972	536.05	96.03%

Testing done at 48 V DC input

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
48.007	0.127	8.25	12.001	–	–	–
48.045	2.711	130.24	12.017	10.000	120.17	92.27%
48.036	5.261	252.71	12.033	20.002	240.68	95.24%
48.014	7.844	376.62	12.050	29.988	361.36	95.95%
48.021	10.466	502.58	12.071	39.975	482.54	96.01%
48.087	13.118	630.80	12.095	49.964	604.31	95.80%

Testing done at 72 V DC input

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
72.025	0.173	12.46	12.000	–	–	–
71.865	1.867	134.17	12.018	10.000	120.18	89.57%
71.898	3.614	259.83	12.026	20.011	240.85	92.70%
71.831	5.354	384.58	12.058	29.996	361.69	94.00%
71.654	7.141	511.68	12.080	39.982	482.98	94.39%
71.568	8.967	641.75	12.106	49.972	604.96	94.27%

Gate timing settings used for efficiency measurement are shown below.

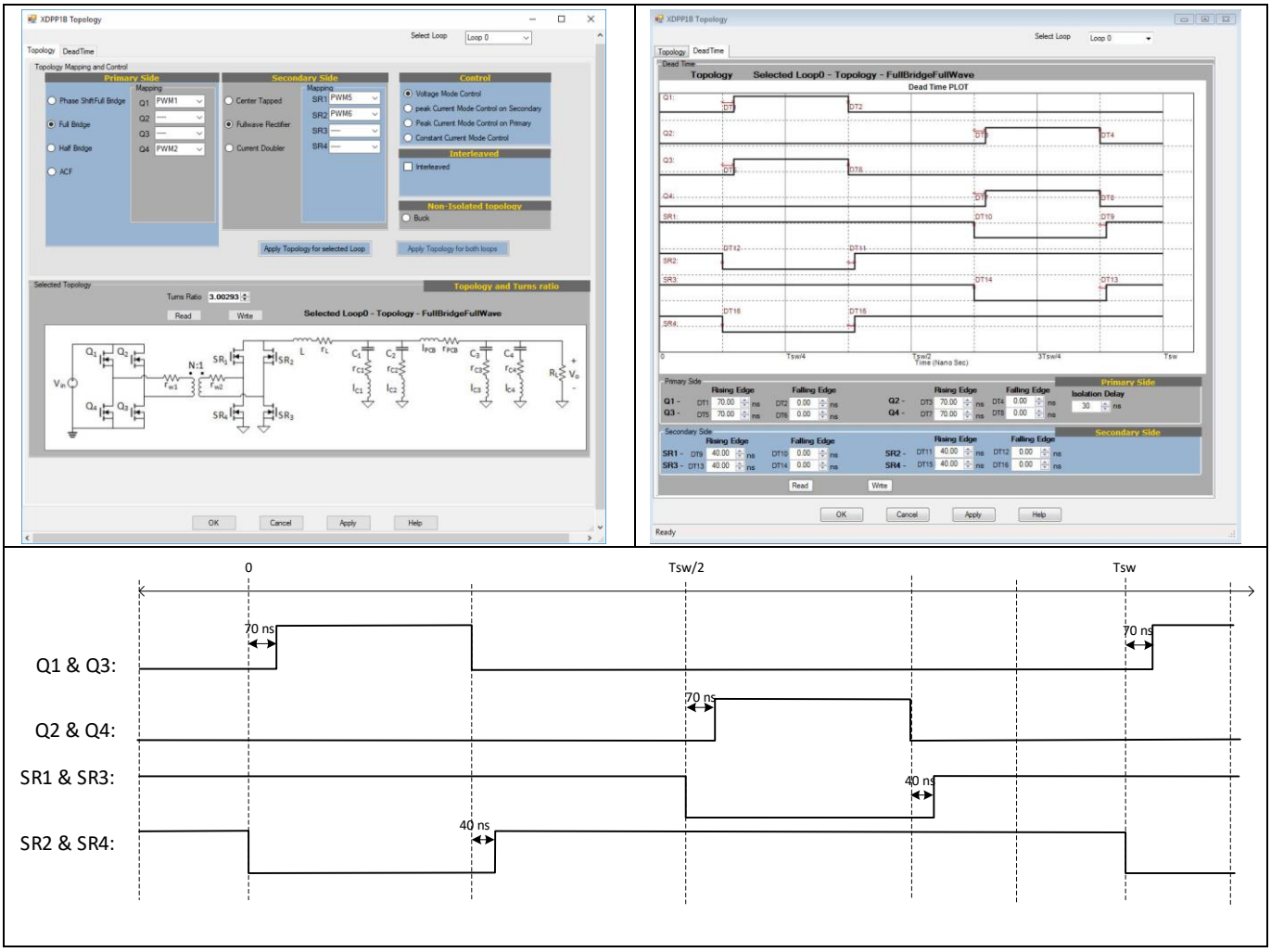


Figure 37 Gate timing settings used for efficiency measurement

4.7 Temperature telemetry

The XDPP1100 supports both external temperature sensing and internal temperature sensing for protection and monitoring. External temperature sensing is performed with a 47 kΩ NTC thermistor, in parallel with a 12 kΩ resistor.

To test temperature telemetry, the unit was heated up while reading the board temperature through the XDPP1100 controller. The board was tested at a nominal input voltage of 48 V DC. The fan speed was slowly

reduced, causing the board to heat up. The measurement was taken by using a thermocouple applied to the PCB. The telemetry reading was fairly close to the actual temperature measurement.

Table 11 Temperature telemetry accuracy

Temperature, Ta (NTC telemetry)	Temperature, Ti (XDPP1100 internal telemetry)	Real I_{sense} trace temperature (thermocouple)
0	0	0
10	10	10
20	20	20
30	31	31
40	40	40
50	51	50
60	60	61
70	70	72

4.8 Thermal image

The thermal image at 50 A full load is shown in **Figure 38**, **Figure 39** and **Figure 40**.

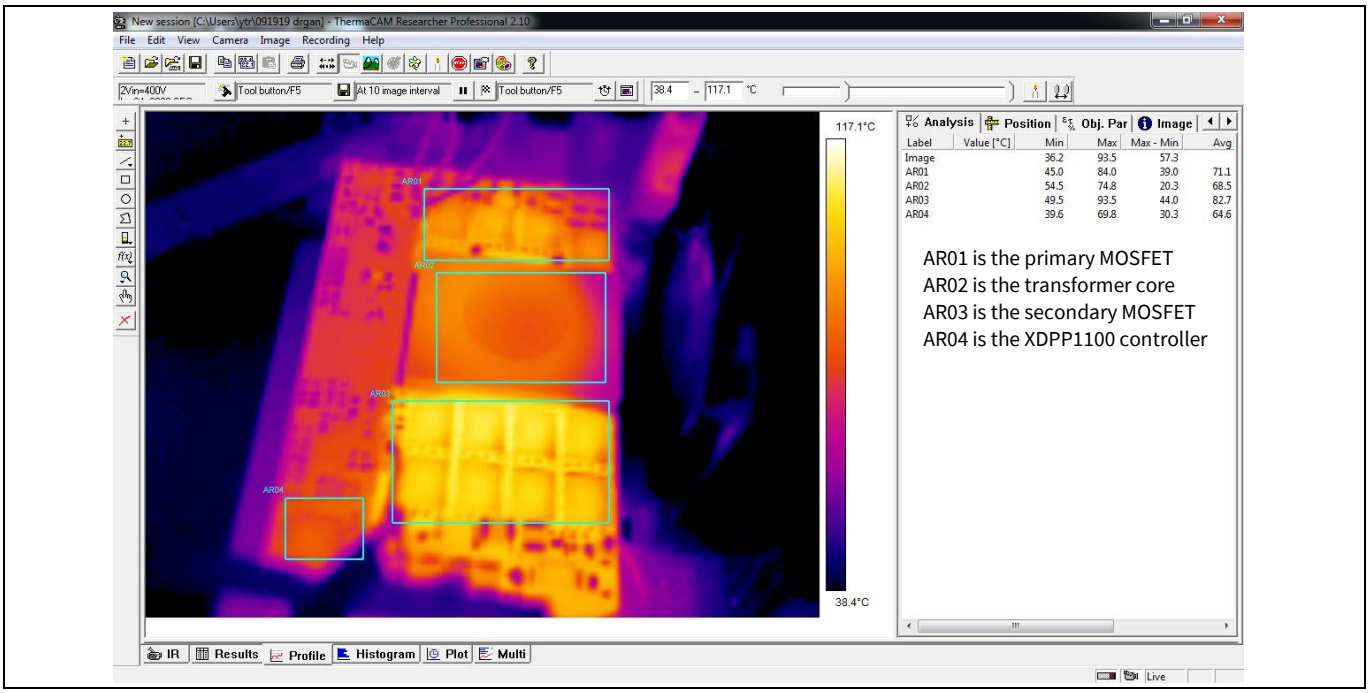


Figure 38 Full load thermal image at 36 V input and 7.5 V on cooling fan

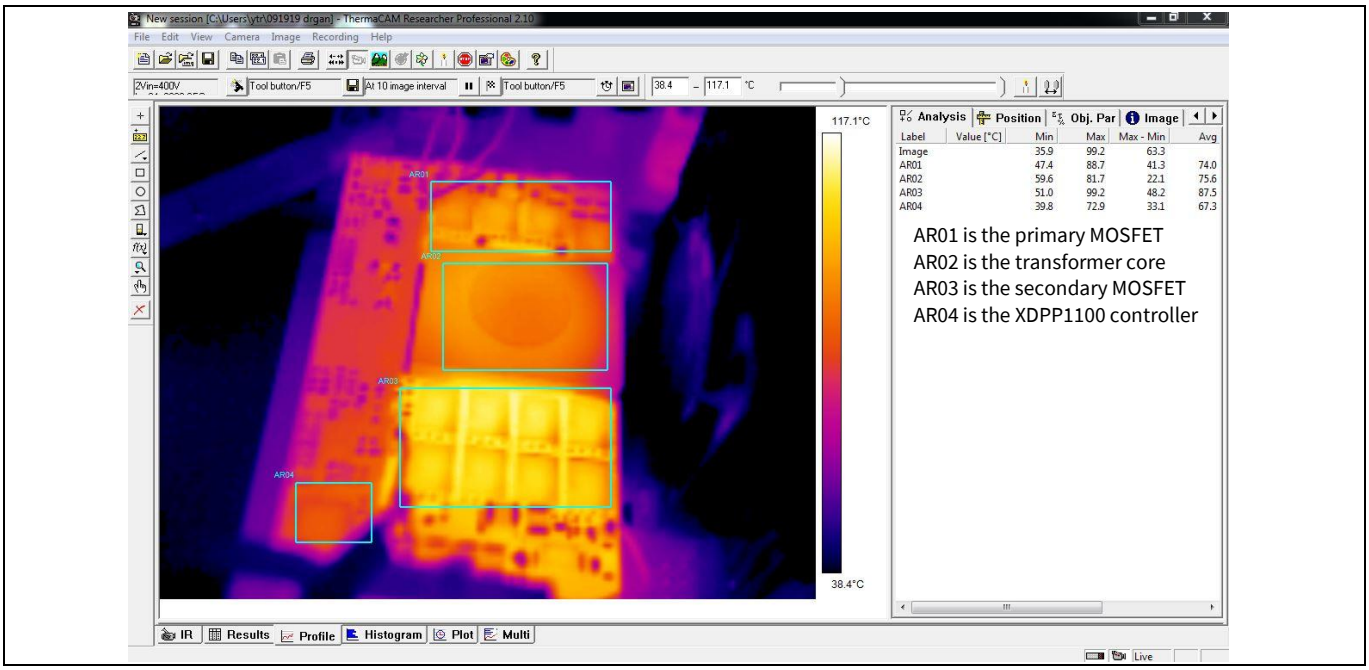


Figure 39 Full load thermal image at 48 V input and 7.5 V on cooling fan

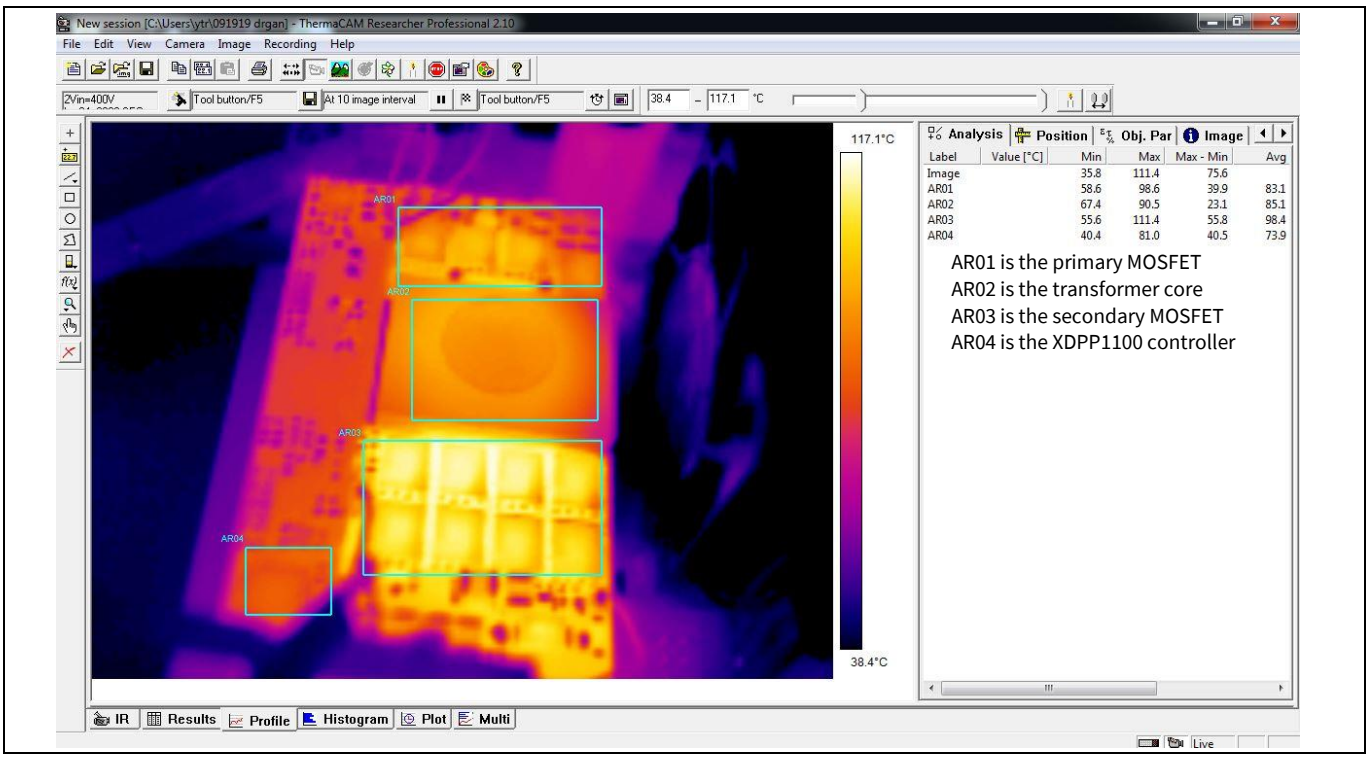


Figure 40 Full load thermal image at 75 V input and 7.5 V on cooling fan

5 Operation waveforms

5.1 Primary and secondary gate and drain signals

The following waveforms were taken to show the optimization of dead-time between the primary and secondary MOSFETs. The dead-time between the primary gate and the diagonal SR gate is minimized to 40 ns for the best efficiency. The detail waveforms shows the dead-time.

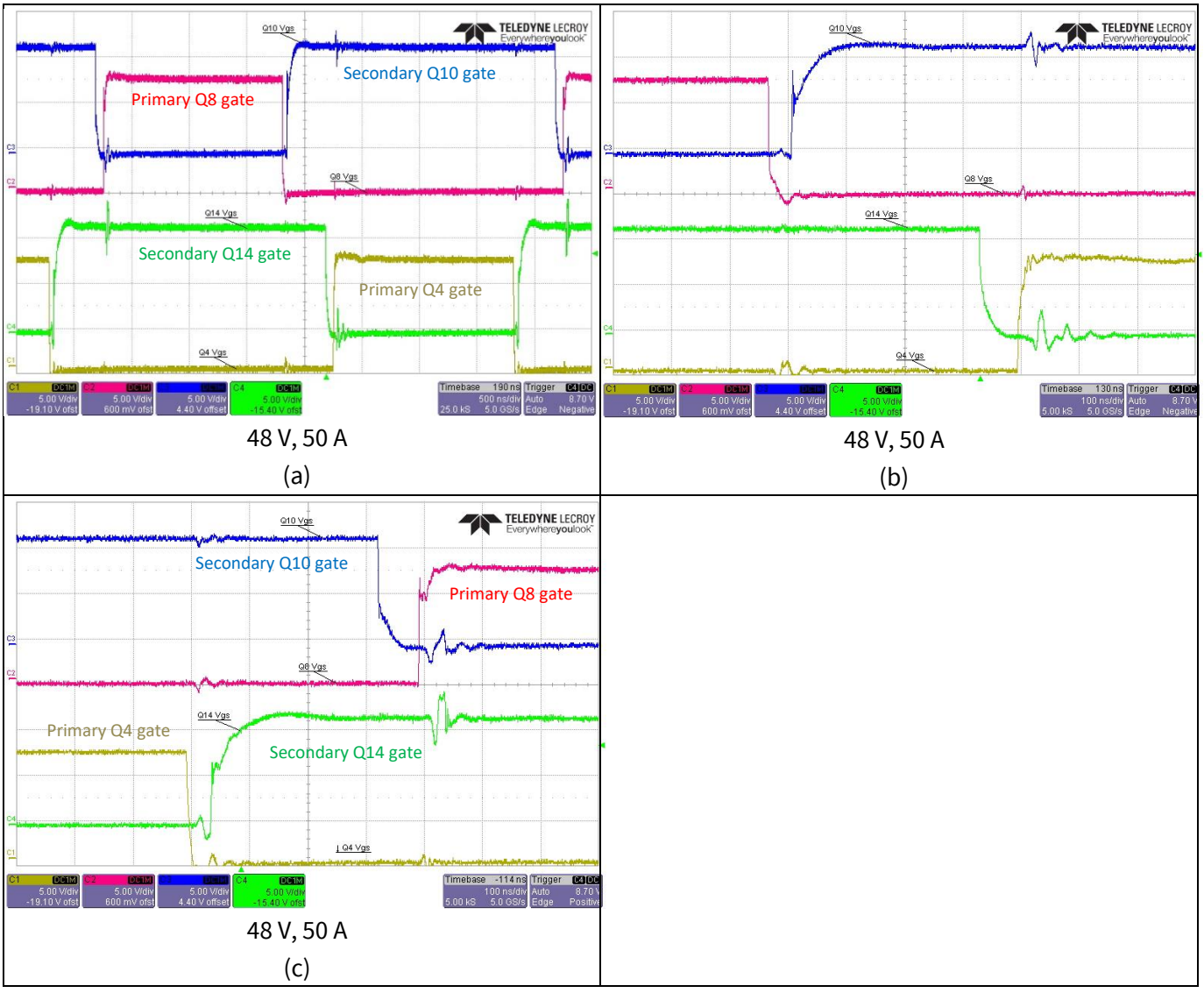


Figure 41 Primary and secondary gate drive waveforms

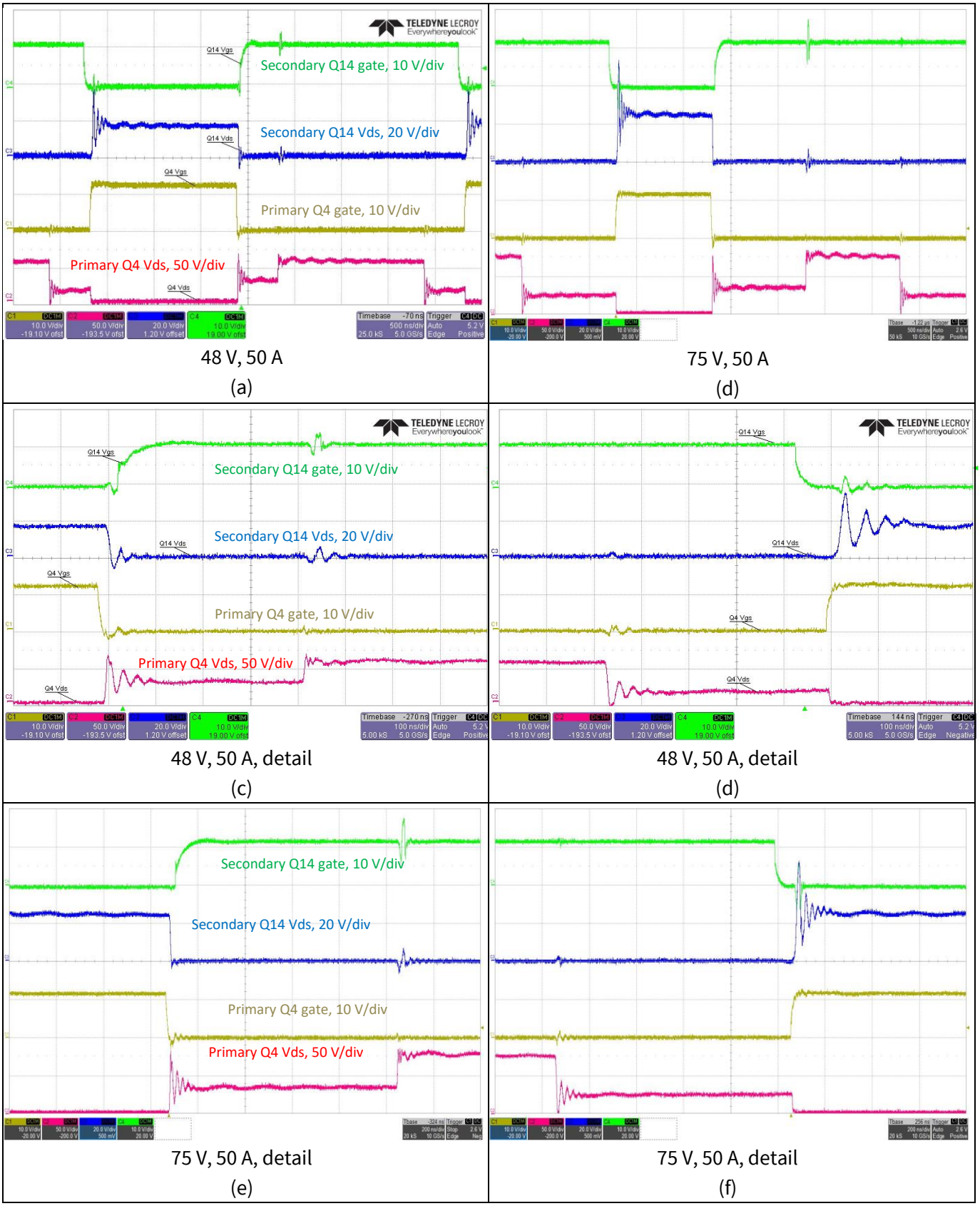
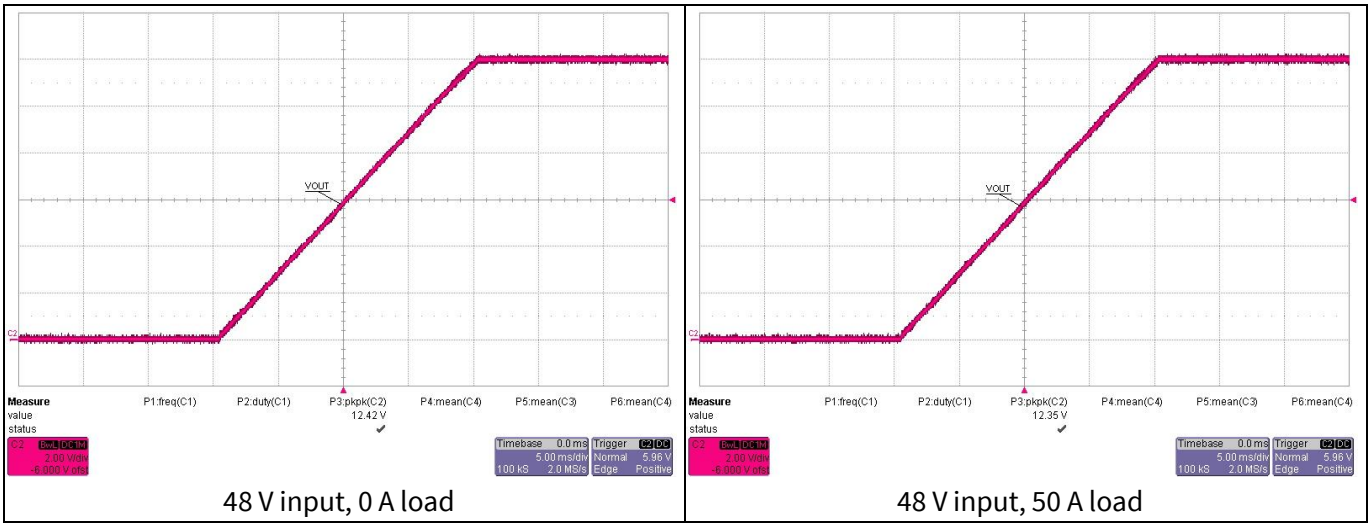


Figure 42 Primary and secondary gate and drain waveforms

5.2 Soft-start

Soft-start is tested at 0, 50 percent and 100 percent load, at 36 V/48 V/72 V input. SR is enabled from the beginning of start-up (diode emulation mode is disabled). It is tested at TON_RISE = 20 ms. V_{OUT} has a monotonic ramp without glitch.

Figure 43 shows start-up waveforms at 48 V input.



48 V input, 0 A load | 48 V input, 50 A load

Figure 43 Monotonic start-up (Ch2: V_{OUT} 2 V/div)

5.3 Pre-bias start-up

Pre-bias start-up is tested at no-load condition, with Diode Emulation (DE) mode (PMBus command 0xC5 FW_CONFIG_REGULATION bit:0 = 1, EN_DE_STARTUP=1), and with SR enabled (PMBus command 0xC5 FW_CONFIG_REGULATION bit:0 = 0, EN_DE_STARTUP=0). The output pre-bias turn-on is tested with and without input voltage sensed by PRISEN. The label of “VOUT without PRISEN patch” is tested with V_{rect} input voltage sensing (tlm0_vin_src_sel=0), with vrs_voltage_init = 58 (initial input voltage set to 48 V). The label of “VOUT using PRISEN patch” is tested with PRISEN input voltage sensing priort to start-up (tlm0_vin_src_sel= 3), and switched to V_{rect} sensing after the converter is enabled. The control of the transition is handled by FW patch.

Settings used for PRISEN to sense input voltage on 600 W FB-FB quarter-brick:

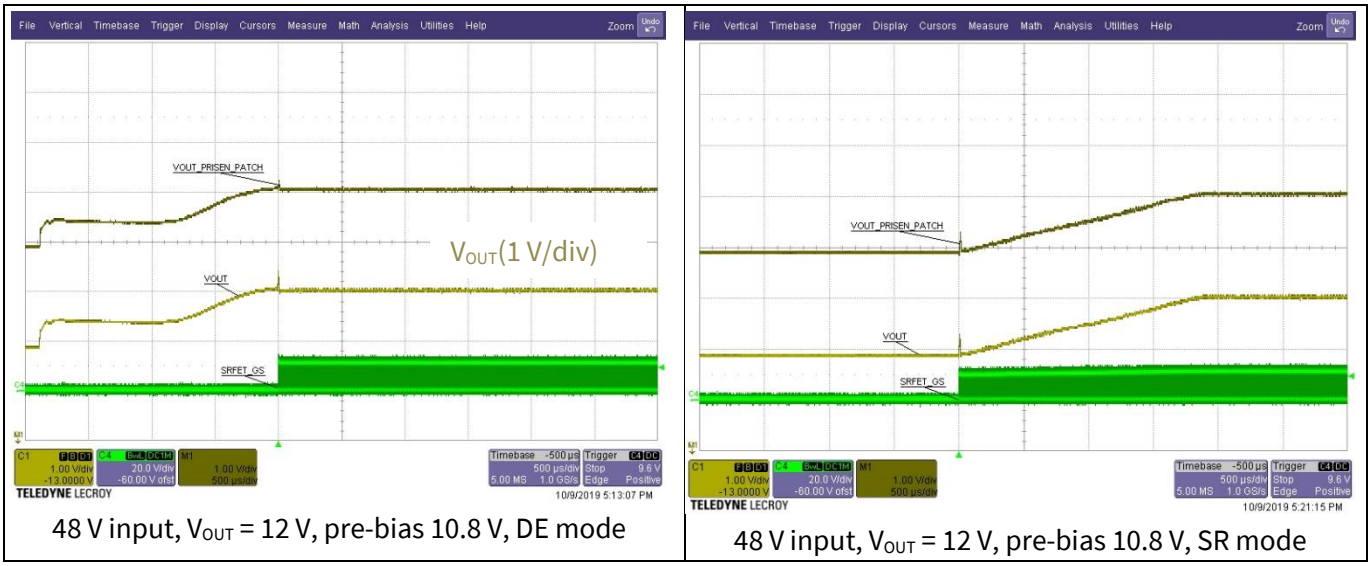
- prisen_meas_en = 1
- vin_pwl_slope = 2993
- vin_trim = 28
- tlm0_vin_src_sel = 3

Pre-bias voltage is set to 90 percent of the target V_{OUT} (10.8 V).

Ch1 = V_{OUT} without PRISEN patch, Ch4 = secondary gate, M1 = V_{OUT} using PRISEN patch

The start-up ramp will keep the same slope as regular start-up without pre-bias. The start time is calculated by FW:

Ramp_time = TON_RISE * (VOUT_COMMAND - Pre-bias_voltage) /VOUT_COMMAND



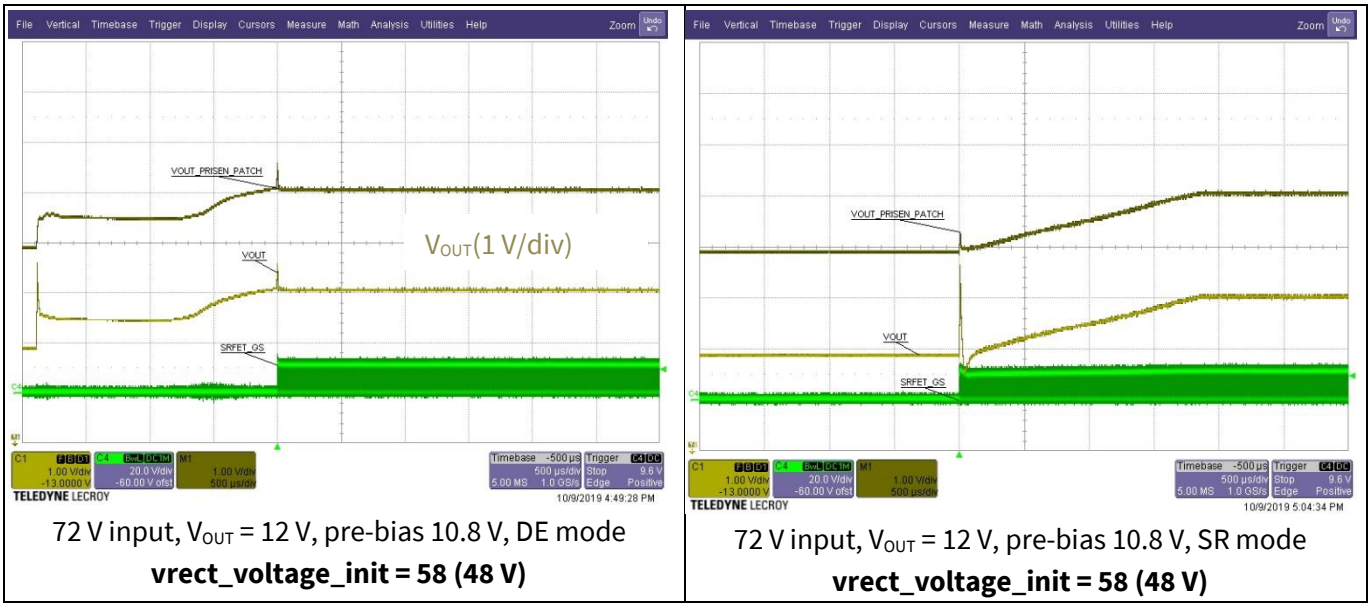
48 V input, V_{OUT} = 12 V, pre-bias 10.8 V, DE mode

48 V input, V_{OUT} = 12 V, pre-bias 10.8 V, SR mode

Figure 44 Pre-bias start-up at 90 percent V_{OUT}, 0 A load, 48 V V_{IN}

A voltage step at no-load is observed at the beginning of ramp with diode emulation start-up (DE mode). This is because the start-up duty-cycle is predicted by the FF circuit based on $V_{OUT}/(V_{IN}*Ns/Np)$. This works when SR is enabled. The actual desired duty-cycle is very narrow at no-load in DE mode. In DE mode, the energy delivered to load is more than required, thus the output voltage is charged up with a step. The feedback loop will then reduce the duty-cycle or even turn off primary PWM. But since there is no load to discharge the output capacitor, the voltage plateau is held there until the internal ramp exceeds the plateau voltage and continues to charge the output capacitor toward target V_{OUT}. At the end of the ramp, SR will turn on when V_{OUT} reaches the target voltage, which is defined by (VOUT_COMMAND – Vout_target_window). There is a small glitch when SR turns on, caused by the difference between body diode voltage drop and MOSFET channel voltage drop.

Ch1 = V_{OUT} without PRISEN patch, Ch4 = secondary gate, M1 = V_{OUT} using PRISEN patch



72 V input, V_{OUT} = 12 V, pre-bias 10.8 V, DE mode
vrect_voltage_init = 58 (48 V)

72 V input, V_{OUT} = 12 V, pre-bias 10.8 V, SR mode
vrect_voltage_init = 58 (48 V)

Figure 45 Pre-bias start-up at 90 percent V_{OUT}, 0 A load, 72 V input

At 72 V input pre-bias start-up, higher voltage spike is observed at the beginning of the ramp in both DE mode and SR mode. This is because the initial voltage was set to 48 V and the FF duty-cycle is calculated based on 48 V input. This results in larger duty-cycle than the system requires. To solve this issue, the board adds another input sensing channel using the PRISEN to sense the input voltage before switching starts. A FW patch is loaded

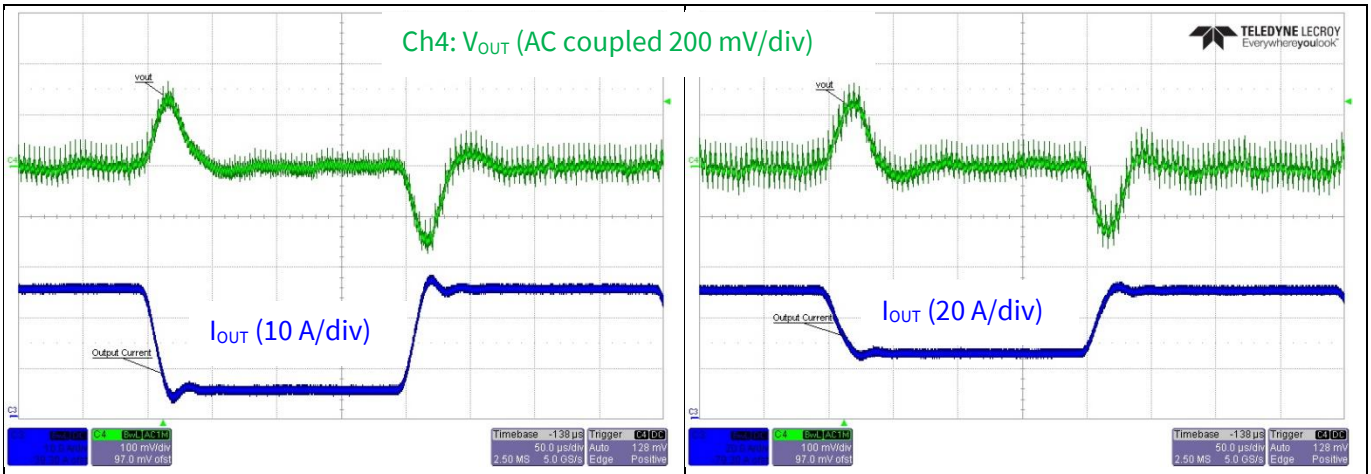
in the chip. It copies the measured input voltage to the initial voltage register (vrs_voltage_init) when the converter starts up. This ensures accurate calculation of the FF duty-cycle. The test result shows that the output voltage spike is greatly reduced by the M1 plot in **Figure 45**.

5.4 Load transient of VMC

The loop was optimized with the following PID values for VMC. For 36 V DC inut the output was set to regulate at 10 V. E-load transition rate is set to 2.5 A/µs.

Pid0_kp_index_1ph = 39, Pid0_ki_index_1ph = 25, Pid0_kd_index_1ph = 60.

The overshoot and undershoot are less than 250 mV. The loop settling time is less than 50 µs.

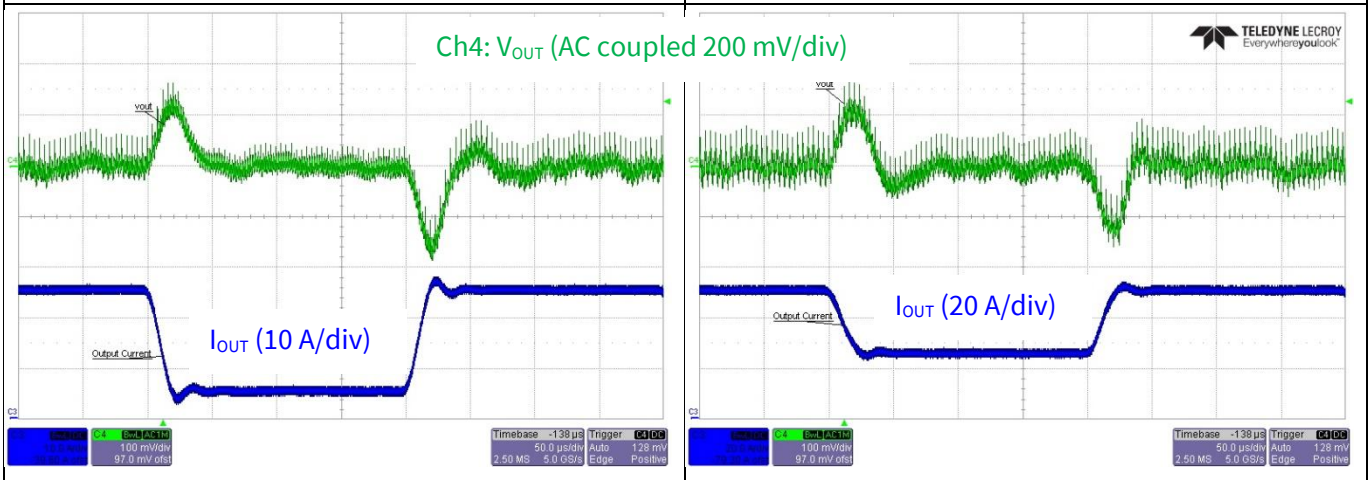


V_{IN} = 36 V DC at 10 percent – 50 percent – 10 percent load transient

(a)

V_{IN} = 36 V DC at 50 percent – 100 percent – 50 percent load transient

(b)

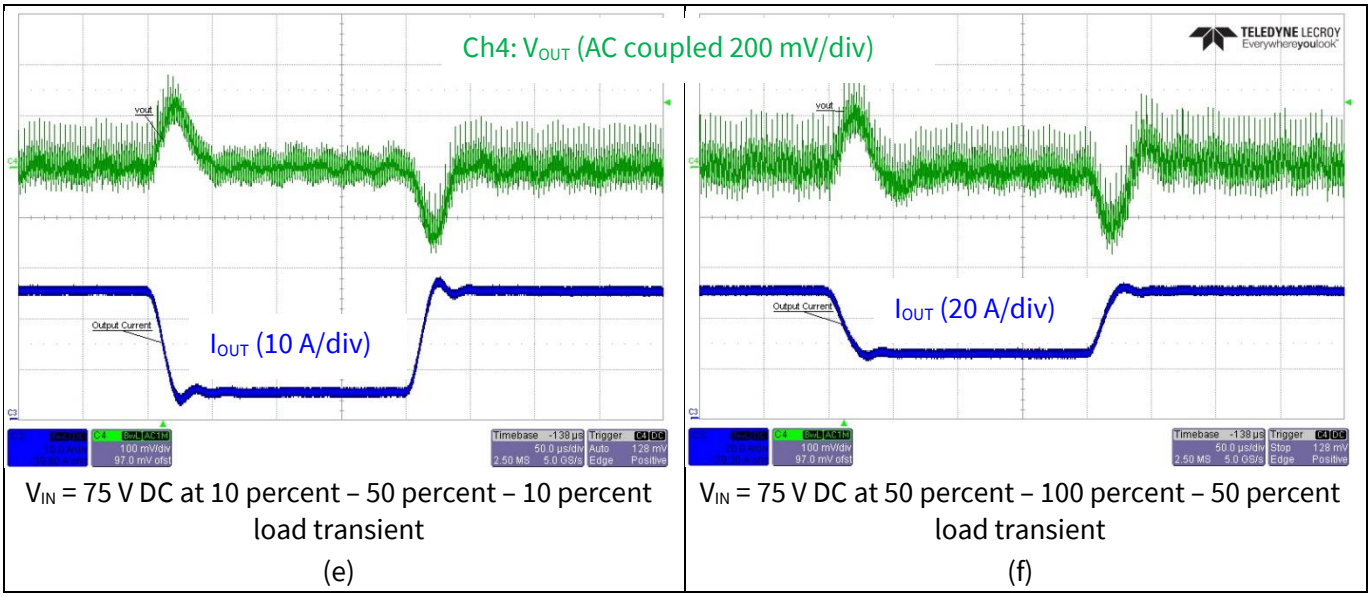


V_{IN} = 48 V DC at 10 percent – 50 percent – 10 percent load transient

(c)

V_{IN} = 48 V DC at 50 percent – 100 percent – 50 percent load transient

(d)



V_{IN} = 75 V DC at 10 percent – 50 percent – 10 percent load transient
(e)

V_{IN} = 75 V DC at 50 percent – 100 percent – 50 percent load transient
(f)

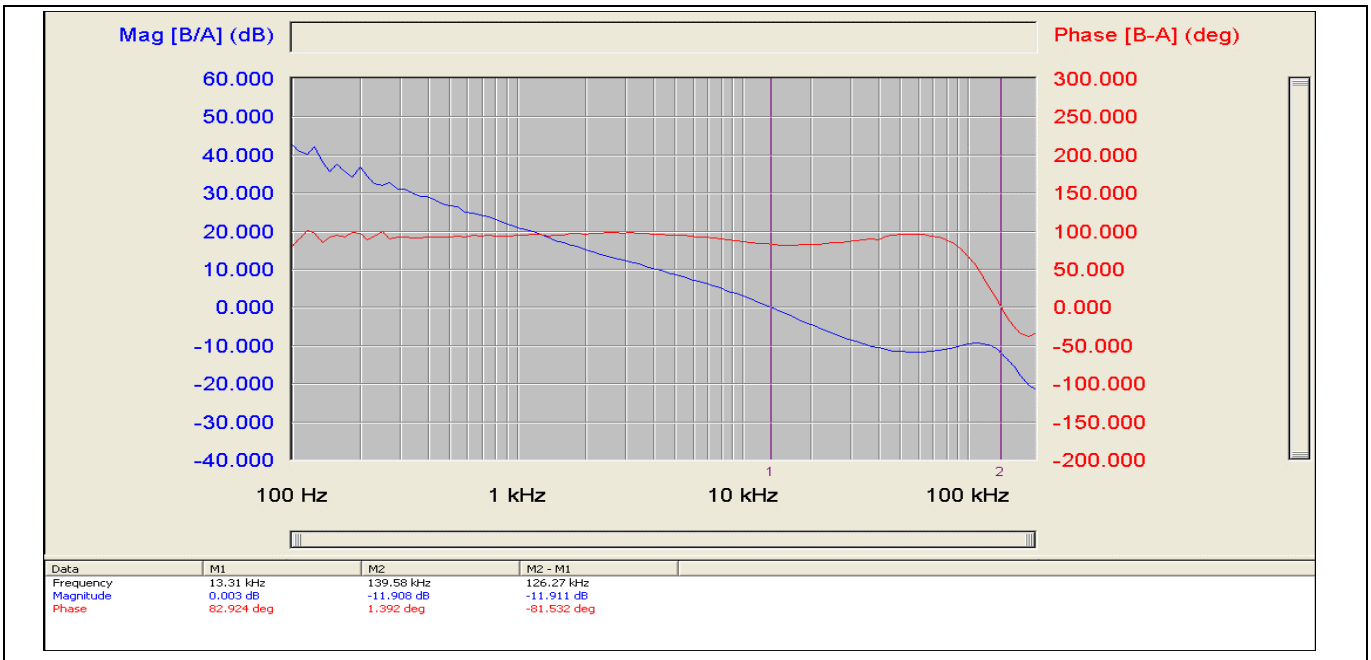
Figure 46 Load-transient waveforms

Ch4: V_{OUT} (AC coupled 200 mV/div), Ch3: I_{OUT}

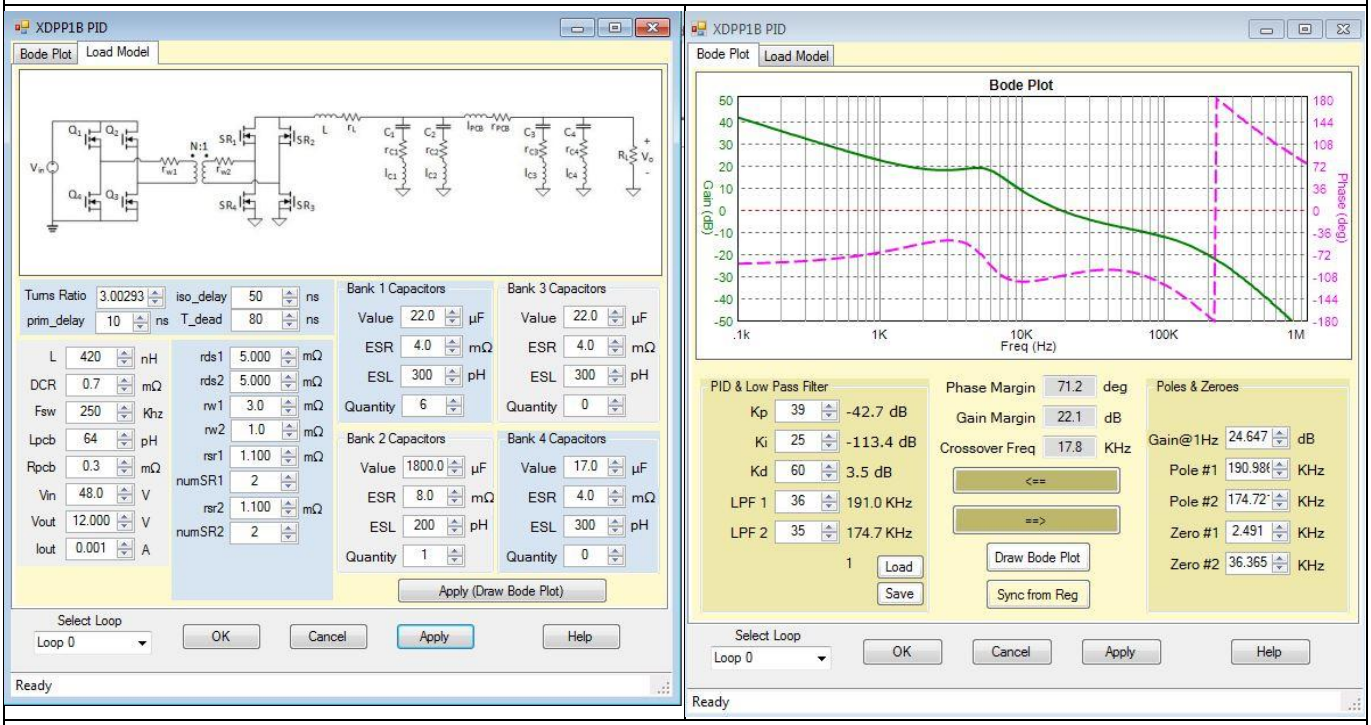
5.5 Bode response

To verify the GUI design tool, the real measured bode plots are compared against GUI predicted bode response. The accuracy of the predicted bode plot is highly dependent on the accuracy of the load model (i.e. the ESR of output capacitors, the DCR of inductor and transformer). Please find the load model in each bode plot figure section. The Bank 2 capacitors are the filter capacitors on the test fixture.

Below are measured bode response plots taken at 48 V at 0 A and 50 A.



Measured bode plot



GUI bode plot

Figure 47 Bode response at 48 V input, 0 A load

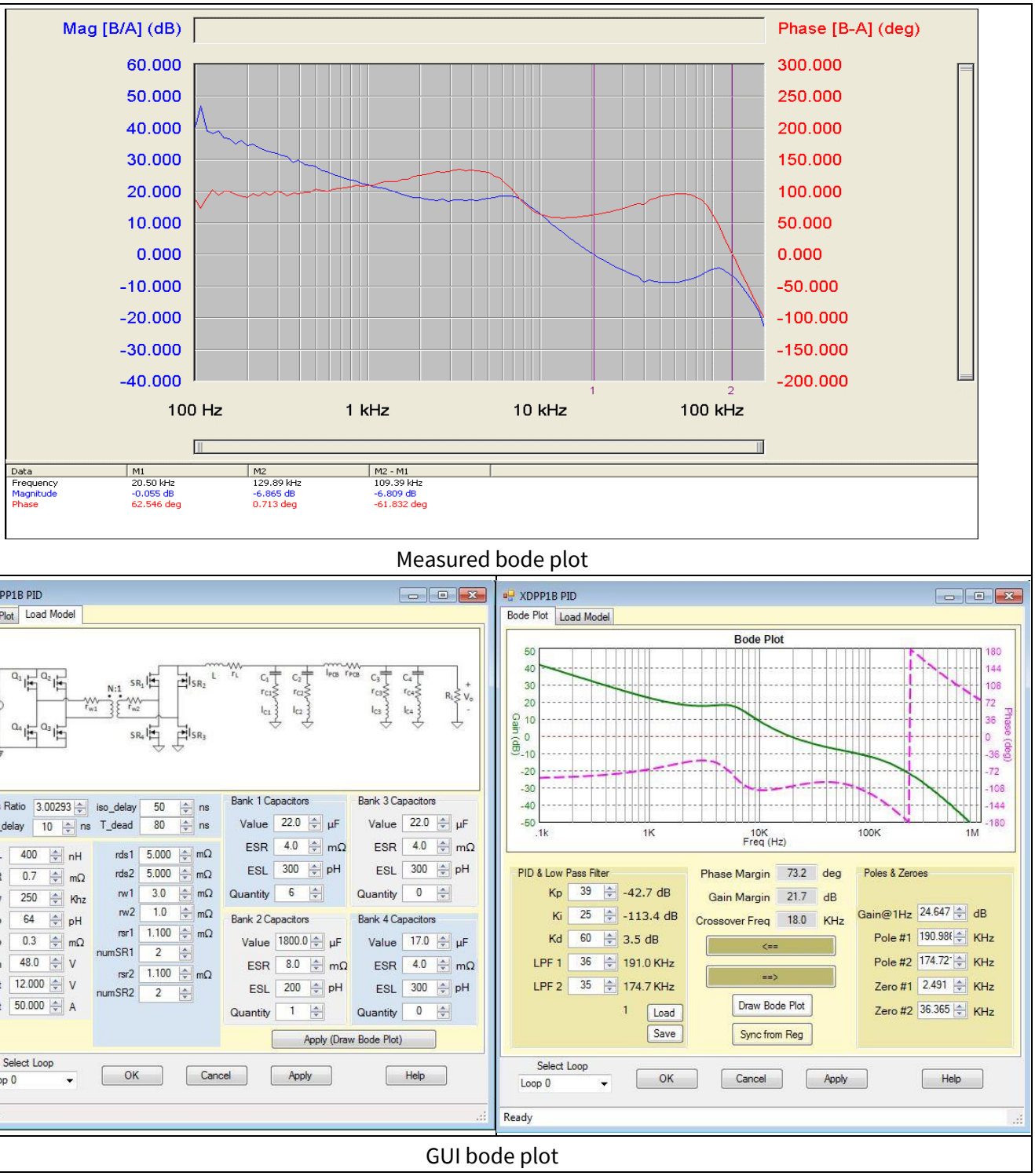


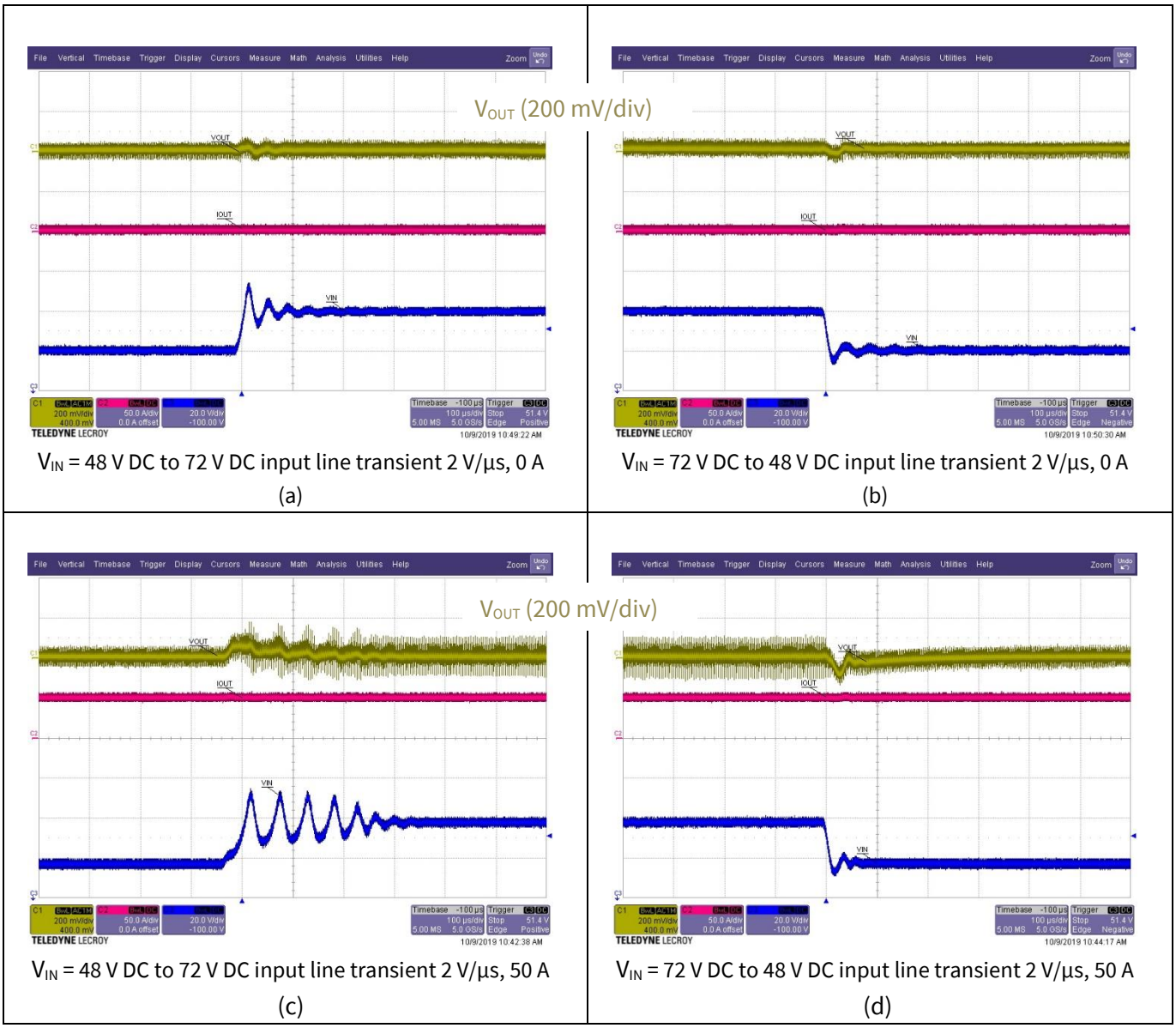
Figure 48 Bode response at V_{IN} = 48 V DC, 50 A load

It can be seen that the measured crossover is fairly close to the predicted GUI bode response at full load. The small difference in crossover frequency is most likely due to tolerances in the loop values used plus in the output filter itself. The bode plot at no-load does not exactly match the predicted response. This is because the model assumes CCM operation and in DCM the model is not accurate.

5.6 Input line transient and feed-forward

Line transient is tested with FF enabled. Set pid0_ff_vrect_sel = 0 to select V_{rect} as the source of input FF sensing. The overshoot and undershoot are less than 100 mV in the line-transient test.

Ch1 = V_{OUT} (200 mV/div), Ch2 = I_{OUT} (50 A/div), Ch3 = V_{IN} (20 V/div)



V_{IN} = 48 V DC to 72 V DC input line transient 2 V/µs, 0 A (a)

V_{IN} = 72 V DC to 48 V DC input line transient 2 V/µs, 0 A (b)

V_{IN} = 48 V DC to 72 V DC input line transient 2 V/µs, 50 A (c)

V_{IN} = 72 V DC to 48 V DC input line transient 2 V/µs, 50 A (d)

Figure 49 Input line transient waveforms

5.7 Flux balancing using VMC

The XDPP1100 implemented volt-second-based flux balancing. It uses the rectified voltage (V_{rect}) for voltage and timing measurement during each half-cycle. Error between the volt-second product of each half-cycle is fed to a PI compensation network for duty-cycle augmentation. The high-speed edge comparator ofvoltage sense front-end has 5 ns accuracy for timing measurement, enabling high-performance flux balancing.

The adjustment only applies to odd half-cycles.

$$volt\_second\_error = vdt + tdv$$

Operation waveforms

$$vdt = (vrs\_vrect\_even + vrs\_vrect\_odd) \times (cnt\_vrscomp\_even - cnt\_vrscomp\_odd)$$

$$tdv = (cnt\_vrscomp\_even + cnt\_vrscomp\_odd) \times (vrs\_vrect\_even - vrs\_vrect\_odd)$$

The following registers are used for volt-second computation. **Table 12** lists the registers of vsp1 for fbal.

Table 12 Status_Vsense registers for volt-second computation (vsp1)

Register name	Description
vsp1_vrs_vrect_even	Measured VS1 (VRSEN) ADC rectification voltage on the even half-cycle. LSB 1.25 mV Range 0 to 5.11875 V
vsp1_vrs_vrect_odd	Measured VS1 (VRSEN) ADC rectification voltage on the odd half-cycle. LSB 1.25 mV Range 0 to 5.11875 V
vsp1_cnt_vrscomp_e	Non-averaged VRS1 VRS comp. pulse width measurement result for the even half-cycle of bridge topologies. LSB 5 ns Range 0 to 10235 ns
vsp1_cnt_vrscomp_o	Non-averaged VRS1 VRS comp. pulse width measurement result for the odd half-cycle of bridge topologies. LSB 5 ns Range 0 to 10235 ns

The status registers can be read from the “common” register tab in the XDPP1100 GUI, under the Status_Vsense folder. vrs_vrect_even and vrs_vrect_odd are the VRS ADC measured voltage after a low-pass filter. The value of vrs_vrect can be estimated by input voltage V_{IN}, MFR_TRANSFORMER_SCALE, and the V_{rect} resistor-divider scale MFR_VRECT_SCALE.

MFR_TRANSFORMER_SCALE defines the transformer turns ratio; set this scale per N_S/N_P.

MFR_VRECT_SCALE is the resistor-divider ratio of V_{rect}.

For example, at 48 V input, transformer scale N_S/N_P = 1:3, V_{rect} scale = 0.073, the vrs_vrect_even and vrs_vrect_odd are expected to be approximately equal to $\frac{48V \times \frac{1}{3} \times 0.073}{1.25mV} = 934$.

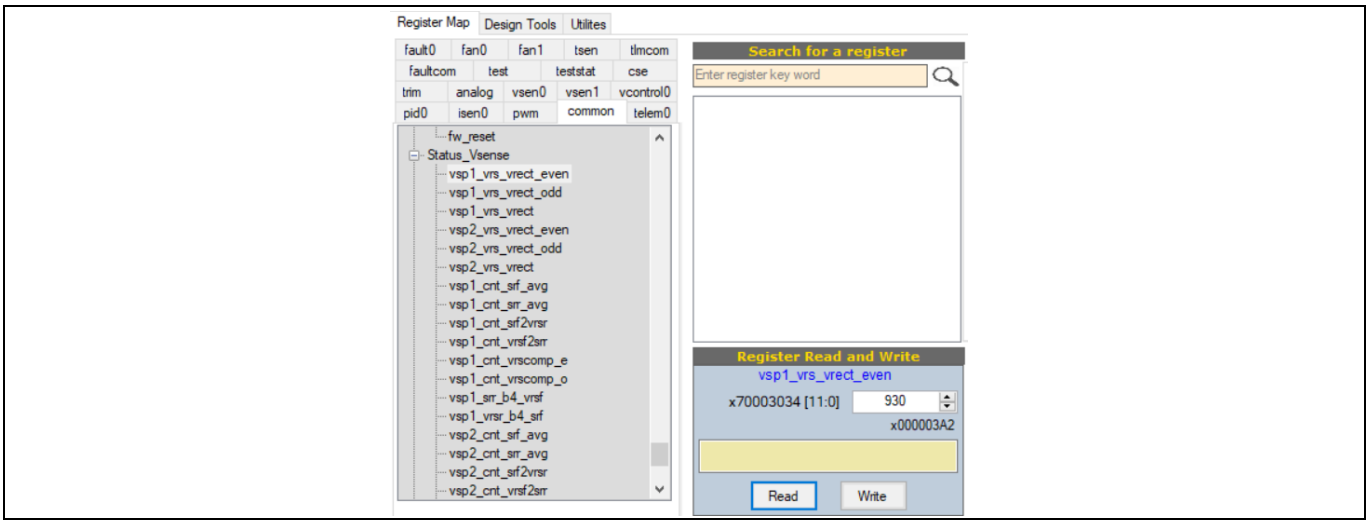


Figure 50 V_{SENSE} status registers

5.7.1 Flux balancing result with mis-matched dead-time

Flux balancing is enabled with kp_fbal = 8, ki_fbal = 30, vbal_mode_sel = 0, ramp0_dutyc_lock = 1, and fbal_time_only = 1 to enable time only balance.

Add 30 ns extra delay imbalance to one side of the primary-side gate drive using VMC. As shown below, PWM2 and PWM3 have longer dead-times than PWM1 and PWM4. This test shows how the XDPP1100 controller compensates for this flux imbalance with the gate timing offset. Note that the flux balance is disabled in DCM when load current is less than 13 A.

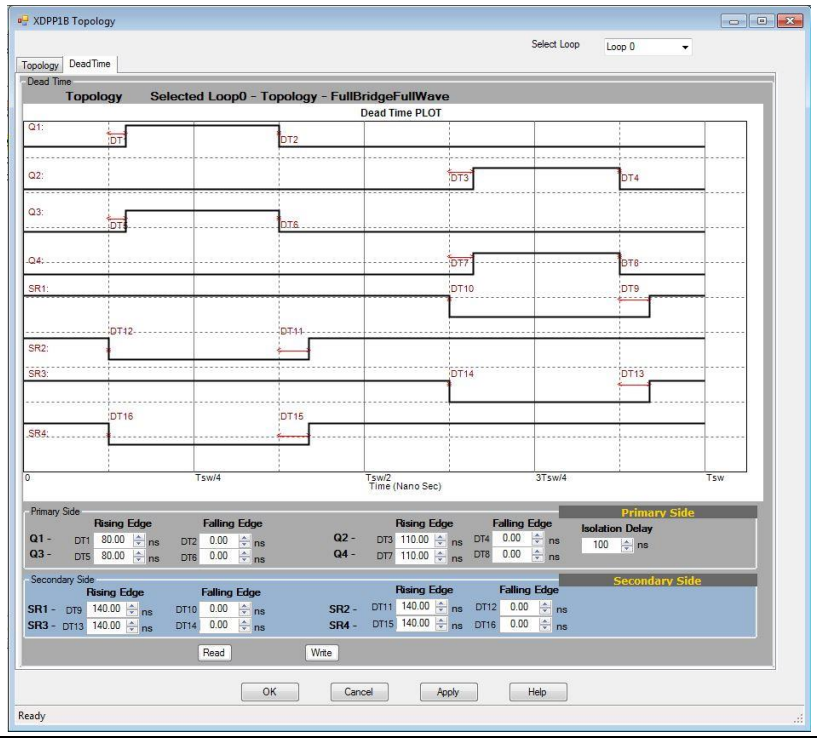


Figure 51 Dead-time configuration for flux balancing test

Table 13 took measurements across input line and load range of vsp1_vrs_vrect_odd, vsp1_vrs_vrect_even, vsp1_cnt_vrscomp_e and vsp1_cnt_vrscomp_o registers as well as photos of the switching waveforms with the 30 ns imbalance with vbal_mode_sel = 0.

Table 13 V_{rect} sense register status

V_{IN}	Output load	vsp1_vrs_vrect_odd	vsp1_vrs_vrect_even	vsp1_cnt_vrscomp_e	vsp1_cnt_vrscomp_o
36 V DC	25 A	689	687	341	340
	50 A	689	690	340	340
48 V DC	25 A	918	917	309	305
	50 A	901	896	315	314
72 V DC	25 A	1355	1353	210	211
	50 A	1313	1307	217	212

Ch1 = primary Vgs “A”, Ch2 = primary Vgs “B”, Ch3 = V_{OUT} (AC coupled), Ch4 = primary-side transformer winding

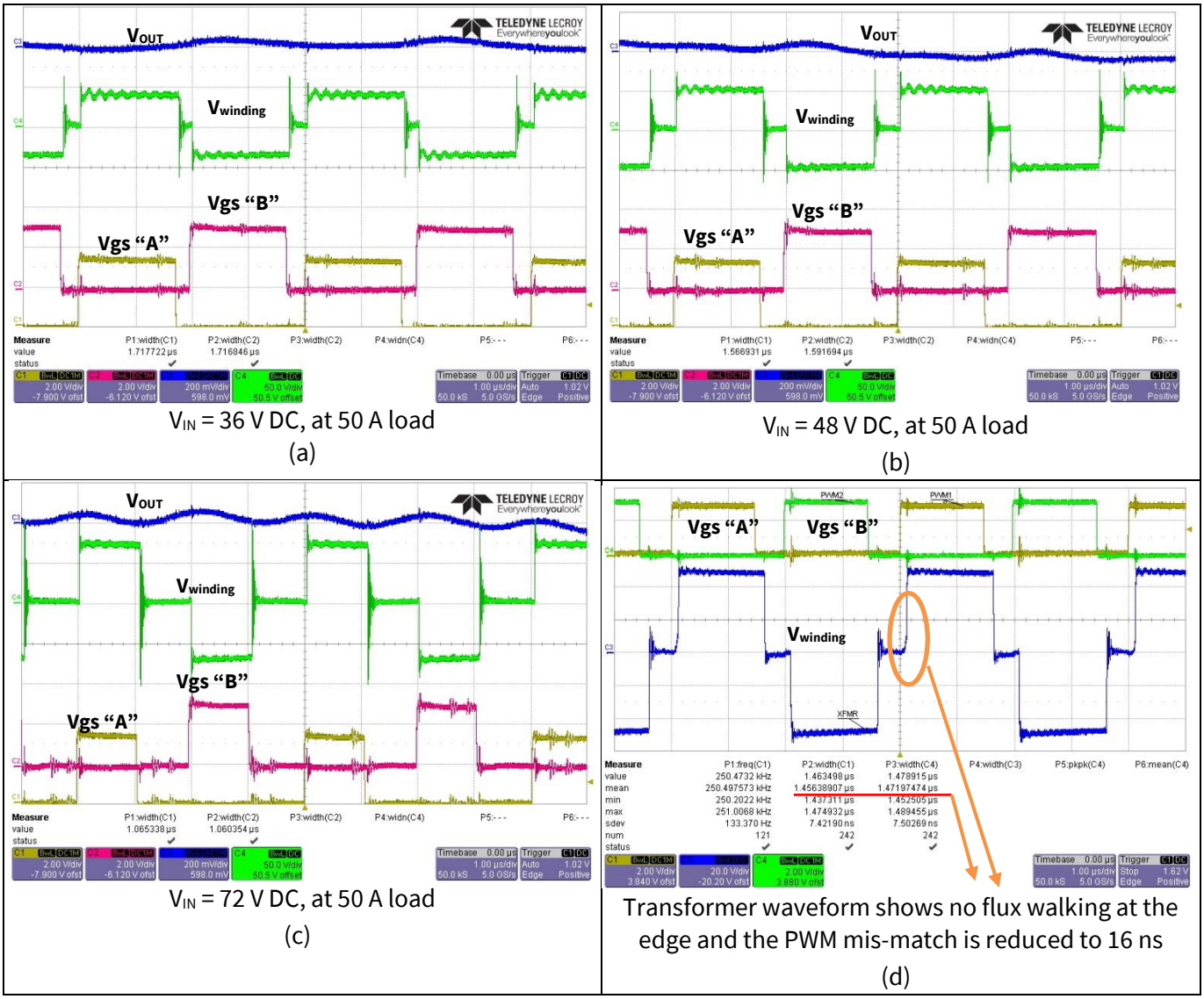


Figure 52 Flux balance waveforms with VBAL_MODE_SEL = 0

5.7.2 Output load transient with flux balancing

This test runs an output transient response with the flux balance enabled on the XDPP1100 controller. The primary-side gate drive has the 30 ns gate drive timing imbalance with vbal_mode_sel = 0. This keeps the voltage mode flux balance active. Also fbal_time_only = 1.

Ch1 = primary Vgs "A", Ch2 = primary Vgs "B", Ch3 = V_{OUT} (AC 500 mV/div), Ch4 = primary-side transformer winding

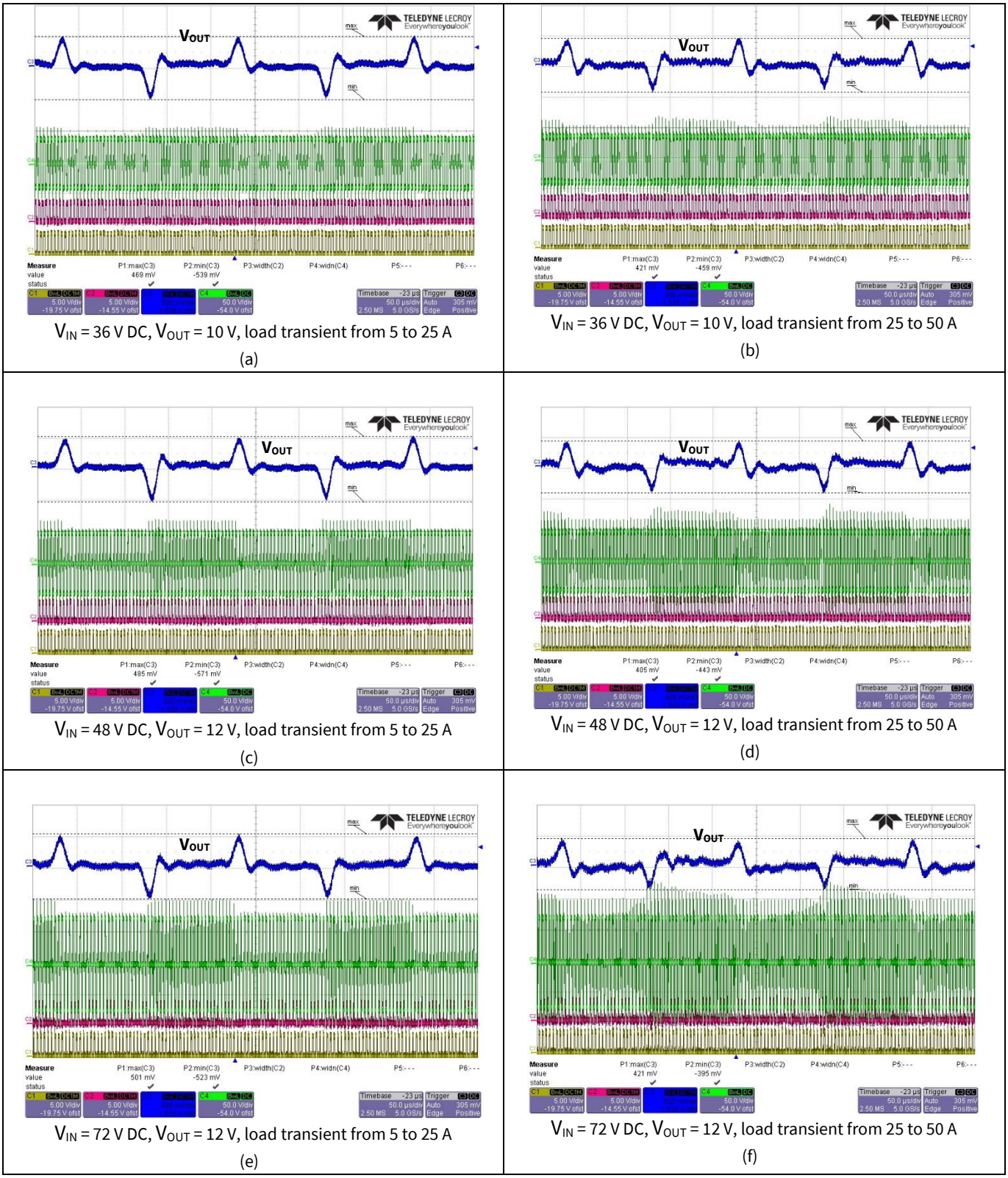


Figure 53 Output transient waveforms with 30 ns dead-time mis-match and flux balancing

It can be seen that during output transient with 30 ns primary gate-drive timing imbalance, we do not see any imbalance in the voltage waveform taken across the primary transformer winding with the flux balance of XDPP1100 enabled.

5.7.3 Output turn-on/-off with 30 ns primary gate-drive timing imbalance

Switching waveforms during output turn-on and turn-off with 30 ns primary gate-drive timing imbalance with XDPP1100 flux balance enabled, vbal_mode_sel = 0. Also fbal_time_only = 0.

Ch1 = primary Vgs “A”, Ch2 = primary Vgs “B”, Ch3 = V_{OUT}, Ch4 = primary-side transformer winding

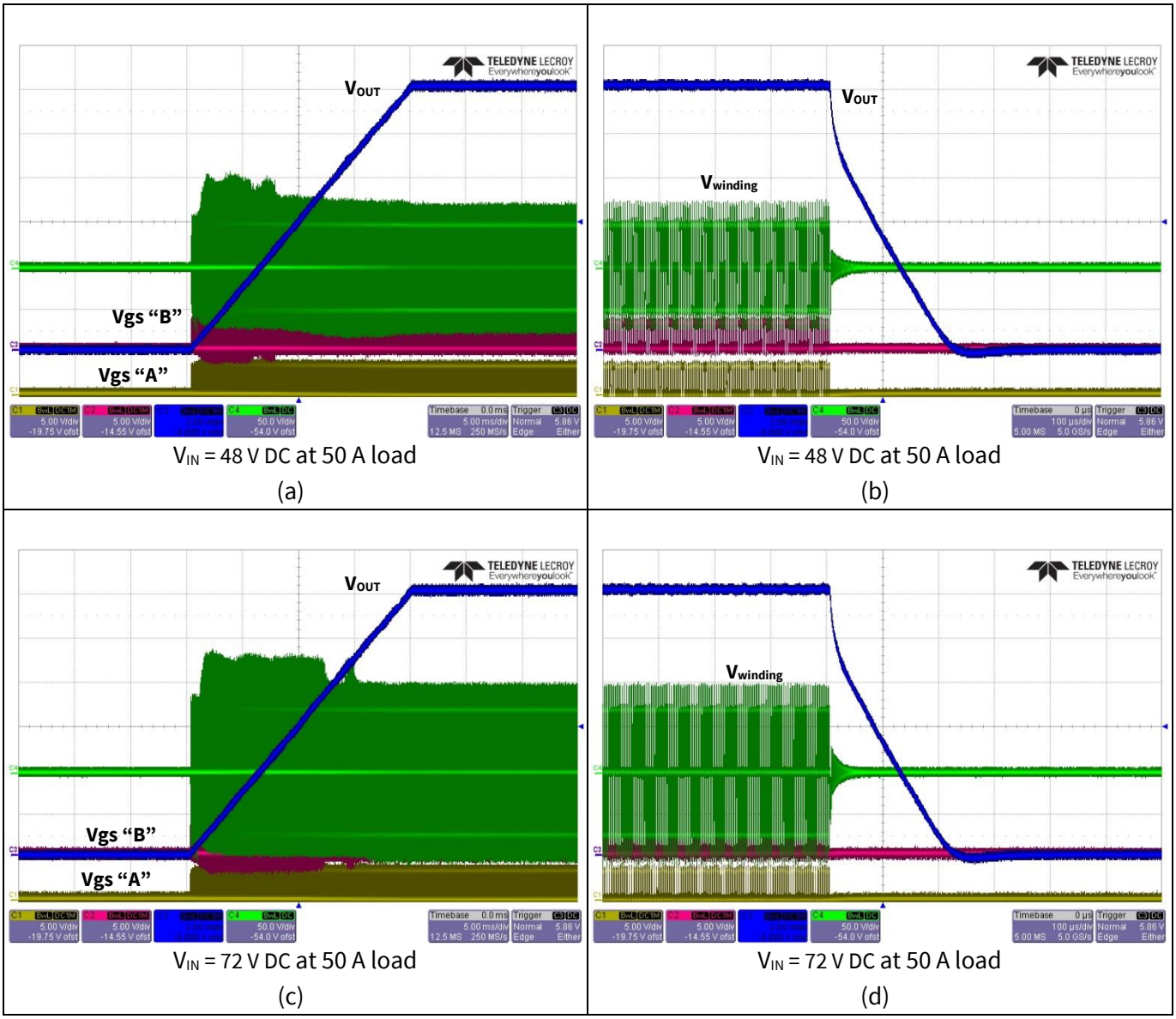


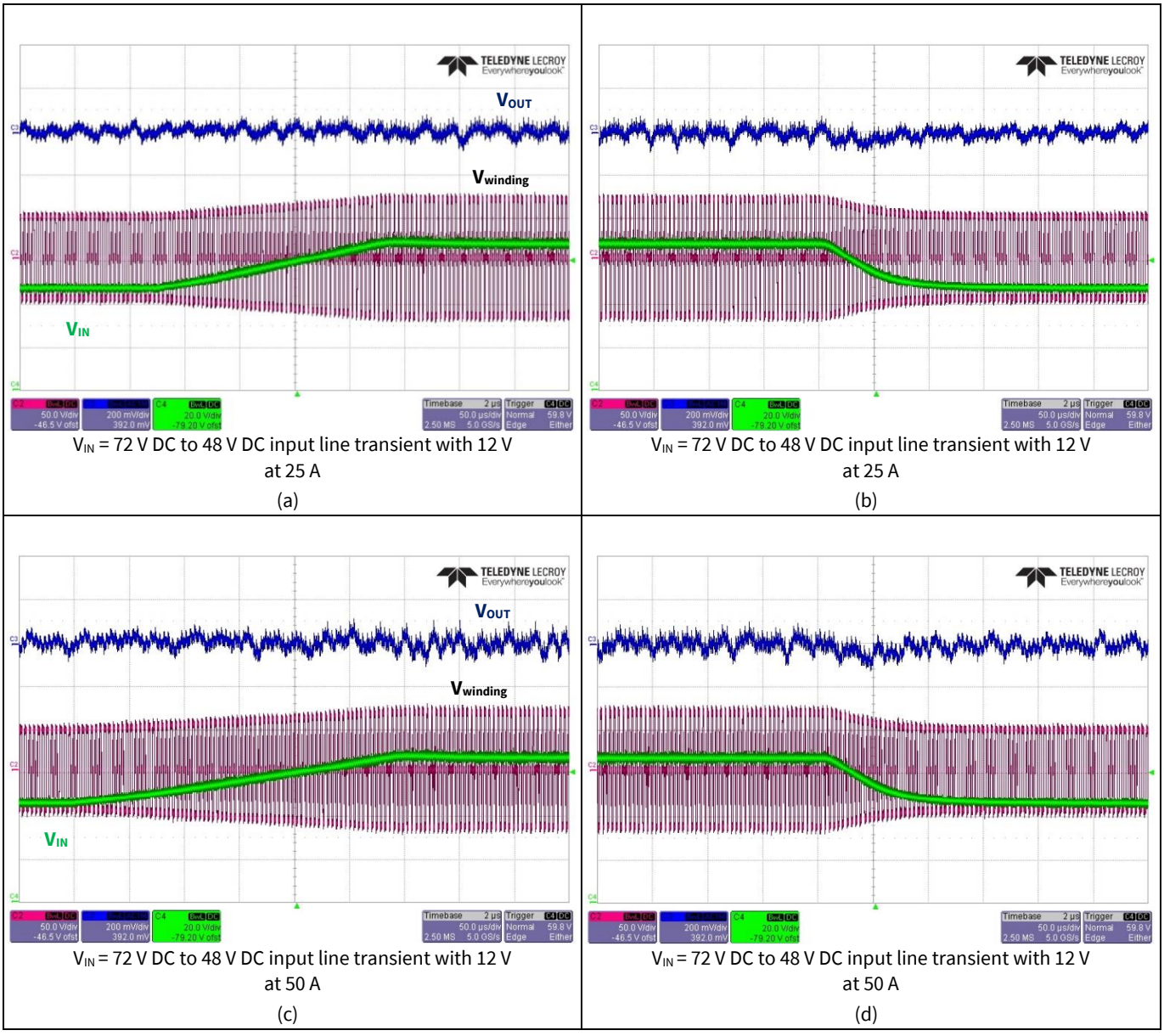
Figure 54 Output turn-on and -off with gate-drive imbalance at V_{IN} = 48 V DC and 72 V DC

The start-up and shutdown waveforms show no issue with the 30 ns imbalance when the flux balance is enabled.

5.7.4 Flux balance during input transient with VMC

An input line transient was applied to the quarter-brick and the switching waveforms were recorded with the 30 ns imbalance dead-time, tested at 0.33 V/µs V_{IN} slew rate. In this test, fbal_time_only = 0 and vbal_mode_sel = 0.

Ch2 = primary-side transformer winding (50 V/div), Ch3 = V_{OUT} (200 mV/div, AC coupled), Ch4 = V_{IN} (20 V/div)



V_{IN} = 72 V DC to 48 V DC input line transient with 12 V at 25 A
(a)

V_{IN} = 72 V DC to 48 V DC input line transient with 12 V at 25 A
(b)

V_{IN} = 72 V DC to 48 V DC input line transient with 12 V at 50 A
(c)

V_{IN} = 72 V DC to 48 V DC input line transient with 12 V at 50 A
(d)

Figure 55 Flux balance during input line transient

Line transient waveforms show the power supply had no issues with the 30 ns imbalance.

5.8 Burst mode operation

To increase light load efficiency, the converter could enter burst mode to reduce switching losses. The burst operation is enabled by setting PMBus command 0x34 POWER_MODE = 0.

The burst entry threshold is defined by register pid0_burst_mode_ith; LSB of this register is IOUT_APC/2. For example, the IOUT_APC of this demo board is 0.334 A configured by PMBus MFR_IOUT_APC of Loop1. The LSB of the burst threshold is 0.167 A.

Operation waveforms

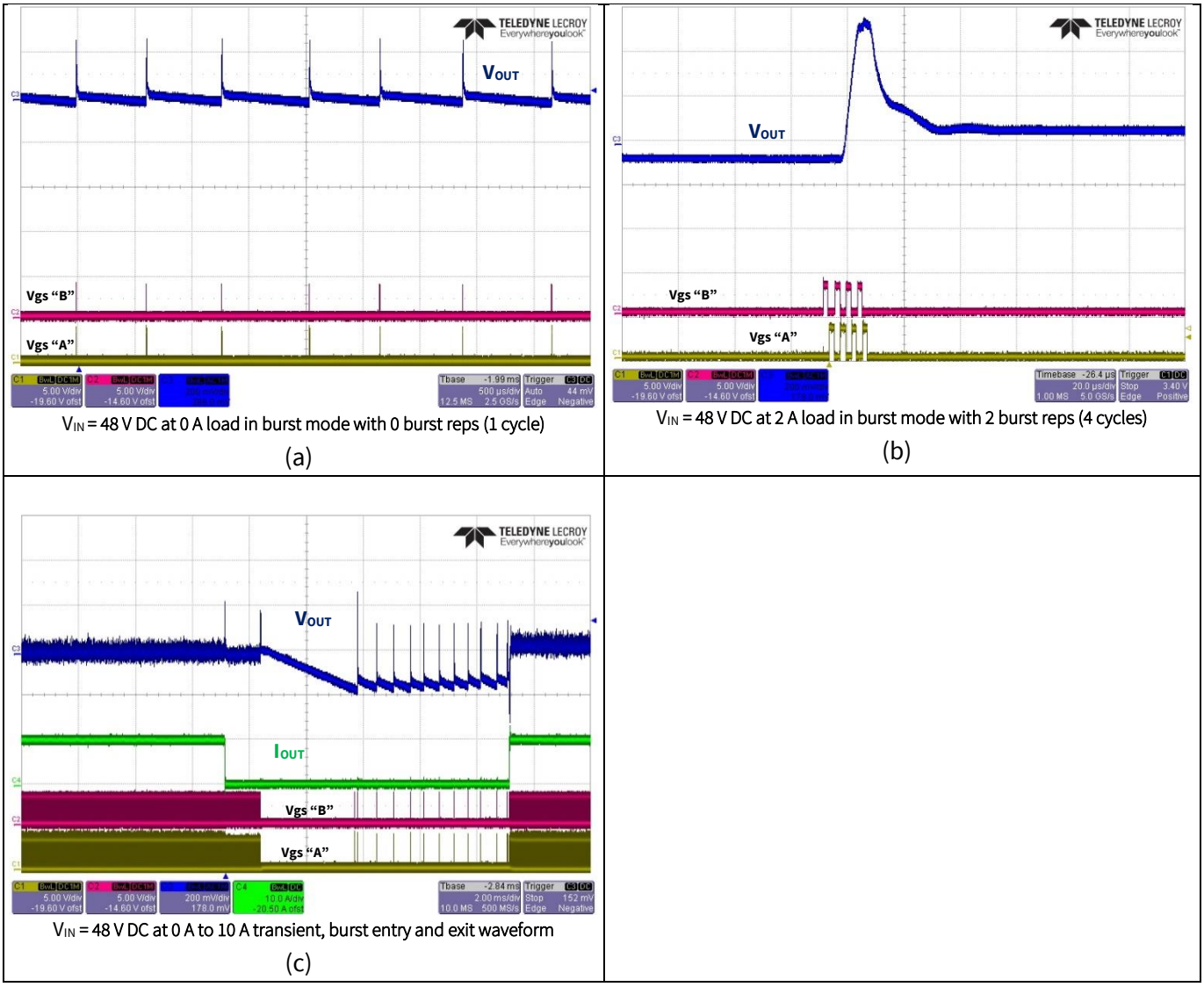
The burst error is configured by register pid0_burst_mode_err_thr, with resolution 1.25 mV. It defines the error voltage at the VSEN pin, thus the output ripple will be:

$$Burst_{ripple} = \frac{\text{pid0\_burst\_mode\_err\_thr} * 1.25\text{mV}}{VOUT\_SCALE\_LOOP}$$

When the load current falls below the desired entry current level, the converter enters burst mode operation. The converter stops switching when entering burst (burst-off). Switching is resumed when the output voltage drops more than the burst error threshold. In burst mode, PID output is frozen to the value prior entering burst. Thus during the burst-on period, the converter works in constant on-time mode. The number of switching cycles in a burst-on period is defined by register pid0_burst_reps. A higher number count can be used to increase the inductor peak current in a burst event, which will increase the burst-off time at a given load condition, thus reducing the averaged power loss. On the other hand, higher burst count results in higher voltage ripple. The optimized value should be determined by the load of burst and the desired output ripple. The SRs are turned off during burst mode. For bridge topologies, the positive and negative half-cycles occur in pairs.

Burst mode configuration:
Pid0_burst_mode_ith = 50, Pid0_burst_mode_err_thr = 15, and 0x34 POWER_MODE = 0.

Ch1 = primary Vgs “A”, Ch2 = primary Vgs “B”, Ch3 = V_{OUT} (200 mV/div, AC coupled), Ch4 = I_{OUT} (10 A/div)



V_{IN} = 48 V DC at 0 A load in burst mode with 0 burst reps (1 cycle)

(a)

V_{IN} = 48 V DC at 2 A load in burst mode with 2 burst reps (4 cycles)

(b)

V_{IN} = 48 V DC at 0 A to 10 A transient, burst entry and exit waveform

(c)

Figure 56 Burst mode operation

6 Protections

In this section, input and output fault protections are verified with different types of fault response. The default fault threhsolds and fault response of the board are listed below.

Table 14 Default fault protection configuration

Protection type		Default value (PMBus configurable)	Unit
Output over-voltage	Fault limit threshold	14	V
	Warn limit threshold	13.5	V
	Fault response	Disable and retry, no retry	
Output under-voltage	Fault limit threshold	8	V
	Warn limit threshold	9	V
	Fault response	Ignore fault	
Output over-current	Fault limit threshold	60	A
	Warn limit threshold	56	A
	Fault response	Operate for delay time 2 ms, retry once with 2 ms delay	
Output under-current	Fault limit threshold	-128	A
	Fault response	Disable and retry, no retry	
Over-temperature	Fault limit threshold	125	°C
	Warn limit threshold	90	°C
	Fault response	Disable and resume when OK, fault clears when on-board NTC temperature falls below the warn limit	
Under-temperature	Fault limit threshold	-40	°C
	Warn limit threshold	-35	°C
	Fault response	Ignore fault	
Input over-voltage	Fault limit threshold	80	V
	Warn limit threshold	78	V
	Fault response	Disable and retry, no retry	
Input under-voltage	Fault limit threshold	31	V
	Warn limit threshold	33	V
	Fault response	Ignore fault	
Input over-current	Fault limit threshold	20	A
	Warn limit threshold	17	A
	Fault response	Disable and retry, no retry	
Max. output voltage turn-on rise time	Fault limit threshold	255	ms
	Fault response	Ignore fault	
Output over-current fast fault or short-circuit	Fault limit threshold	65	A
	Fault response	Shut down and no retry	

The fault threshold and response can be configured by the design tool “Fault Protections”. The XDPP1100 also allows the user to configure the sensitivity of the fault detection. The “Fault Configuration” tab configures the fault registers that define the consecutive fault count and the hysteresis of the fault comparator. More details of the fault and protections can be found in the XDPP1100 application note.

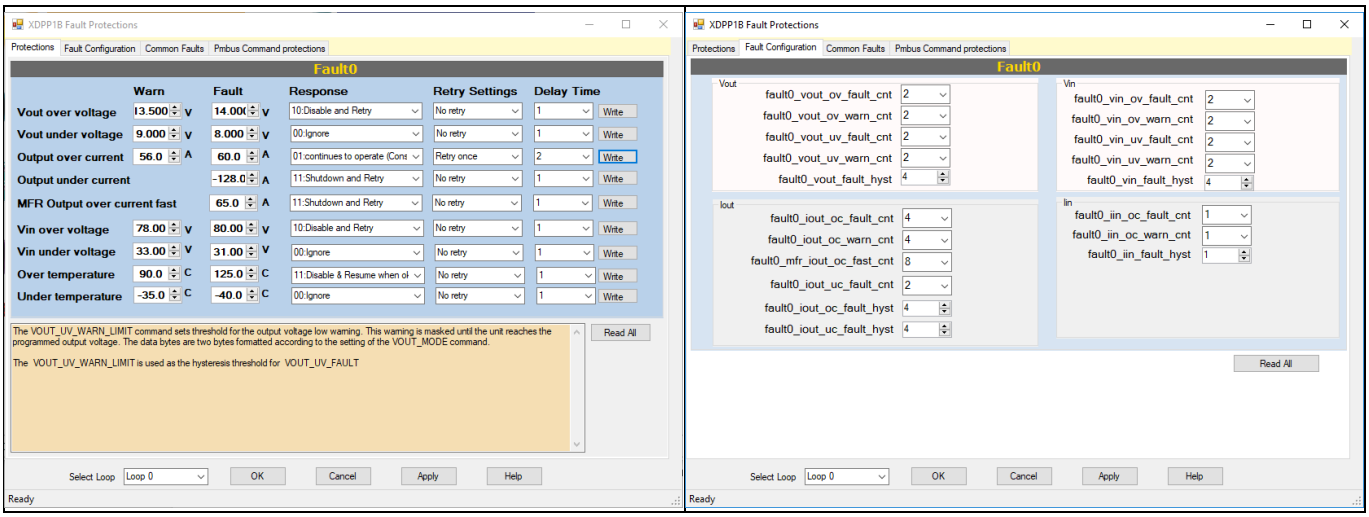
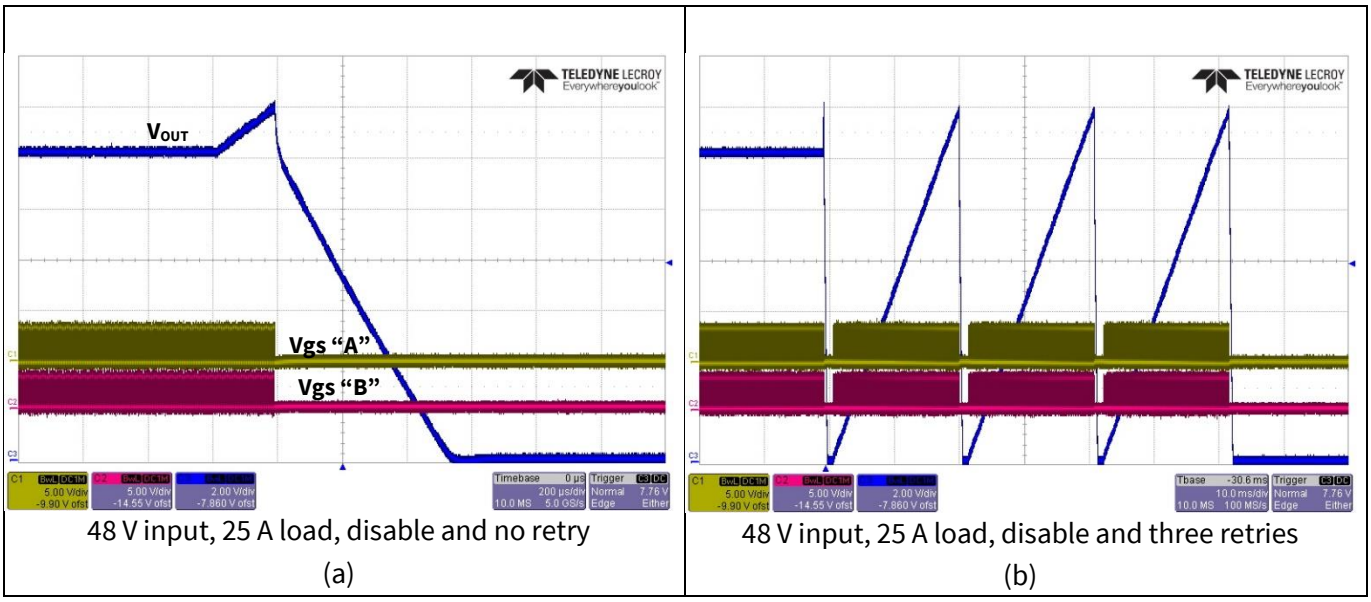


Figure 57 Fault Protections design tool

6.1 Output OVP

Ch1 = primary Vgs “A”, Ch2 = primary Vgs “B”, Ch3 = V_{OUT}



48 V input, 25 A load, disable and no retry

(a)

48 V input, 25 A load, disable and three retries

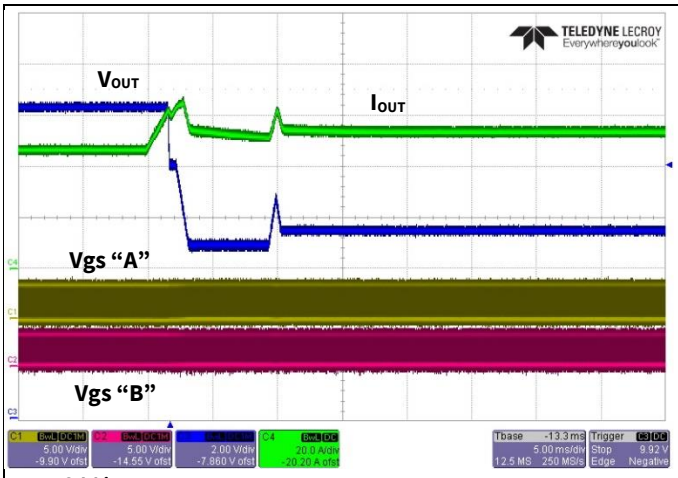
(b)

Figure 58 Output OVP waveform

6.2 Output OCP

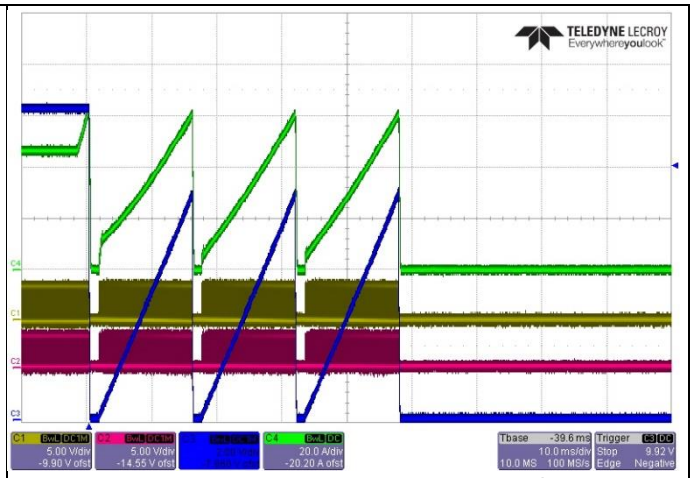
Ch1 = primary Vgs “A”, Ch2 = primary Vgs “B”, Ch3 = V_{OUT}, Ch4 = I_{OUT}

Set e-load to CR mode for constant current test.



48 V input, 50 A to over-current, constant current

(a)



48 V input, 50 A to over-current, shutdown with three retries

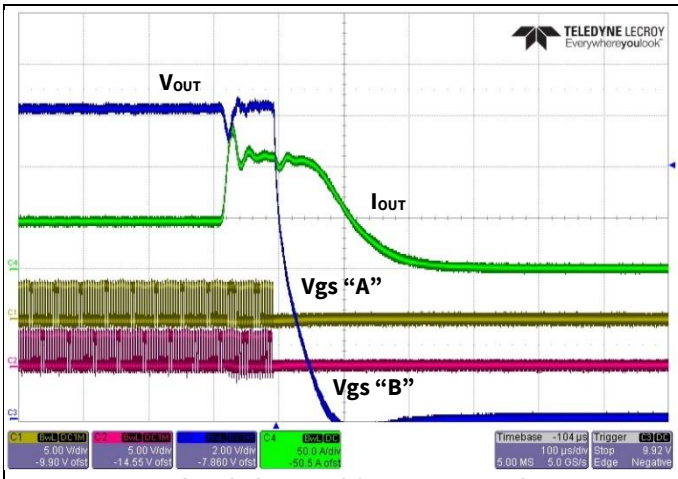
(b)

Figure 59 Output OCP waveforms

6.3 Output short-circuit protection

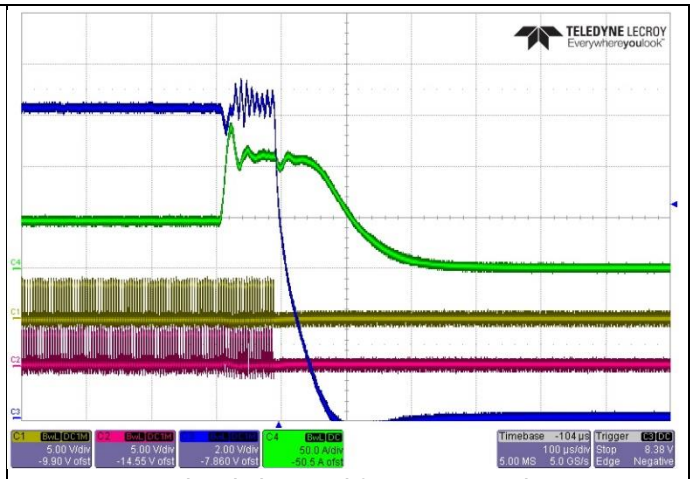
The output was shorted with a load bank.

Ch1 = primary Vgs “A”, Ch2 = primary Vgs “B”, Ch3 = V_{OUT} (2 V/div), Ch4 = I_{OUT} (50 A/div)



V_{IN} = 48 V DC, load changed from 50 A to short-circuit with load bank

(a)



V_{IN} = 75 V DC, load changed from 50 A to short-circuit with load bank

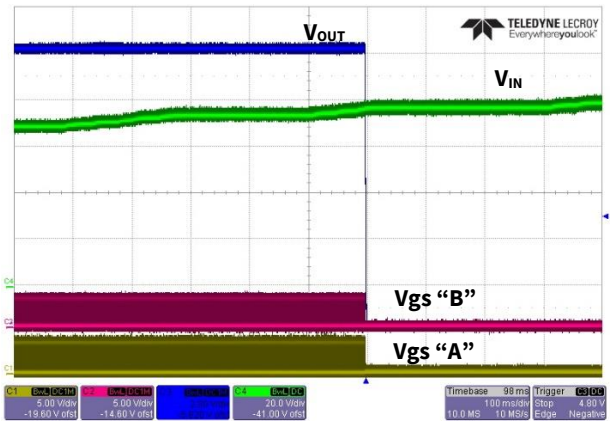
(b)

Figure 60 Output short-circuit waveforms using load bank

6.4 Input OVP

When the input voltage is sensed from the secondary side by V_{rect} sensing, input over-voltage shutdown will be latched shutdown. The converter could resume operation after the fault is cleared, Figure 61 (a).

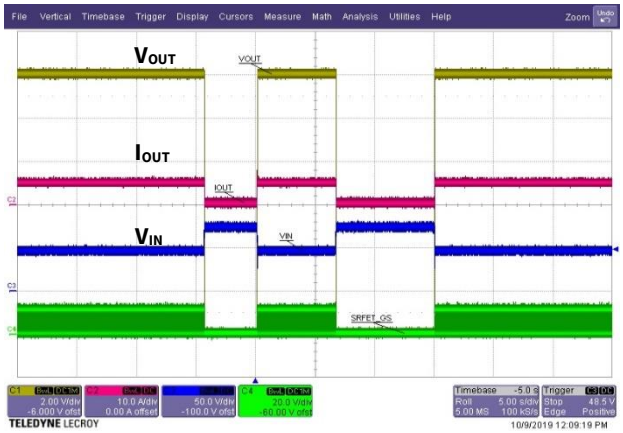
With the help of the PRISEN circuit, the input voltage sensing could transfer from V_{rect} sensing to PRISEN sensing after a fault shutdown. The converter could countinously monitor the input voltage and resume operation once the fault is cleared, Figure 61 (b).



V_{IN} = ramped up to 80 V DC at 25 A load

(a)

Ch1 = primary Vgs "A", Ch2 = primary Vgs "B",
Ch3 = V_{OUT} (2 V/div), Ch4 = V_{IN} (20 V/div)



Input voltage stepped between 48 V and 80 V,
input OV resume when OK

(b)

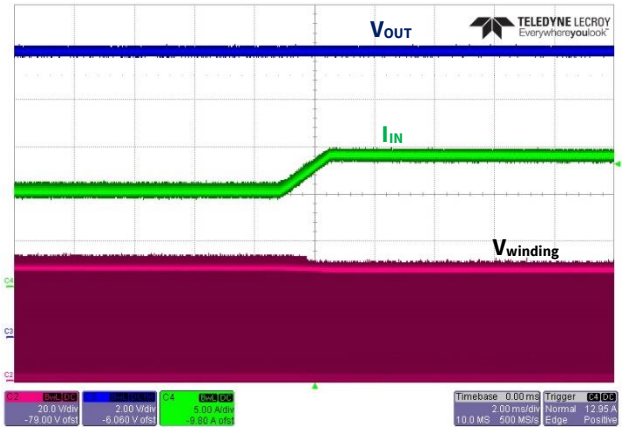
Ch1 = V_{OUT} (2 V/div), Ch2 = I_{OUT} (10 A/div),
Ch3 = V_{IN} (50 V/div), Ch4 = SR gate drive (20 V/div)

Figure 61 V_{IN} OV fault protection

6.5 Input OCP

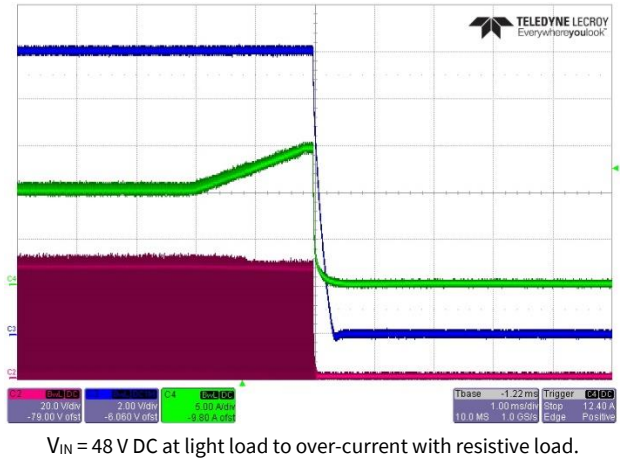
Note: Output current limit and output power limit were raised so as to not interfere with the test.

Ch2 = primary-side transformer winding, Ch3 = V_{OUT} (2 V/div), Ch4 = I_{IN} (5 A/div)



V_{IN} = 48 V DC at light load to over-current with resistive load.
Input over-current set to ignore over-current fault.

(a)



V_{IN} = 48 V DC at light load to over-current with resistive load.
Input over-current set to disable and no retry.

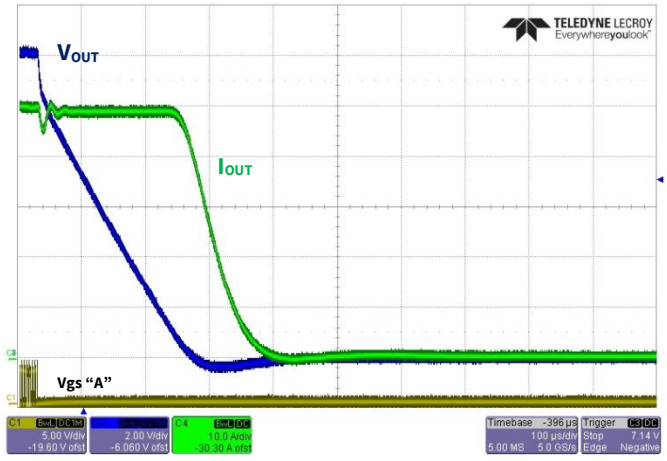
(b)

Figure 62 Input OCP waveforms

6.6 Over-temperature protection

The quarter-brick has two thermistors with one located next to the CS copper trace and the other located next to Q14. Over-temperature was tested by reducing the airflow over the unit under test while operating at full load. For the disable and resume when OK waveform, the fault warning threshold is placed close to the fault threshold to see the output resuming quickly.

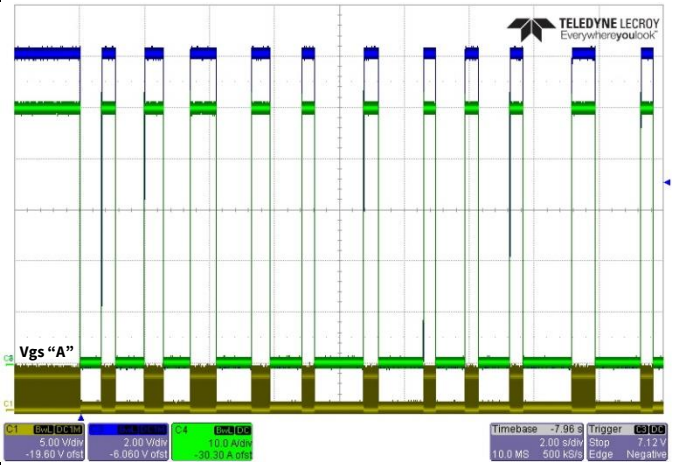
Ch1 = primary Vgs “A”, Ch3 = V_{OUT} (2 V/div), Ch4 = I_{OUT} (10 A/div)



V_{IN} = 48 V DC at 50 A load during over-temperature shutdown

Disable and no retry

(a)



V_{IN} = 48 V DC at 50 A load during over-temperature shutdown

Disable and resume when OK

(b)

Figure 63 Over-temperature shutdown

7 Current sharing

The XDPP1100 supports both passive current sharing by the load line, and active current sharing by IMON.

Load-line (droop) current sharing can be implemented without any external components or circuit. The downside is that the load regulation is degraded. The maximum output power of each unit is reduced due to the reduced output voltage at the maximum rated current.

Active current sharing involves using a current sharing wire, which connects all parallel modules to communicate average current information between modules. The XDPP1100 offers a single-wire active current sharing feature. **Figure 64** shows the active current sharing example with two units in parallel.

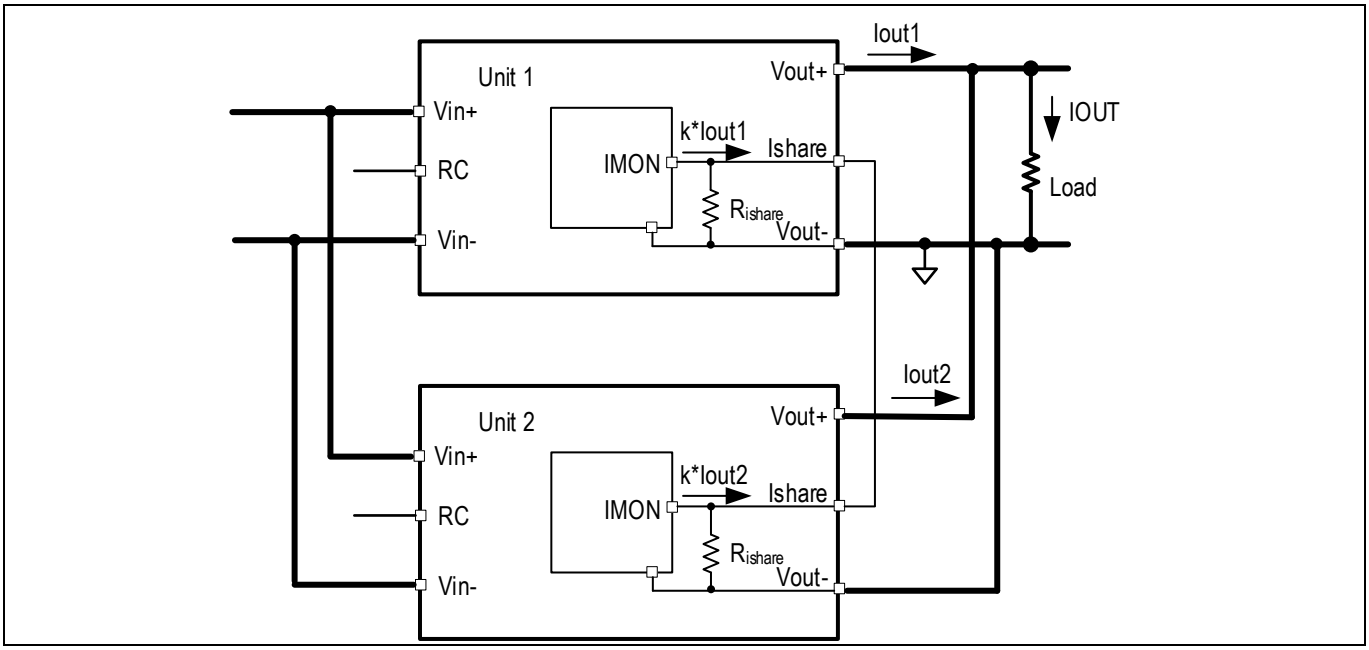


Figure 64 XDPP1100 active current sharing

IMON is an analog DAC output representing the output current. IMON is used for output current monitoring, and for active current balancing between multiple parallel modules. An internal current source proportional to the output current of Loop0 sources comes out from the IMON pin. The IMON current DAC (IDAC) output current range is 0 to 640 µA. The gain of the current source is configurable, which allows the user to scale the current source per application. At no-load, this source current is 320 µA. IMON source current lower than 320 µA indicates negative current in this module.

A 1.875 k Ω precision resistor (R_{ishare}) connected between IMON and ground presents a voltage proportional to the output current of each module. At full load, the IMON voltage will be 1.2 V (640 µA x 1.875 k Ω); and at no-load, IMON voltage is 0.6 V (320 µA x 1.875 k Ω).

Connecting the IMON of each module together allows the XDPP1100 to detect the level of average current.

$$IOUT = Iout1 + Iout2 + \cdots + Ioutn$$

$$V_{IMON} = (k \cdot Iout1 + k \cdot Iout2 + \cdots + k \cdot Ioutn) \times \frac{R_{ishare}}{n} = k \cdot R_{ishare} \times \frac{IOUT}{n}$$

I_{OUT} is total current supplied to load, *n* is the number of units that are connected in parallel, *k* is the IMON source current scale factor. The voltage of the IMON pin represents the average current.

Each module compares its own output current with the average current, therefore making the corresponding adjustment.

Current sharing

To prevent oscillation on a small error current, a dead zone applies to the current sharing block. When the error current is less than the dead zone, current sharing is inactive.

The XDPP1100 provides both positive and negative clamps to voltage adjustment under active current sharing.

The active current sharing configuration can be done with the GUI design tool, under the “Advanced Features”.

Current sharing during start-up is always more challenging than in steady-state. The power supplies could have different start-up delays or different ramp times due to device variation. The voltage difference between units could be much more than the set-point error in the steady-state.

An added_droop feature was implemented in the FW patch. The droop is added during start-up ramp. The added_droop helps to reduce the error of current sharing at start-up. It is removed once the power supply reaches regulation, thus the max. output power won’t be sacrificed. It could be configured by the patched PMBus command 0xFC MFR_ ADDED_DROOP_ DURING_RAMP. Use the “Load PMBus Spread Sheet” button to import the MFR PMBus command into GUI. The PMBus command spreadsheet can be found in the GUI installation folder.

More details of current sharing can be found in the XDPP1100 application note.

A test fixture that could fit three quarter-bricks is designed for the current sharing test. In this test, two units were placed in parallel to verify the current sharing performance. Output voltge mis-match was set intentionally to check the worst case. The current sharing by linear droop and by IMON active current sharing are compared.

7.1.1 Start-up waveform with V_{OUT} mis-match = 100 mV

Unit 1, VOUT_COMMAND = 11.95 V, xaddr 0x41
Unit 2, VOUT_COMMAND = 12.05 V, xaddr 0x40

Test case 1: active current sharing is disabled, current sharing by droop only

- Added droop is 14 mΩ at ramp and reduced to 9 mΩ at regulation
- vc0_vavp_kfp = 24 (output voltage sense low-pass filter)
- vc0_vavp_clamp_neg = 0 (negative droop clamp)
- vc0_vavp_clamp_pos = 24 (positive droop clamp, -480 mV at V_{OUT})
- Enable DE start-up of one unit (can be either unit 1 or unit 2); the waveform is taken with unit 2 DE start-up enabled

Test case 2: active current sharing is enabled

- No added droop at ramp, standard droop 4 m Ω at regulation
- vc0_vavp_kfp = 24
- Ishr_scale = 10 (current share scale, defined per the maximum output current 50 A)
- ishr_ki = 8, ishr_kp = 0 (active current share PI filter)
- ishare_clamp_neg = 2 (negative clamp, -25 mV at V_{OUT})
- ishare_clamp_pos = 10 (positive clamp, +125 mV at V_{OUT})
- MFR_ISHARE_THRESHOLD = 0x0002 (2 A)
- Enable unit 2 DE start-up

Ch1: I_{OUT1} of unit 1 (5 A/div), Ch2: V_{OUT} (2 V/div), Ch3: IMON pin (0.5 V/div), Ch4: I_{OUT2} of unit 2 (5 A/div)

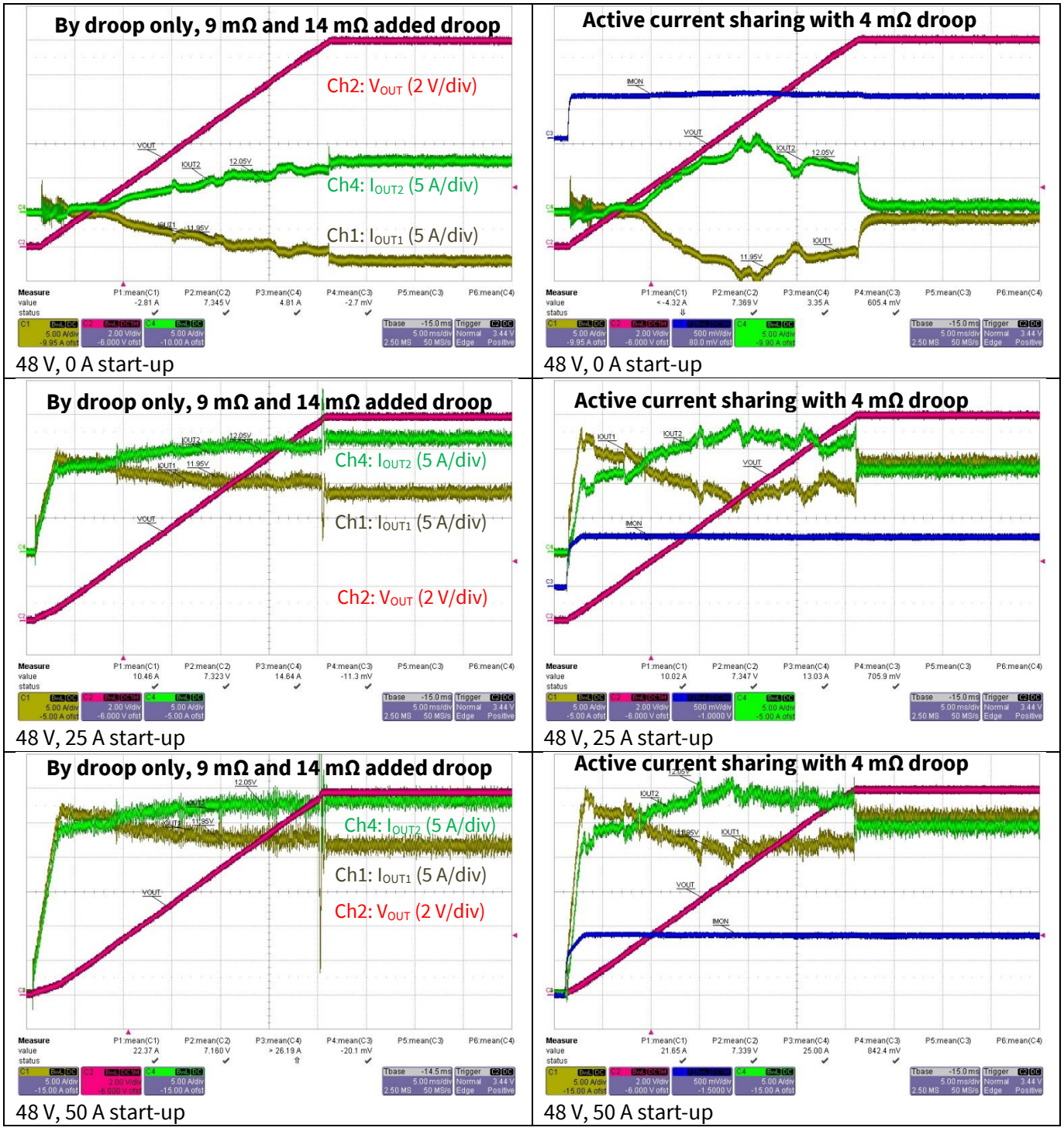


Figure 65 Current sharing waveform at start-up

It is obvious that the active current sharing has much better result than the droop-based current sharing, especially in regulation state. It could bring the currents in each module close to each other. The error at start-up ramp could be reduced by adding droop resistance to the ramp.

7.1.2 Load-transient waveform with V_{OUT} mis-match = 100 mV

Unit 1, VOUT_COMMAND = 11.95 V, xaddr 0x41
Unit 2, VOUT_COMMAND = 12.05 V, xaddr 0x40

Ch1: I_{OUT1} of unit#1 (5 A/div), Ch2: V_{OUT} (2 V/div), Ch3: IMON pin (0.5 V/div), Ch4: I_{OUT2} of unit 2 (5 A/div)

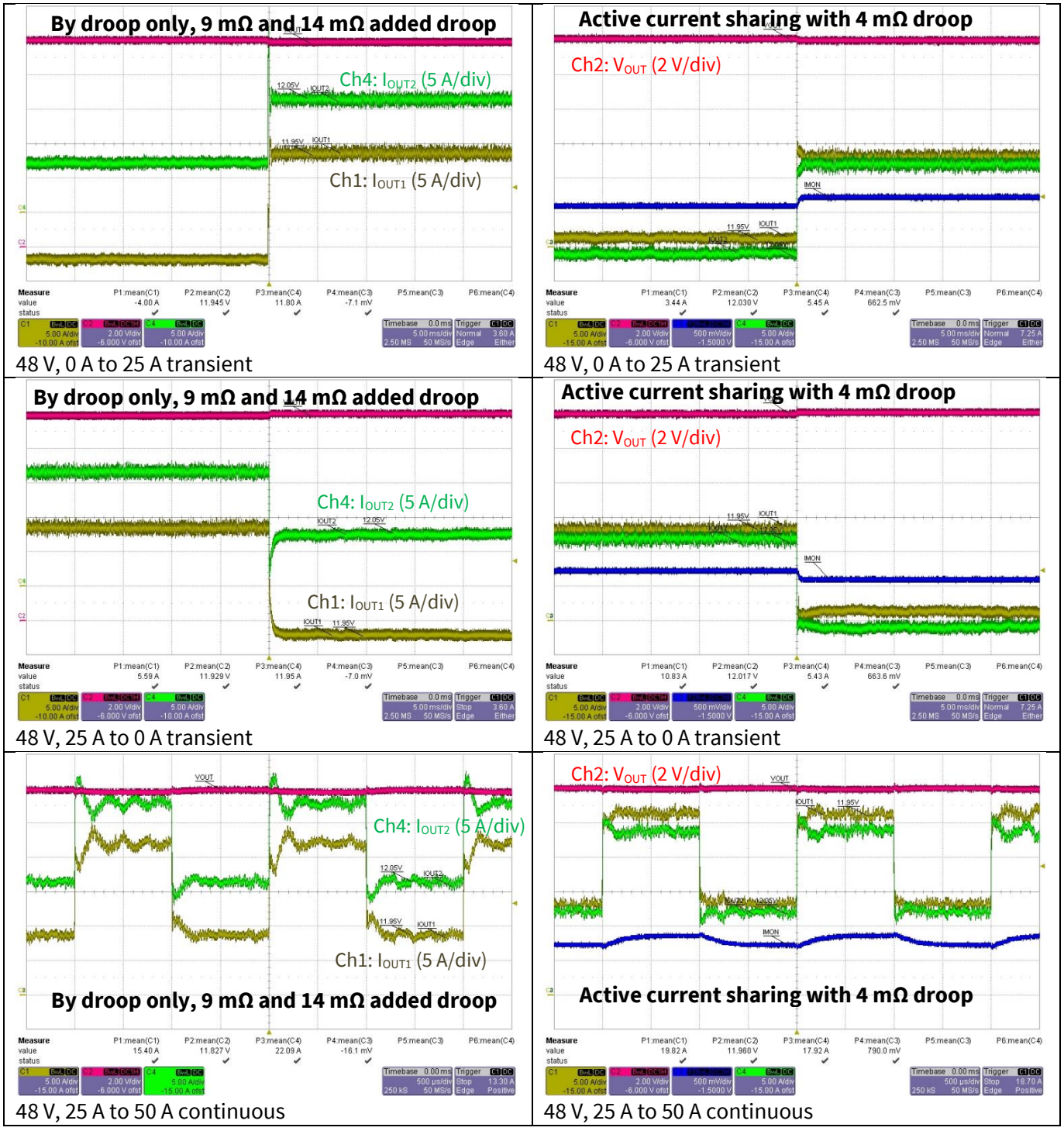


Figure 66 Current sharing at dynamic load

The load-transient test also shows that active current sharing does a better job than the passive droop method.

7.1.3 Start-up waveform with TON_DELAY and V_{OUT} mis-match

Unit 1, VOUT_COMMAND = 11.95 V, xaddr 0x41, TON_DELAY = 0, TON_RISE = 30 ms
Unit 2, VOUT_COMMAND = 12.05 V, xaddr 0x40, TON_DELAY = 10 ms, TON_RISE = 30 ms

In the test, unit 2 has 10 ms turn-on delay. Unit 2 is started with pre-bias condition. DE start-up is configured in unit 2. The output voltge shows smooth ramp up in both solutions. The active current sharing shows a better current sharing result.

Ch1: I_{OUT1} of unit 1 (5 A/div), Ch2: V_{OUT} (2 V/div), Ch3: IMON pin (0.5 V/div), Ch4: I_{OUT2} of unit 2 (5 A/div)

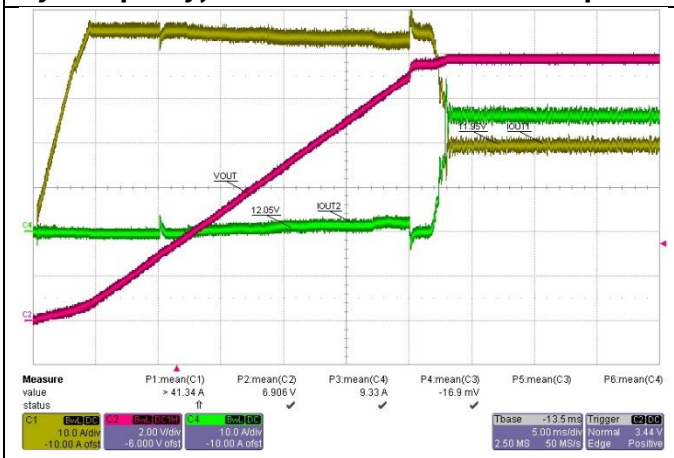
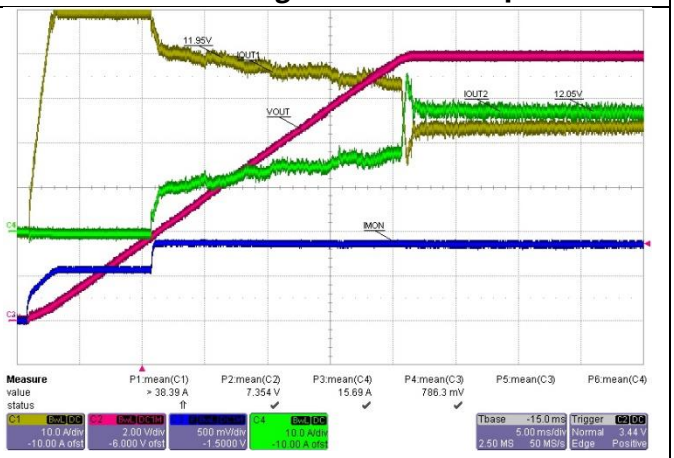
By droop only, 9 mΩ and 14 mΩ added droop	Active current sharing with 4 m Ω droop
	
48 V, 45 A start-up with 10 ms delay	48 V, 50 A start-up with 10 ms delay

Figure 67 Start-up waveforms with V_{OUT} mis-match and TON_DELAY

8 Mechanical outline

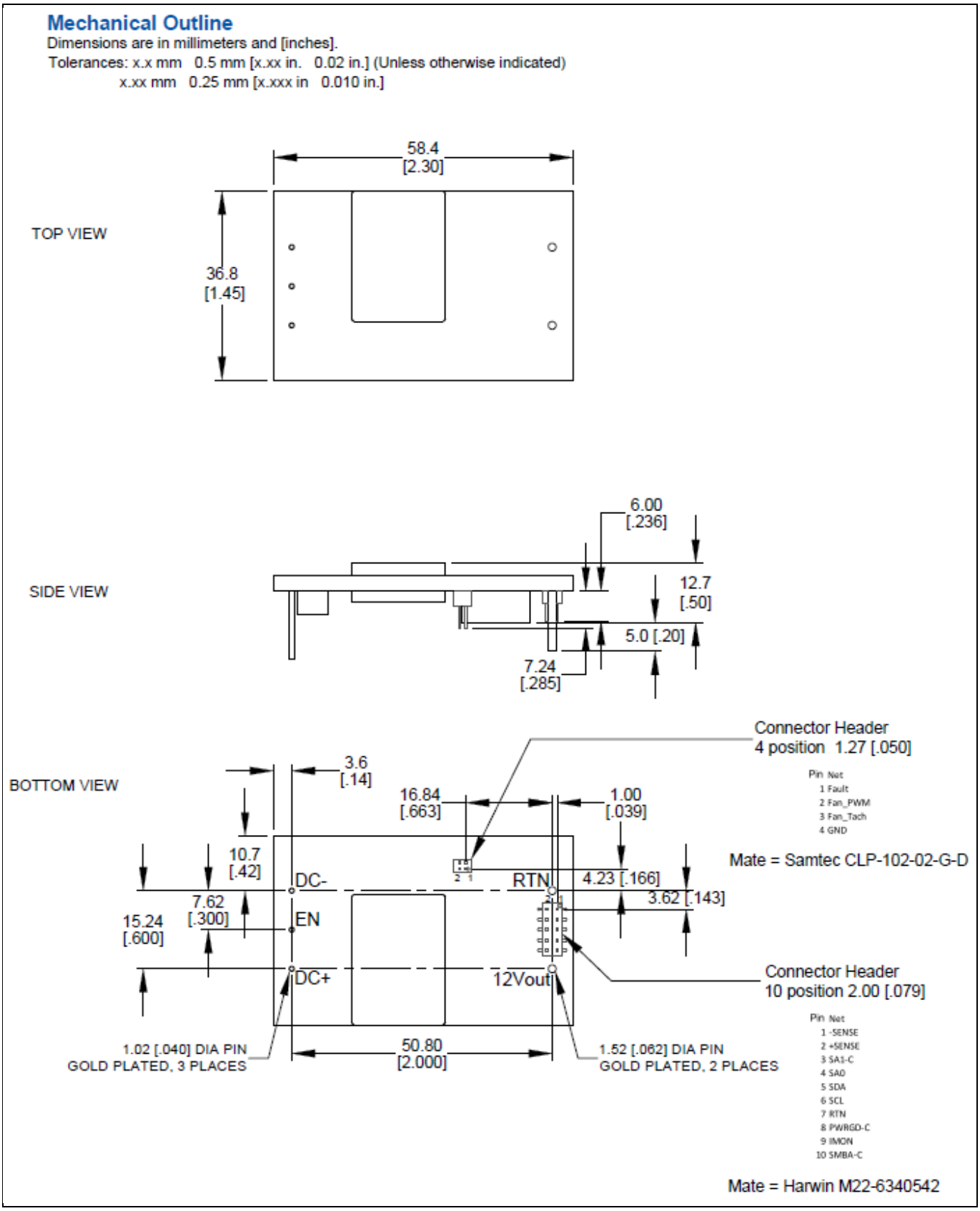


Figure 68 Board mechanical outline

9 Summary

This document introduces a complete Infineon system solution for a telecom 600 W FB-FB DB isolated DC-DC converter achieving 96 percent peak efficiency.

The XDPP1100 is a highly integrated and programmable digital power supply controller. It has a unique architecture that includes many optimized power-processing digital blocks to enhance the performance of Isolated DC-DC converters, reduce external components and minimize FW development effort. For advance power conversion and monitoring, the XDPP1100 device also provides accurate telemetry and power management bus (PMBus) interface for system communication. These advanced features make it an ideal power controller for modern high-end power systems employed in telecom infrastructure.

Specific power management peripherals have been added to enable high efficiency across the entire operating range, high integration for increased power density, reliability, and lowest overall system cost and high flexibility with support for the widest number of control schemes and topologies. Such peripherals include: light-load burst mode, synchronous rectification, input voltage feed-forward, copper trace current sense with temperature compensation, ideal diode emulation, flux balancing, secondary-side input voltage sensing, soft-start with pre bias, feedback loop open or short-circuit protection, and fast load-transient response.

The XDPP1100 device supports many commonly used DC-DC topologies, such as hard-switched full-bridge and half-bridge, phase-shifted full-bridge, active clamp forward, full-bridge and half-bridge current doubler rectifier, interleaved active clamp forward, interleaved half-bridge, and interleaved full-bridge. A dual-rail version also supports pre-buck or post-buck configuration.

Infineon's 100 V OptiMOS™ 5 BSC050N10NS5 SuperS08 and 40 V OptiMOS™ 6 BSC010N04LS6 SuperS08 power transistors, the latest and best-performing low parasitic devices from Infineon, combined with an optimized layout and an optimized driving circuitry, achieve incomparable performance with minimum stress on the devices. Both the primary and secondary OptiMOS™ FETs are driven from Infineon's 2EDF7275K EiceDRIVER™ gate drivers. The EiceDRIVER™ 2EDi is a family of fast dual-channel isolated MOSFET gate-driver ICs providing functional (2EDFx) or reinforced (2EDSx) input-to-output isolation by means of coreless transformer (CT) technology. Due to high driving current, excellent common-mode rejection and fast signal propagation, 2EDi is particularly well suited to driving medium- to high-voltage MOSFETs (CoolMOS™, OptiMOS™) in fast-switching power systems.

This DC-DC converter proves the feasibility of telecom isolated FB-FB as a high-efficiency topology for an isolated telecom 600 W quarter-brick converter, achieving the highest levels of efficiency when combined with the latest, best-in-class Infineon devices with their benchmark low $R_{DS(on)}$ and low parasitics.

References

[1] XDPP1100 datasheet

[2] XDPP1100 GUI installation and user guide

Revision history

Document version	Date of release	Description of changes
V1.0	2020-03-06	First release
V1.1	2020-10-28	Added Figure 8 test fixture connector and I2C connection drawing

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