XMC4300

Microcontroller Series for Industrial Applications

ARM® Cortex®-M4
32-bit processor core

About this Document

This datasheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4300 series devices.

The document describes the characteristics of a superset of the XMC4300 series devices. For simplicity, the various device types are referred to by the collective term XMC4300 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  - describes the functionality of the superset of devices.
- **Datasheets**
  - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  - list deviations from the specifications given in the related Reference Manual or Datasheets. Errata Sheets are provided for the superset of devices.

Attention**: **Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.
Please refer to http://www.infineon.com/xmc4000 to get access to the latest versions of those documents.

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1 Summary of Features

The XMC4300 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

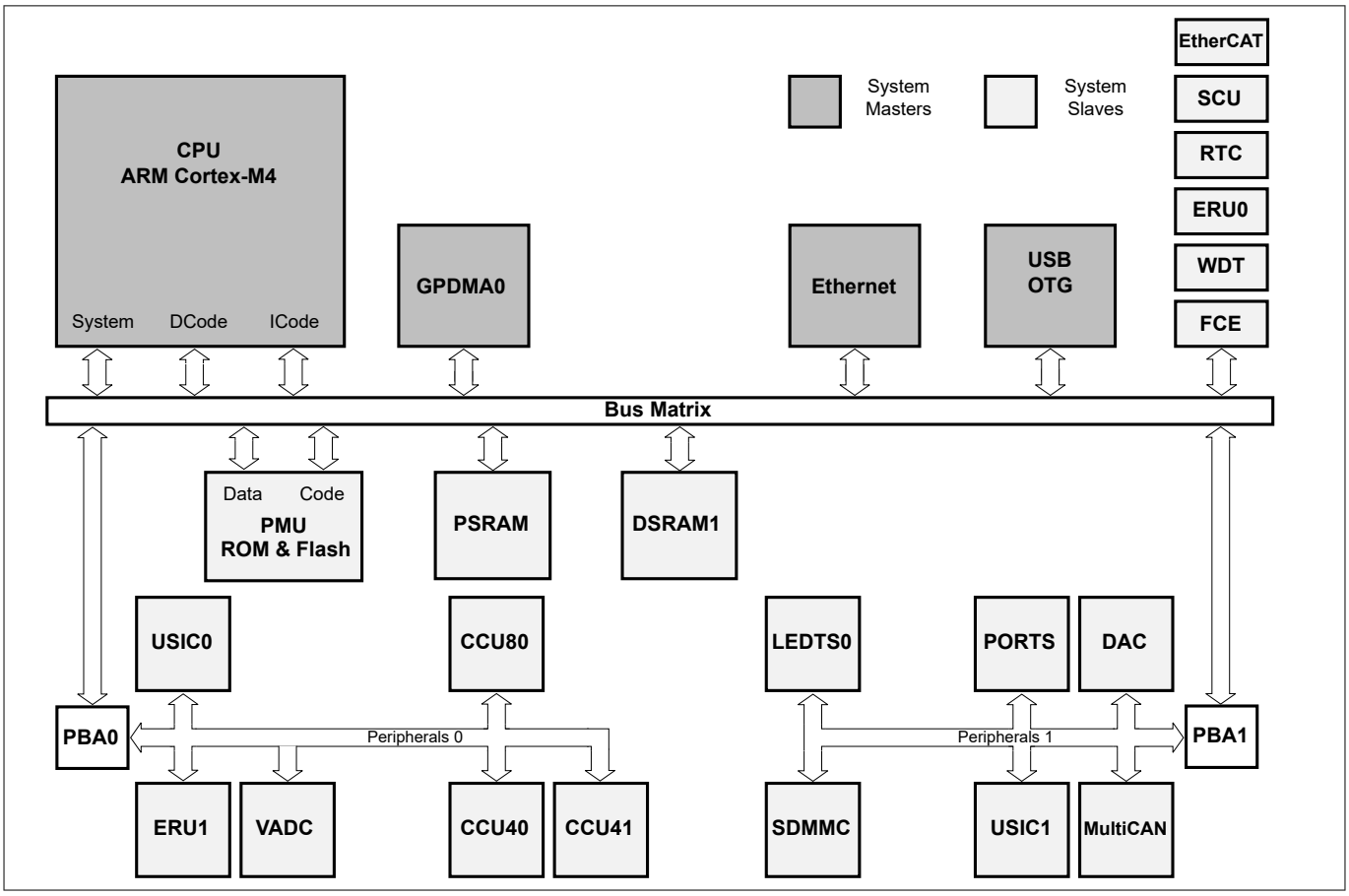

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- General Purpose DMA with up-to 8 channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

On-Chip Memories

- 16 KB on-chip boot ROM
- 64 KB on-chip high-speed program memory

1 Summary of Features

- 64 KB on-chip high speed data memory
- 256 KB on-chip Flash Memory with 8 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- EtherCATSlave interface (ECAT) capable of 100 Mbit/s transfer rates with 2 MII ports, 8 Fieldbus Memory Management Units (FMMU), 8 Sync Manager, 64 bit distributed clocks
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with 2 nodes, 64 message objects (MO), data rate up to 1 MBaud
- Four Universal Serial Interface Channels (USIC),providing 4 serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface
- SD and Multi-Media Card interface (SDMMC) for data storage memory cards

Analog Frontend Peripherals

- Two Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- One Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Two Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability
- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 6 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - E: LFBGA
  - F: LQFP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - K: -40°C to 125°C
- <FFFF> the Flash memory size

For ordering codes for the XMC4300 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4300 series, some descriptions may not apply to a specific product. Please see Device Types.

For simplicity the term **XMC4300** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC4300 Device Types

Derivative[1)]	Package	Flash Kbytes	SRAM Kbytes
XMC4300-F100x256	PG-LQFP-100	256	128

1) x is a placeholder for the supported temperature range.

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC4300 Device Types

Derivative[1)]	LEDTS Intf.	SD MMC Intf.	ETH Intf.	ECAT Slave Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4300-F100x256	1	1	RMII	2 x MII	1	2 x 2	N0, N1 MO[0..63]

1) x is a placeholder for the supported temperature range.

Table 3 Features of XMC4300 Device Types

Derivative[1)]	ADC Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice
XMC4300-F100x256	16	2	2 x 4	1 x 4

1) x is a placeholder for the supported temperature range.

1.4 Definition of Feature Variants

The XMC4300 types are offered with several memory sizes and number of available VADC channels. Table 4 describes the location of the available Flash memory, Table 5 describes the location of the available SRAMs, Table 6 the available VADC channels.

Table 4 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
256 Kbytes	0800 0000$_H$– 0803 FFFF$_H$	0C00 0000$_H$– 0C03 FFFF$_H$

Table 5 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM
128 Kbytes	1FFF 0000$_H$– 1FFF FFFF$_H$	2000 0000$_H$– 2000 FFFF$_H$

Table 6 ADC Channels[1)]

Package	VADC G0	VADC G1
PG-LQFP-100	CH0..CH7	CH0..CH7

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.5 Identification Registers

The identification registers allow software to identify the marking.

Table 7 XMC4300 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 3001$_H$	AA
JTAG IDCODE	101D F083$_H$	AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

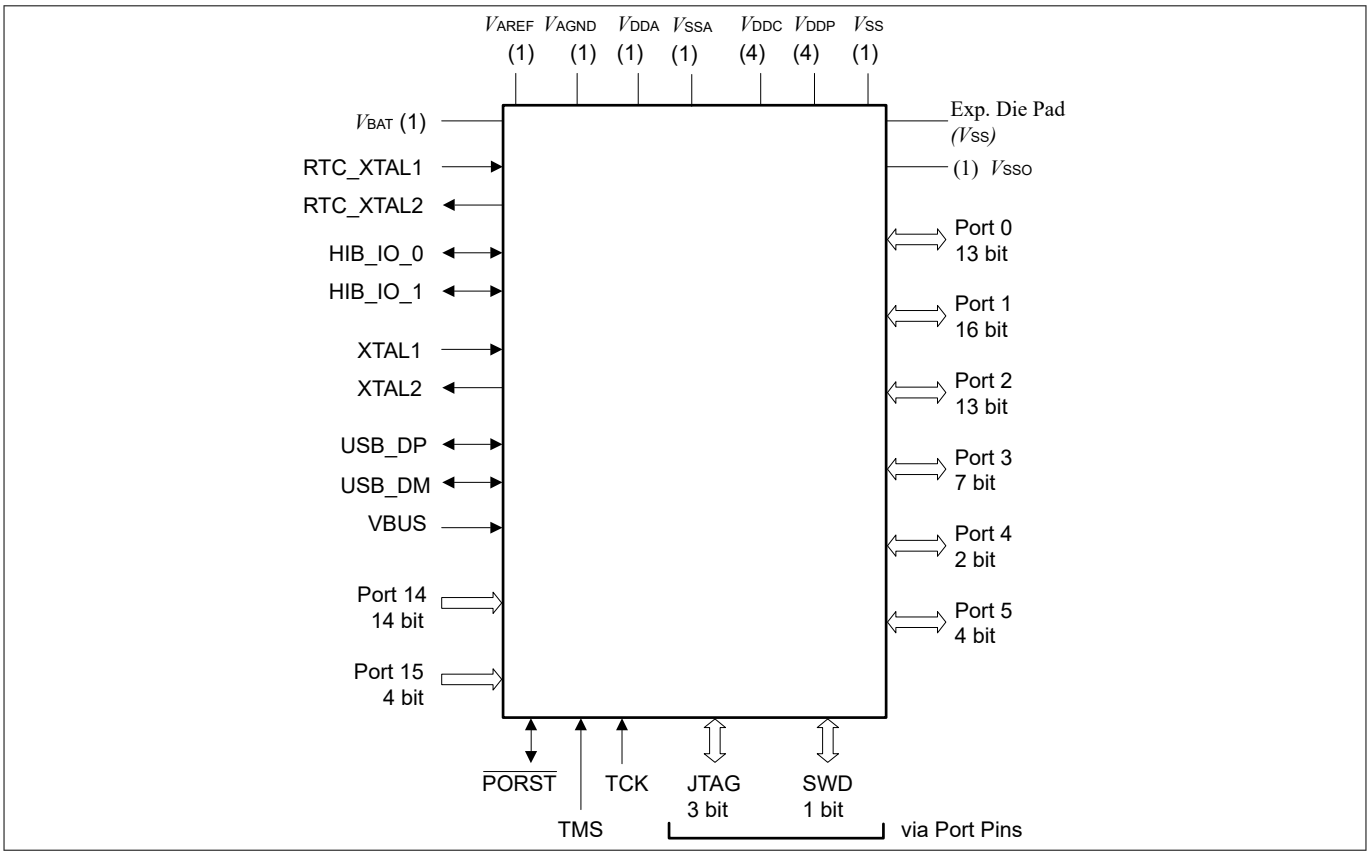

Figure 2 XMC4300 Logic Symbol PG-LQFP-100

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

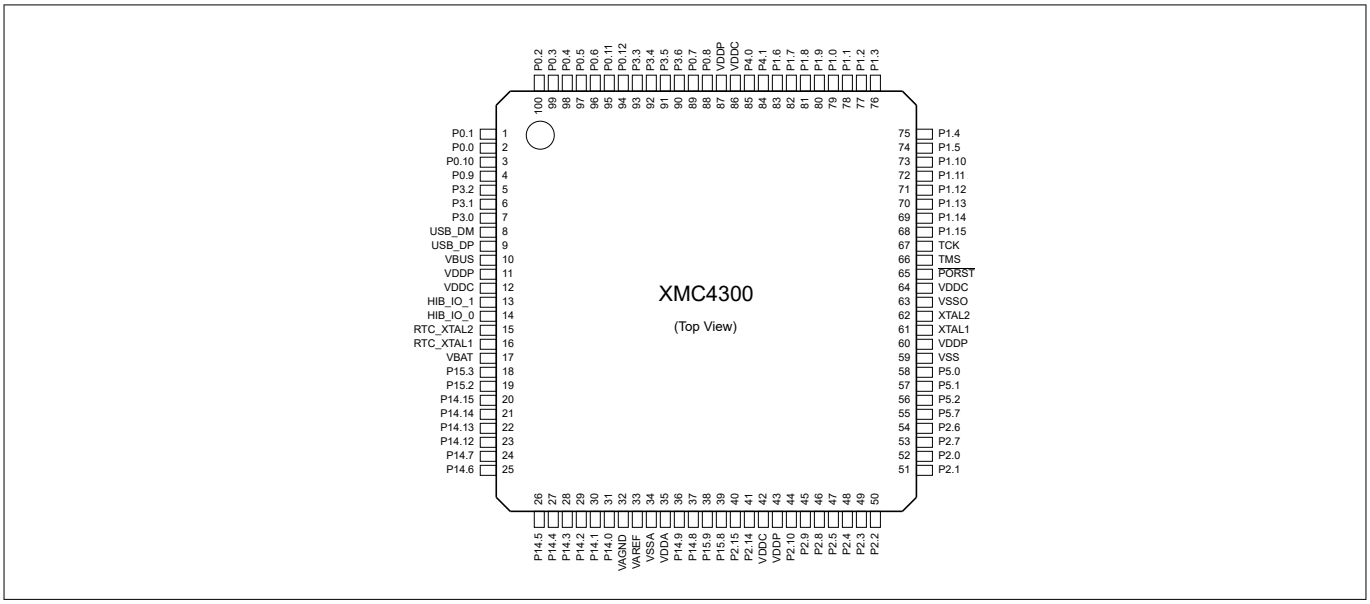

Figure 3 XMC4300 PG-LQFP-100 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 8 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. $\overline{\text{PORST}}$) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/ DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, that is deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 9 Package Pin Mapping

Function	LQFP-100	Pad Type	Notes
P0.0	2	A1+	
P0.1	1	A1+	
P0.2	100	A2	
P0.3	99	A2	

(table continues...)

Table 9 (continued) Package Pin Mapping

Function	LQFP-100	Pad Type	Notes
P0.4	98	A2	
P0.5	97	A2	
P0.6	96	A2	
P0.7	89	A2	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	88	A2	After a system reset, via HWSEL this pin selects the $\overline{\text{DB.TRST}}$ function, with a weak pull-down active.
P0.9	4	A2	
P0.10	3	A1+	
P0.11	95	A1+	
P0.12	94	A1+	
P1.0	79	A1+	
P1.1	78	A1+	
P1.2	77	A2	
P1.3	76	A2	
P1.4	75	A1+	
P1.5	74	A1+	
P1.6	83	A2	
P1.7	82	A2	
P1.8	81	A2	
P1.9	80	A2	
P1.10	73	A1+	
P1.11	72	A1+	
P1.12	71	A2	
P1.13	70	A2	
P1.14	69	A2	
P1.15	68	A2	
P2.0	52	A2	
P2.1	51	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	50	A2	
P2.3	49	A2	
P2.4	48	A2	
P2.5	47	A2	

(table continues...)

Table 9 (continued) Package Pin Mapping

Function	LQFP-100	Pad Type	Notes
P2.6	54	A1+	
P2.7	53	A1+	
P2.8	46	A2	
P2.9	45	A2	
P2.10	44	A2	
P2.14	41	A2	
P2.15	40	A2	
P3.0	7	A2	
P3.1	6	A2	
P3.2	5	A2	
P3.3	93	A1+	
P3.4	92	A1+	
P3.5	91	A2	
P3.6	90	A2	
P4.0	85	A2	
P4.1	84	A2	
P5.0	58	A1+	
P5.1	57	A1+	
P5.2	56	A1+	
P5.7	55	A1+	
P14.0	31	AN/DIG_IN	
P14.1	30	AN/DIG_IN	
P14.2	29	AN/DIG_IN	
P14.3	28	AN/DIG_IN	
P14.4	27	AN/DIG_IN	
P14.5	26	AN/DIG_IN	
P14.6	25	AN/DIG_IN	
P14.7	24	AN/DIG_IN	
P14.8	37	AN/DAC/DIG_IN	
P14.9	36	AN/DAC/DIG_IN	
P14.12	23	AN/DIG_IN	
P14.13	22	AN/DIG_IN	
P14.14	21	AN/DIG_IN	

(table continues...)

Table 9 (continued) Package Pin Mapping

Function	LQFP-100	Pad Type	Notes
P14.15	20	AN/DIG_IN	
P15.2	19	AN/DIG_IN	
P15.3	18	AN/DIG_IN	
P15.8	39	AN/DIG_IN	
P15.9	38	AN/DIG_IN	
HIB_IO_0	14	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
HIB_IO_1	13	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active. As output the medium driver mode is active.
USB_DP	9	special	
USB_DM	8	special	
TCK	67	A1	Weak pull-down active.
TMS	66	A1+	Weak pull-up active. As output the strong-soft driver mode is active.
$\overline{\text{PORST}}$	65	special	Weak pull-up permanently active, strong pull-down controlled by EVR.
XTAL1	61	clock_IN	
XTAL2	62	clock_O	
RTC_XTAL1	16	clock_IN	
RTC_XTAL2	15	clock_O	
VBAT	17	Power	When VDDP is supplied VBAT has to be supplied as well.
VBUS	10	special	
VAREF	33	AN_Ref	
VAGND	32	AN_Ref	
VDDA	35	AN_Power	
VSSA	34	AN_Power	
VDDC	12	Power	
VDDC	42	Power	
VDDC	64	Power	
VDDC	86	Power	
VDDP	11	Power	

(table continues...)

Table 9 (continued) Package Pin Mapping

Function	LQFP-100	Pad Type	Notes
VDDP	43	Power	
VDDP	60	Power	
VDDP	87	Power	
VSS	59	Power	
VSSO	63	Power	
VSS	Exp. Pad	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board. For thermal aspects, please refer to the Datasheet. Board layout examples are given in an application note.

2.2.2 Port I/O Functions

The following general scheme is used to describe each Port pin:

Table 10 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

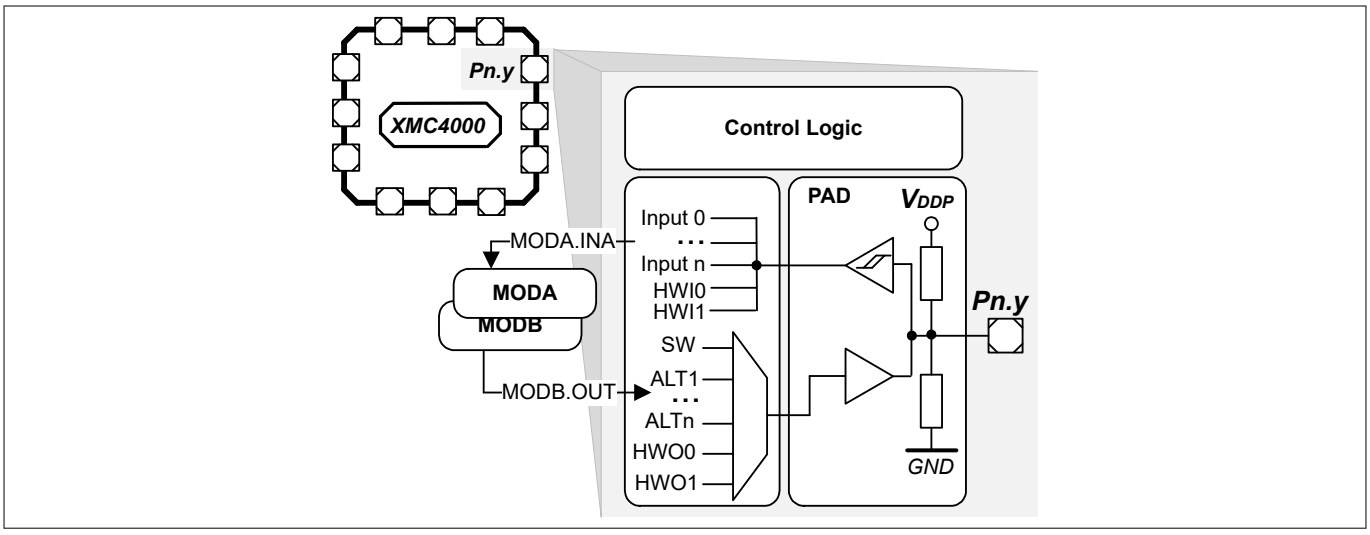

Figure 4 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

2.2.2.1 Port I/O Function Table

Table 11 Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ECAT0. PHY_RST	CAN. N0_TXD	CCU80. OUT21	LEDTS0. COL2			U1C1. DX0D	ETH0. CLK_RMIIB	ERU0. 0B0					ETH0. CLKRXB
P0.1	USB. DRIVEVBUS	U1C1. DOUT0	CCU80. OUT11	LEDTS0. COL3				ETH0. CRS_DVB	ERU0. 0A0				ECAT0. P1_RX_CLA	ETH0. RXDVB
P0.2	ECAT0. P1_TXD2	U1C1. SELO1	CCU80. OUT01		U1C0. DOUT3	U1C0. HWIN3	ETH0. RXD0B		ERU0. 3B3					
P0.3	ECAT0. P1_TXD3		CCU80. OUT20		U1C0. DOUT2	U1C0. HWIN2	ETH0. RXD1B			ERU1. 3B0				
P0.4	ETH0. TX_EN		CCU80. OUT10		U1C0. DOUT1	U1C0. HWIN1		U1C0. DX0A	ERU0. 2B3				ECAT0. P1_RXD3A	
P0.5	ETH0. TXD0	U1C0. DOUT0	CCU80. OUT00		U1C0. DOUT0	U1C0. HWIN0		U1C0. DX0B		ERU1. 3A0			ECAT0. P1_RXD2A	
P0.6	ETH0. TXD1	U1C0. SELO0	CCU80. OUT30					U1C0. DX2A	ERU0. 3B2		CCU80. IN2B		ECAT0. P1_RXD1A	

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
P0.7	WDT. SERVICE_OUT	U0C0. SELO0	ECAT0. LED_ERR			DB. TDI	U0C0. DX2B		ERU0. 2B1		CCU80. IN0A	CCU80. IN1A	CCU80. IN2A	CCU80. IN3A
P0.8	SCU. EXTCLK	U0C0. SCLKOUT	ECAT0. LED_RUN			$\overline{\text{DB.}}$ $\overline{\text{TRST}}$	U0C0. DX1B		ERU0. 2A1		CCU80. IN1B			
P0.9		U1C1. SELO0	CCU80. OUT12	LEDTS0. COL0	ETH0. MDO	ETH0. MDIA	U1C1. DX2A	USB. ID	ERU0. 1B0				ECAT0. P1_RX_DVA	
P0.10	ETH0. MDC	U1C1. SCLKOUT	CCU80. OUT02	LEDTS0. COL1			U1C1. DX1A		ERU0. 1A0				ECAT0. P1_TX_CLA	
P0.11	ECAT0. P1_LINK_ACT	U1C0. SCLKOUT	CCU80. OUT31		$\overline{\text{SDMMC.}}$ $\overline{\text{RST}}$		ETH0. RXERB	U1C0. DX1A	ERU0. 3A2				ECAT0. P1_RXD0A	
P0.12		U1C1. SELO0	CCU40. OUT3		ECAT0. MDO	ECAT0. MDIA		U1C1. DX2B	ERU0. 2B2					
P1.0		U0C0. SELO0	CCU40. OUT3	ERU1. PDOUT3			U0C0. DX2A		ERU0. 3B0		CCU40. IN3A			ECAT0. P0_TX_CLA
P1.1		U0C0. SCLKOUT	CCU40. OUT2	ERU1. PDOUT2		SDMMC. SDWC	U0C0. DX1A		ERU0. 3A0		CCU40. IN2A			ECAT0. P0_RX_CLA

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO 0**	**HWI 0**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P1.2	ECAT0. P0_TXD 3		CCU40. OUT1	ERU1. PDOUT 1	U0C0. DOUT 3	U0C 0. HWI N3				ERU1. 2B0	CCU40. IN1A			
P1.3	ECAT0. P0_TX_ ENA	U0C0. MCLKO UT	CCU40. OUT0	ERU1. PDOUT 0	U0C0. DOUT 2	U0C 0. HWI N2				ERU1. 2A0	CCU40. IN0A			
P1.4	WDT. SERVIC E_OUT	CAN. N0_TXD	CCU80. OUT33		U0C0. DOUT 1	U0C 0. HWI N1	U0C0. DX0B	CAN. N1_RXD D	ERU0. 2B0		CCU41. IN0C			ECAT0. P0_RXD 0A
P1.5	CAN. N1_TXD	U0C0. DOUT0	CCU80. OUT23		U0C0. DOUT 0	U0C 0. HWI N0	U0C0. DX0A	CAN. N0_RXD A	ERU0. 2A0	ERU1. 0A0	CCU41. IN1C			ECAT0. P0_RXD 1A
P1.6	ECAT0. P0_TXD 0	U0C0. SCLKO UT			SDM MC. DATA 1_OU T	SDM MC. DATA 1_IN								
P1.7	ECAT0. P0_TXD 1	U0C0. DOUT0		U1C1. SELO2	SDM MC. DATA 2_OU T	SDM MC. DATA 2_IN								

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
P1.8	ECAT0. P0_TXD 2	U0C0. SELO1		U1C1. SCLKO UT	SDM MC. DATA 4_OU T	SDM MC. DATA 4_IN								
P1.9	U0C0. SCLKO UT			U1C1. DOUT0	SDM MC. DATA 5_OU T	SDM MC. DATA 5_IN								ECAT0. P0_RX_ DVA
P1.10	ETH0. MDC	U0C0. SCLKO UT		ECAT0. LED_ER R		$\overline{\text{SDMMC. SDCD}}$					CCU41. IN2C			ECAT0. P0_RXD 2A
P1.11	ECAT0. LED_ST ATE_R UN	U0C0. SELO0		ECAT0. LED_RU N	ETH0. MDO	ETH 0. MDIC					CCU41. IN3C			ECAT0. P0_RXD 3A
P1.12	ETH0. TX_EN	CAN. N1_TXD		ECAT0. P0_LIN K_ACT	SDM MC. DATA 6_OU T	SDM MC. DATA 6_IN								
P1.13	ETH0. TXD0	U0C1. SELO3		ECAT0. PHY_CL K25	SDM MC. DATA 7_OU T	SDM MC. DATA 7_IN	CAN. N1_RXD C							

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
P1.14	ETH0. TXD1	U0C1. SELO2		ECAT0. SYNC0			U1C0. DX0E							
P1.15	SCU. EXTCLK			U1C0. DOUT0						ERU1. 1A0				ECAT0. P0_LINKB
P2.0	CAN. N0_TXD			LEDTS0. COL1	ETH0. MDO	ETH0. MDIB			ERU0. 0B3		CCU40. IN1C			
P2.1				LEDTS0. COL0	DB.TDO/ TRACESWO		ETH0. CLK_RMIIA			ERU1. 0B0	CCU40. IN0C			ETH0. CLKRXA
P2.2	VADC. EMUX00		CCU41. OUT3	LEDTS0. LINE0	LEDTS0. EXTENDED0	LEDTS0. TSIN0A	ETH0. RXD0A	U0C1. DX0A	ERU0. 1B2		CCU41. IN3A			
P2.3	VADC. EMUX01	U0C1. SELO0	CCU41. OUT2	LEDTS0. LINE1	LEDTS0. EXTENDED1	LEDTS0. TSIN1A	ETH0. RXD1A	U0C1. DX2A	ERU0. 1A2		CCU41. IN2A			

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
P2.4	VADC. EMUX02	U0C1. SCLKOUT	CCU41. OUT1	LEDTS0. LINE2	LEDTS0. EXTENDED2	LEDTS0. TSIN2A	ETH0. RXERA	U0C1. DX1A	ERU0. 0B2		CCU41. IN1A			
P2.5	ETH0. TX_EN	U0C1. DOUT0	CCU41. OUT0	LEDTS0. LINE3	LEDTS0. EXTENDED3	LEDTS0. TSIN3A	ETH0. RXDVA	U0C1. DX0B	ERU0. 0A2		CCU41. IN0A			ETH0. CRS_DVA
P2.6		ERU1. PDOUT3	CCU80. OUT13	LEDTS0. COL3				CAN. N1_RXDA	ERU0. 1B3		CCU40. IN3C	ECAT0. P0_RX_ERRB		
P2.7	ETH0. MDC	CAN. N1_TXD	CCU80. OUT03	LEDTS0. COL2						ERU1. 1B0	CCU40. IN2C			
P2.8	ETH0. TXD0	ERU1. PDOUT1	CCU80. OUT32	LEDTS0. LINE4	LEDTS0. EXTENDED4	LEDTS0. TSIN4A	DAC. TRIGGER5				CCU40. IN0B	CCU40. IN1B	CCU40. IN2B	CCU40. IN3B
P2.9	ETH0. TXD1	ERU1. PDOUT2	CCU80. OUT22	LEDTS0. LINE5	LEDTS0. EXTENDED5	LEDTS0. TSIN5A	DAC. TRIGGER4				CCU41. IN0B	CCU41. IN1B	CCU41. IN2B	CCU41. IN3B

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
P2.10	VADC. EMUX1 0	ERU1. PDOUT 0	ECAT0. PHY_RS T	ECAT0. SYNC1										
P2.14	VADC. EMUX1 1	U1C0. DOUT0	CCU80. OUT21					U1C0. DX0D						
P2.15	VADC. EMUX1 2	ECAT0. P1_TXD 3	CCU80. OUT11	LEDTS0 . LINE6	LEDT S0. EXTE NDED 6	LEDT S0. TSIN 6A	ETH0. COLA	U1C0. DX0C						
P3.0		U0C1. SCLKO UT		ECAT0. P1_TX_ ENA			U0C1. DX1B				CCU80. IN2C			
P3.1		U0C1. SELO0	ECAT0. P1_TXD 0				U0C1. DX2B		ERU0. 0B1		CCU80. IN1C			
P3.2	USB. DRIVEV BUS	CAN. N0_TXD	ECAT0. P1_TXD 1	LEDTS0 . COLA					ERU0. 0A1		CCU80. IN0C			
P3.3		U1C1. SELO1		ECAT0. MCLK	SDM MC. LED							CCU80. IN3B		

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
P3.4		U1C1. SELO2			SDMMC. BUS_POWER							CCU80. IN0B	ECAT0. P1_LINA	
P3.5		U1C1. SELO3		U0C1. DOUT0	SDMMC. CMD_OUT	SDMMC. CMD_IN			ERU0. 3B1				ECAT0. P1_RX_ERRA	
P3.6		U1C1. SELO4		U0C1. SCLKOUT	SDMMC. CLK_OUT	SDMMC. CLK_IN			ERU0. 3A1					
P4.0		ECAT0. PHY_CLK25		U1C0. SCLKOUT	SDMMC. DATA0_OUT	SDMMC. DATA0_IN	U1C1. DX1C		U0C1. DX0E					ECAT0. P0_RX_ERRA
P4.1		U1C1. MCLKOUT		U0C1. SELO0	SDMMC. DATA3_OUT	SDMMC. DATA3_IN								ECAT0. P0_LINA
P5.0				ERU1. PDOUT0				ETH0. RXD0D	U0C0. DX0D	ECAT0. P0_RXD0B				

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
P5.1	U0C0. DOUT0			ERU1. PDOUT 1				ETH0. RXD1D		ECAT0. P0_RXD 1B				
P5.2		ECAT0. P0_LIN K_ACT		ERU1. PDOUT 2				ETH0. CRS_DV D		ECAT0. P0_RXD 2B				ETH0. RXDVD
P5.7	ECAT0. SYNC0			LEDTS0 . COLA						ECAT0. P0_RXD 3B				
P14.0							VADC. G0CH0							
P14.1							VADC. G0CH1							
P14.2							VADC. G0CH2	VADC. G1CH2						
P14.3							VADC. G0CH3	VADC. G1CH3			CAN. N0_RXD B			
P14.4							VADC. G0CH4							ECAT0. LATCH1 A
P14.5							VADC. G0CH5							ECAT0. LATCH0 A

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
P14.6							VADC. G0CH6						G0ORC 6	ECAT0. P1_RX_ CLKB
P14.7							VADC. G0CH7						G0ORC 7	ECAT0. P1_RXD 0B
P14.8					DAC. OUT_ 0			VADC. G1CH0			ETH0. RXD0C			
P14.9					DAC. OUT_ 1			VADC. G1CH1			ETH0. RXD1C			
P14.12								VADC. G1CH4						ECAT0. P1_RXD 1B
P14.13								VADC. G1CH5						ECAT0. P1_RXD 2B
P14.14								VADC. G1CH6					G1ORC 6	ECAT0. P1_RXD 3B
P14.15								VADC. G1CH7					G1ORC 7	ECAT0. P1_RX_ DVB

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
P15.2														ECAT0. P1_RX_ ERRB
P15.3														ECAT0. P1_LIN KB
P15.8											ETH0. CLK_R MIIC			ETH0. CLKRXC
P15.9											ETH0. CRS_DV C			ETH0. RXDVC
HIB_IO_0	HIBOUT	WDT. SERVIC E_OUT					AKEUP A							
HIB_IO_1	HIBOUT	WDT. SERVIC E_OUT					AKEUP B							
USB_DP														
USB_DM														
TCK						DB.T C/ SCLK								

(table continues...)

Table 11 (continued) Port I/O Functions

Function	Output					Input								
	ALT1	ALT2	ALT3	ALT4	HWO 0	HWI 0	Input	Input	Input	Input	Input	Input	Input	Input
TMS					DB.TMS/ SWDIO									
$\overline{\text{PORST}}$														
XTAL1							U0C0.DX0F	U0C1.DX0F	U1C0.DX0F	U1C1.DX0F				
XTAL2														
RTC_XTAL1									ERU0.1B1					
RTC_XTAL2														

2.3 Power Connection Scheme

Figure 5 shows a reference power connection scheme for the XMC4300.

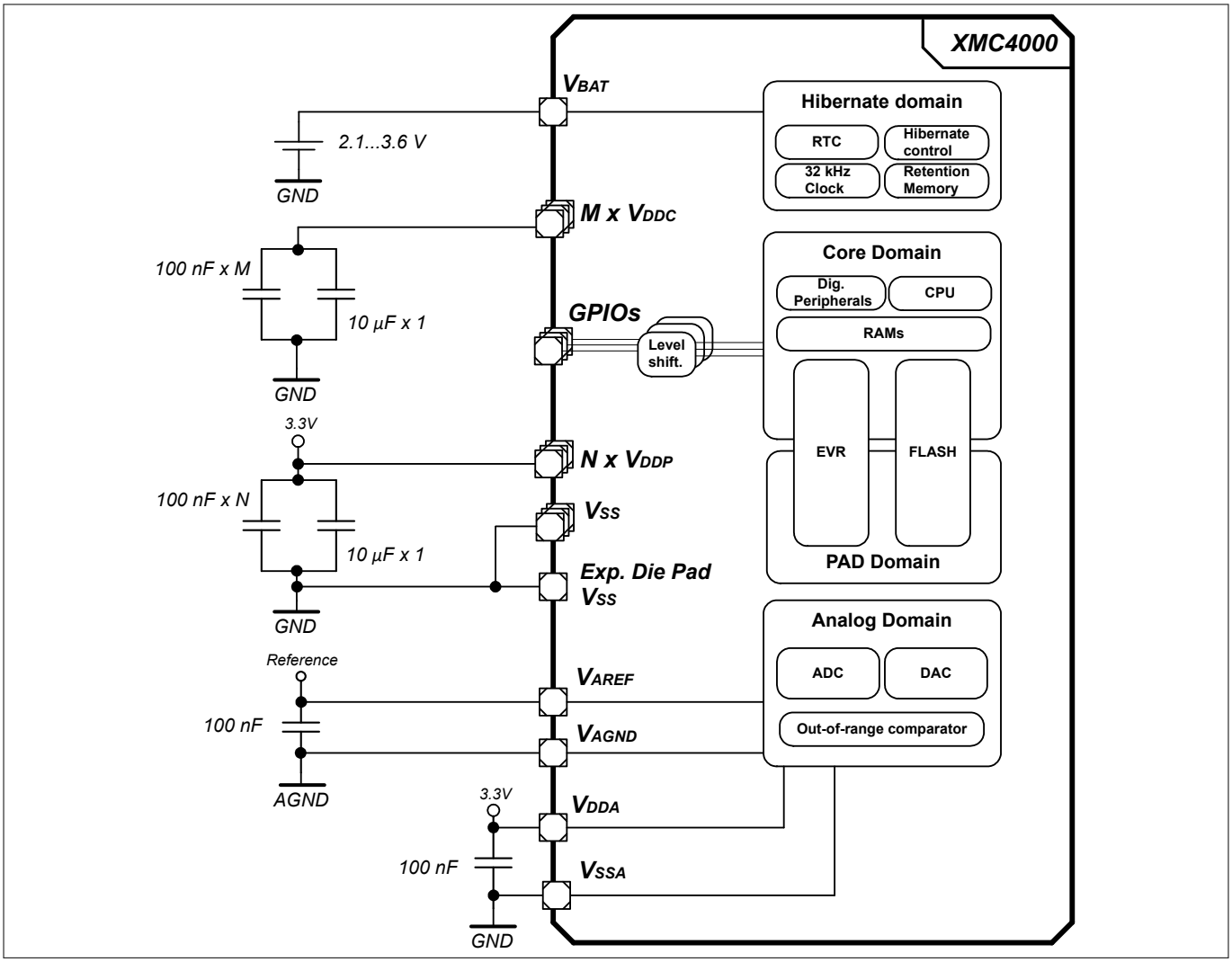

Figure 5 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS}. An additional 10 µF capacitor is connected to the V_{DDP} nets and an additional 10 uF capacitor to the V_{DDP} nets.

The XMC4300 has a common ground concept, all V_{SS}, V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

V_{AGND} is the low potential to the analog reference V_{AREF}. Depending on the application it can share the common ground or have a different potential. In devices with shared V_{DDA}/V_{AREF} and V_{SSA}/V_{AGND} pins the reference is tied to the supply. Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT}, the V_{BAT} pin can also be connected directly to V_{DDP}.

3 Electrical Parameters

Attention: ***All parameters in this chapter are preliminary target values and may change based on characterization results.***

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4300 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with a two-letter abbreviation in column “Symbol”:

- **CC**

  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4300 and must be regarded for system design
- **SR**

  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4300 is designed in

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 12 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Storage temperature	T_{ST} SR	-65	–	150	°C	–
Junction temperature	T_J SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP} SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN} SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF} SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN} SR	-10	–	+10	mA	

(table continues...)

Table 12 (continued) Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Absolute maximum sum of all input circuit currents for one port group during overload condition[1)]	ΣI_{IN} SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN} SR	-100	–	+100	mA	

1) The port groups are defined in Pin Reliability in Overload.

Figure 6 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}. The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in Pin Reliability in Overload.

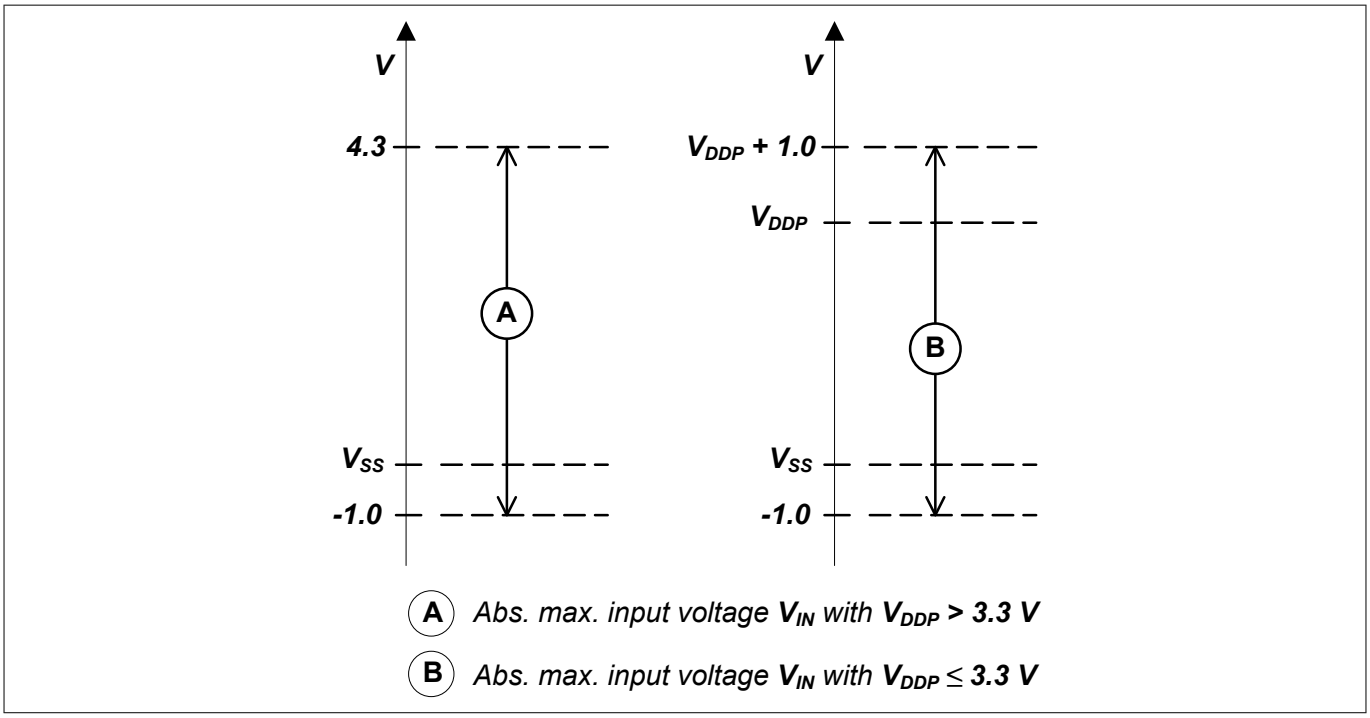

Figure 6 Absolute Maximum Input Voltage Ranges

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 13 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- Operating Conditions are met for
  - pad supply levels (V_{DDP} or V_{DDA})
  - temperature

If a pin current is outside of the Operating Conditions but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

***Note**: An overload condition on one or more pins does not require a reset.*

***Note**: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.*

Table 13 Overload Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1)]	I_{OVG} SR	–	–	20	mA	$\Sigma\lvert I_{OVx}\rvert$, for all $I_{OVx} < 0$ mA
		–	–	20	mA	$\Sigma\lvert I_{OVx}\rvert$, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	80	mA	ΣI_{OVG}

1) The port groups are defined in Table 16.

Figure 7 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

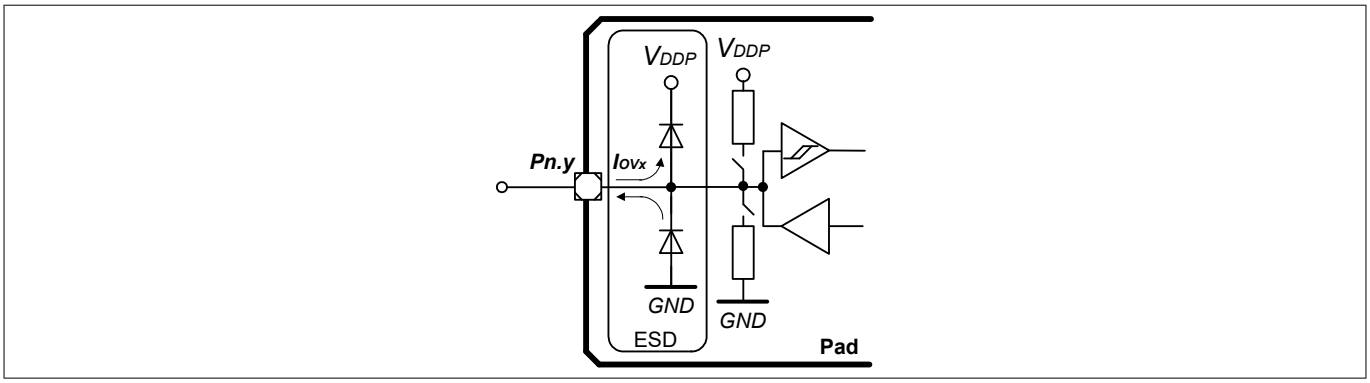

Figure 7 Input Overload Current via ESD structures

Table 14 and Table 15 list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the Absolute Maximum Ratings must not be exceeded during overload.

Table 14 PN-Junction Characteristics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40°C	I_{OV} = 5 mA, T_J = 150°C
A1/A1+	$V_{IN} = V_{DDP} + 1.0$ V	$V_{IN} = V_{DDP} + 0.75$ V
A2	$V_{IN} = V_{DDP} + 0.7$ V	$V_{IN} = V_{DDP} + 0.6$ V
AN/DIG_IN	$V_{IN} = V_{DDP} + 1.0$ V	$V_{IN} = V_{DDP} + 0.75$ V

Table 15 PN-Junction Characteristics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40°C	I_{OV} = 5 mA, T_J = 150°C
A1/A1+	$V_{IN} = V_{SS} - 1.0$ V	$V_{IN} = V_{SS} - 0.75$ V
A2	$V_{IN} = V_{SS} - 0.7$ V	$V_{IN} = V_{SS} - 0.6$ V
AN/DIG_IN	$V_{IN} = V_{DDP} - 1.0$ V	$V_{IN} = V_{DDP} - 0.75$ V

Table 16 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[12:0], P3.[6:0]
2	P14.[15:0], P15.[9:2]
3	P2.[15:0], P5.[7:0]
4	P1.[15:0], P4.[1:0]

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and their basic characteristics.

Table 17 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O,	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended
			A2 (e.g. ext. Bus)	80 MHz	15 pF	Series termination recommended

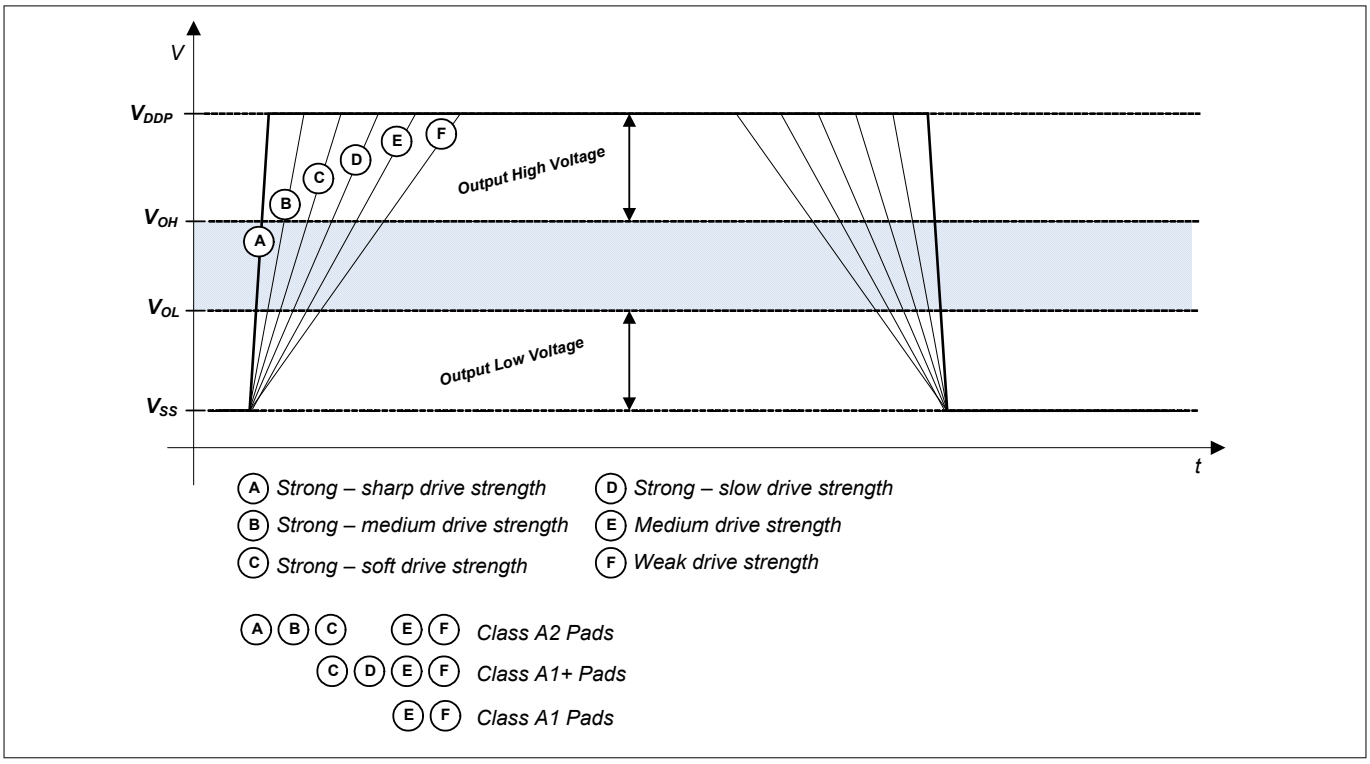

Figure 8 Output Slopes with different Pad Driver Modes

Figure 8 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in Input/Output Pins.

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4300. All parameters specified in the following sections refer to these operating conditions, unless noted otherwise.

Table 18 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	125	°C	Temp. Range K
Digital supply voltage	V_{DDP} SR	3.13[1]	3.3	3.63[2]	V	
Core Supply Voltage	V_{DDC} CC	-[1]	1.3	–	V	Generated internally
Digital ground voltage	V_{SS} SR	0	–	–	V	
ADC analog supply voltage	V_{DDA} SR	3.0	3.3	3.6[2]	V	
Analog ground voltage for V_{DDA}	V_{SSA} SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain	V_{BAT} SR	1.95[3]	–	3.63	V	When V_{DDP} is supplied V_{BAT} has to be supplied as well.
System Frequency	f_{SYS} SR	–	–	144	MHz	
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group[4]	ΣI_{SC_PG} SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	100	mA	

1) See also the Supply Monitoring thresholds, Power-Up and Supply Monitoring.
2) Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h over lifetime.
3) To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.
4) The port groups are defined in Table 16.

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.

The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 19 Standard Pad Parameters

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/ outputs)	C_{IO} CC	–	10	pF	
Pull-down current	$\lvert I_{PDL}\rvert$ SR	150	–	µA	[1] $V_{IN} \geq 0.6 \times V_{DDP}$
		–	10	µA	[2] $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-up current	$\lvert I_{PUH}\rvert$ SR	–	10	µA	[2] $V_{IN} \geq 0.6 \times V_{DDP}$
		100	–	µA	[1] $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[3]	*HYSA* CC	$0.1 \times V_{DDP}$	–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–	10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100	–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{PPD}\rvert$ CC	13	–	mA	V_{IN} = 1.0 V

1) Current required to override the pull device with the opposite logic level (“force current”). With active pull device, at load currents between force and keep current the input state is undefined.
2) Load current at which the pull device still maintains the valid logic level (“keep current”). With active pull device, at load currents between force and keep current the input state is undefined.
3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

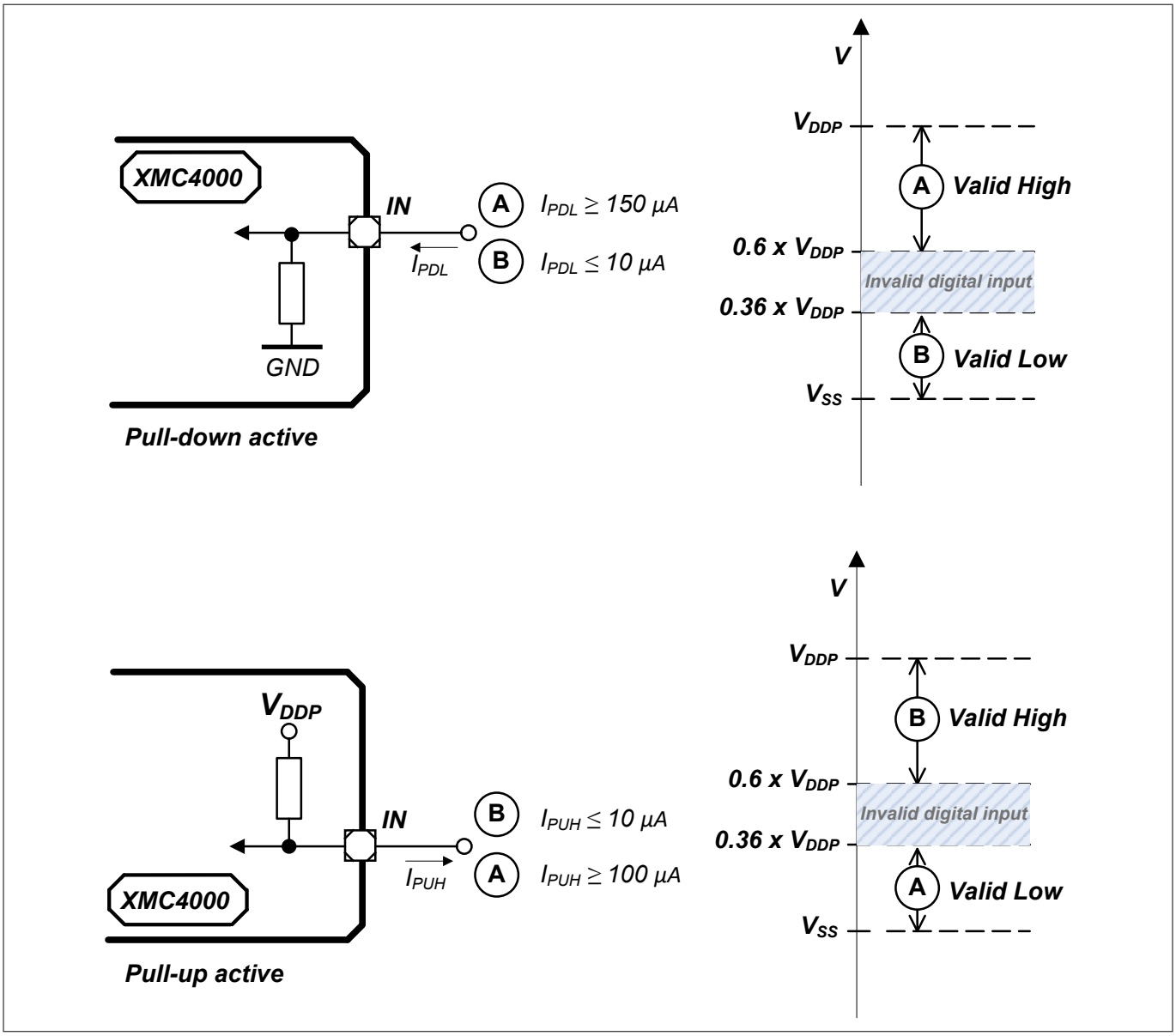

Figure 9 Pull Device Input Characteristics

Figure 9 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load

Table 20 Standard Pads Class_A1

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Input leakage current	I_{OZA1} CC	-500	500	nA	$0\ V \leq V_{IN} \leq V_{DDP}$
Input high voltage	V_{IHA1} SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA1} SR	-0.3	$0.36 \times V_{DDP}$	V	

(table continues...)

Table 20 (continued) Standard Pads Class_A1

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Output high voltage, POD[1] = weak	V_{OHA1} CC	V_{DDP} - 0.4	–	V	$I_{OH} \geq$ -400 µA
		2.4	–	V	$I_{OH} \geq$ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4	–	V	$I_{OH} \geq$ -1.4 mA
		2.4	–	V	$I_{OH} \geq$ -2 mA
Output low voltage	V_{OLA1} CC	–	0.4	V	$I_{OL} \leq$ 500 µA; POD[1] = weak
		–	0.4	V	$I_{OL} \leq$ 2 mA; POD[1] = medium
Fall time	t_{FA1} CC	–	150	ns	C_L = 20 pF; POD[1] = weak
		–	50	ns	C_L = 50 pF; POD[1] = medium
Rise time	t_{RA1} CC	–	150	ns	C_L = 20 pF; POD[1] = weak
		–	50	ns	C_L = 50 pF; POD[1] = medium

1) POD = Pin Out Driver

Table 21 Standard Pads Class_A1+

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Input leakage current	I_{OZA1+} CC	-1	1	µA	0 V ≤ V_{IN} ≤ V_{DDP}
Input high voltage	V_{IHA1+} SR	0.6 × V_{DDP}	V_{DDP} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILA1+} SR	-0.3	0.36 × V_{DDP}	V	
Output high voltage, POD[1] = weak	V_{OHA1+} CC	V_{DDP} - 0.4	–	V	$I_{OH} \geq$ -400 µA
		2.4	–	V	$I_{OH} \geq$ -500 µA
Output high voltage, POD[1] = medium		V_{DDP} - 0.4	–	V	$I_{OH} \geq$ -1.4 mA
		2.4	–	V	$I_{OH} \geq$ -2 mA
Output high voltage, POD[1] = strong		V_{DDP} - 0.4	–	V	$I_{OH} \geq$ -1.4 mA
		2.4	–	V	$I_{OH} \geq$ -2 mA

(table continues...)

Table 21 (continued) Standard Pads Class_A1+

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Output low voltage	V_{OLA1+} CC	–	0.4	V	$I_{OL} \leq 500$ µA; POD[1] = weak
		–	0.4	V	$I_{OL} \leq 2$ mA; POD[1] = medium
		–	0.4	V	$I_{OL} \leq 2$ mA; POD[1] = strong
Fall time	t_{FA1+} CC	–	150	ns	C_L = 20 pF; POD[1] = weak
		–	50	ns	C_L = 50 pF; POD[1] = medium
		–	28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–	16	ns	C_L = 50 pF; POD[1] = strong; edge = soft;
Rise time	t_{RA1+} CC	–	150	ns	C_L = 20 pF; POD[1] = weak
		–	50	ns	C_L = 50 pF; POD[1] = medium
		–	28	ns	C_L = 50 pF; POD[1] = strong; edge = slow
		–	16	ns	C_L = 50 pF; POD[1] = strong; edge = soft

1) POD = Pin Out Driver

Table 22 Standard Pads Class_A2

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Input Leakage current	I_{OZA2} CC	-6	6	µA	$0\ V \leq V_{IN} < 0.5*V_{DDP} - 1\ V$; $0.5*V_{DDP} + 1\ V < V_{IN} \leq V_{DDP}$
		-3	3	µA	$0.5*V_{DDP} - 1\ V < V_{IN} < 0.5*V_{DDP} + 1$ V
Input high voltage	V_{IHA2} SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V

(table continues...)

Table 22 (continued) Standard Pads Class_A2

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Input low voltage	V_{ILA2} SR	-0.3	0.36 × V_{DDP}	V	
Output high voltage, POD = weak	V_{OHA2} CC	V_{DDP} - 0.4	–	V	I_{OH} ≥ -400 µA
		2.4	–	V	I_{OH} ≥ -500 µA
Output high voltage, POD = medium		V_{DDP} - 0.4	–	V	I_{OH} ≥ -1.4 mA
		2.4	–	V	I_{OH} ≥ -2 mA
Output high voltage, POD = strong		V_{DDP} - 0.4	–	V	I_{OH} ≥ -1.4 mA
		2.4	–	V	I_{OH} ≥ -2 mA
Output low voltage, POD = weak	V_{OLA2} CC	–	0.4	V	I_{OL} ≤ 500 µA
Output low voltage, POD = medium		–	0.4	V	I_{OL} ≤ 2 mA
Output low voltage, POD = strong		–	0.4	V	I_{OL} ≤ 2 mA
Fall time	t_{FA2} CC	–	150	ns	C_L = 20 pF; POD = weak
		–	50	ns	C_L = 50 pF; POD = medium
		–	3.7	ns	C_L = 50 pF; POD = strong; edge = sharp
		–	7	ns	C_L = 50 pF; POD = strong; edge = medium
		–	16	ns	C_L = 50 pF; POD = strong; edge = soft
Rise time	t_{RA2} CC	–	150	ns	C_L = 20 pF; POD = weak
		–	50	ns	C_L = 50 pF; POD = medium
		–	3.7	ns	C_L = 50 pF; POD = strong; edge = sharp

(table continues...)

Table 22 (continued) Standard Pads Class_A2

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
		–	7.0	ns	C_L = 50 pF; POD = strong; edge = medium
		–	16	ns	C_L = 50 pF; POD = strong; edge = soft

Table 23 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Input leakage current	I_{OZHIB} CC	-500	500	nA	0 V ≤ V_{IN} ≤ V_{BAT}
Input high voltage	V_{IHHIB} SR	0.6 × V_{BAT}	V_{BAT} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3	0.36 × V_{BAT}	V	
Input Hysteresis for HIB_IO pins[1)]	*HYSHIB* CC	0.1 × V_{BAT}	–	V	V_{BAT} ≥ 3.13 V
		0.06 × V_{BAT}	–	V	V_{BAT} < 3.13 V
Output high voltage, POD[1)] = medium	V_{OHHIB} CC	V_{BAT} - 0.4	–	V	I_{OH} ≥ -1.4 mA
Output low voltage	V_{OLHIB} CC	–	0.4	V	I_{OL} ≤ 2 mA
Fall time	t_{FHIB} CC	–	50	ns	V_{BAT} ≥ 3.13 V C_L = 50 pF
		–	100	ns	V_{BAT} < 3.13 V C_L = 50 pF
Rise time	t_{RHIB} CC	–	50	ns	V_{BAT} ≥ 3.13 V C_L = 50 pF
		–	100	ns	V_{BAT} < 3.13 V C_L = 50 pF

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.2 Analog to Digital Converters (VADC)

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 24 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Analog reference voltage[1]	V_{AREF} SR	V_{AGND} +1	–	V_{DDA}+0.05[2]	V	
Analog reference ground[1]	V_{AGND} SR	V_{SSM} - 0.05	–	V_{AREF} - 1	V	
Analog reference voltage range[1] [3]	V_{AREF} - V_{AGND} SR	1	–	V_{DDA} + 0.1	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[4]	I_{OZ1} CC	-100	–	200	nA	0.03 × V_{DDA} < V_{AIN} < 0.97 × V_{DDA}
		-500	–	100	nA	0 V ≤ V_{AIN} ≤ 0.03 × V_{DDA}
		-100	–	500	nA	0.97 × V_{DDA} ≤ V_{AIN} ≤ V_{DDA}
Input leakage current at V_{AREF}	I_{OZ2} CC	-1	–	1	µA	0 V ≤ V_{AREF} ≤ V_{DDA}
Input leakage current at V_{AGND}	I_{OZ3} CC	-1	–	1	µA	0 V ≤ V_{AGND} ≤ V_{DDA}
Internal ADC clock	f_{ADCI} CC	2	–	36	MHz	V_{DDA} = 3.3 V
Switched capacitance at the analog voltage inputs[5]	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the positive reference voltage input[1] [6]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[1]	$C_{AREFTOT}$ CC	–	20	40	pF	
Total Unadjusted Error	*TUE* CC	-4	–	4	LSB	12-bit resolution; V_{DDA} = 3.3 V; V_{AREF} = V_{DDA}[7]
Differential Non-Linearity Error[8]	EA_{DNL} CC	-3	–	3	LSB	
Gain Error[8]	EA_{GAIN} CC	-4	–	4	LSB	
Integral Non-Linearity[8]	EA_{INLCC}	-3	–	3	LSB	
Offset Error[8]	EA_{OFF} CC	-4	–	4	LSB	
RMS Noise[9]	E_{NRMS} CC	–	1	2[10] [11]	LSB	
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion V_{DDP} = 3.6 V, T_J = 150°C

(table continues...)

Table 24 (continued) VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Charge consumption on V_{AREF} per conversion[1)]	Q_{CONV} CC	–	30	–	pC	0 V ≤ V_{AREF} ≤ V_{DDA}[12)]
ON resistance of the analog input path	R_{AIN} CC	–	600	1200	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	
Resistance of the reference voltage input path	R_{AREF} CC	–	700	1700	Ohm	

1) Applies to AINx, when used as alternate reference input.
2) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).
3) If the analog reference voltage is below VDDA, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.
4) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see Figure 12).
5) The sampling capacity of the conversion C-network is pre-charged to $V_{AREF}/2$ before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from $V_{AREF}/2$.
6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.
7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.
8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.
9) This parameter is valid for soldered devices and requires careful analog board design.
10) Resulting worst case combined error is arithmetic combination of TUE and EN_{RMS}.
11) Value is defined for one sigma Gauss distribution.
12) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$. The fastest 12-bit post-calibrated conversion of t_c = 459 ns results in a typical average current of I_{AREF} = 65.4 µA.

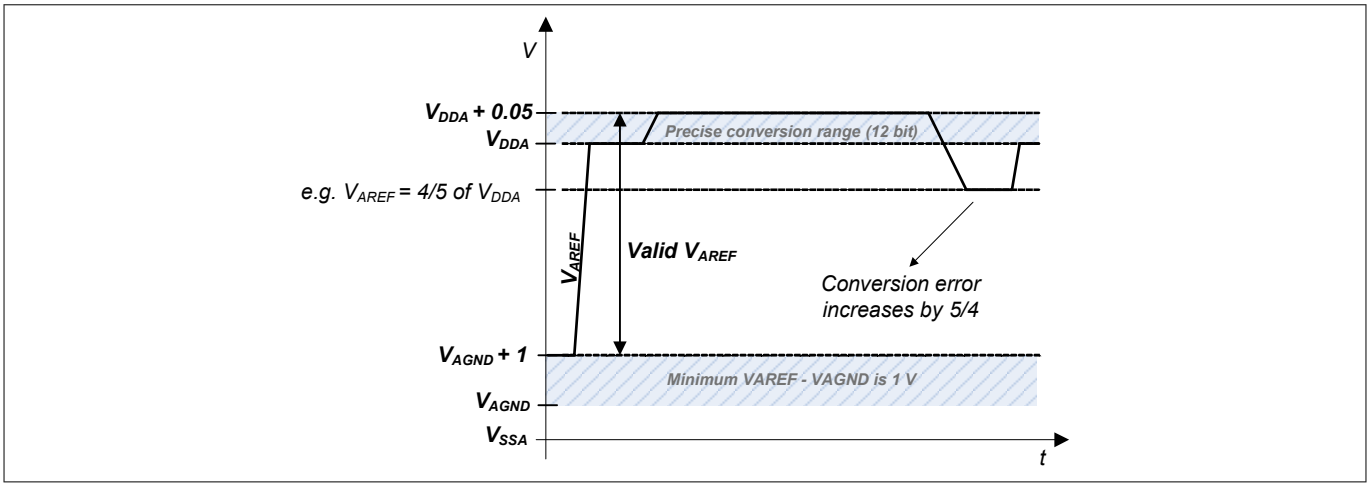

Figure 10 VADC Reference Voltage Range

The power-up calibration of the VADC requires a maximum number of 4352 f_{ADCI} cycles.

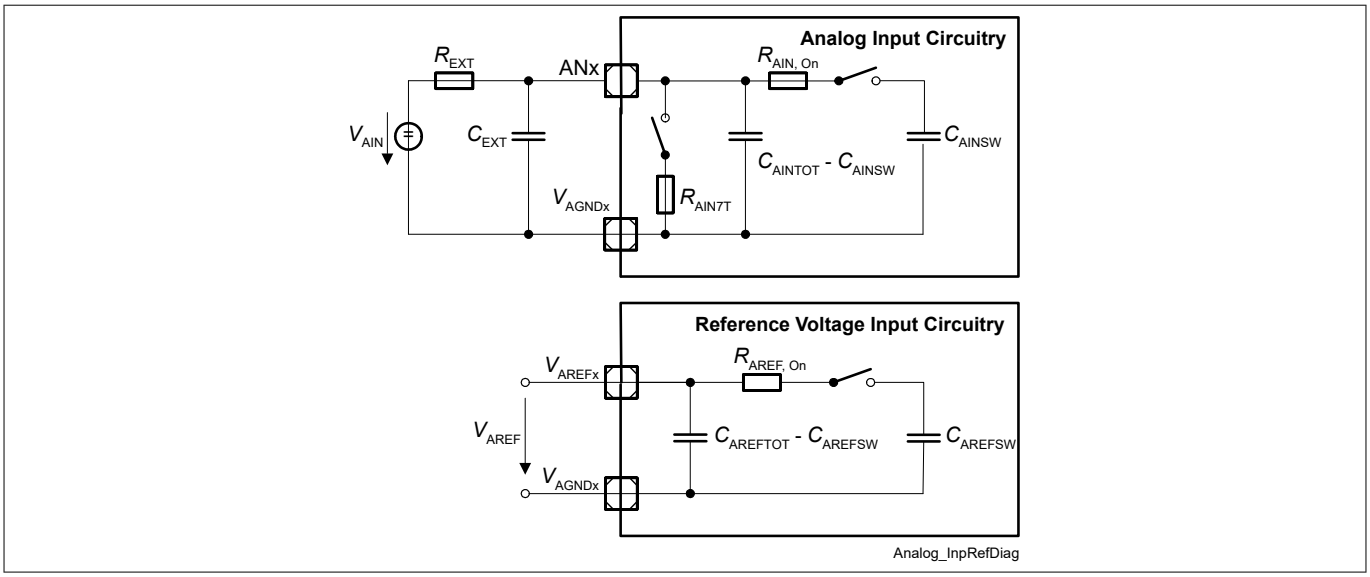

Figure 11 VADC Input Circuits

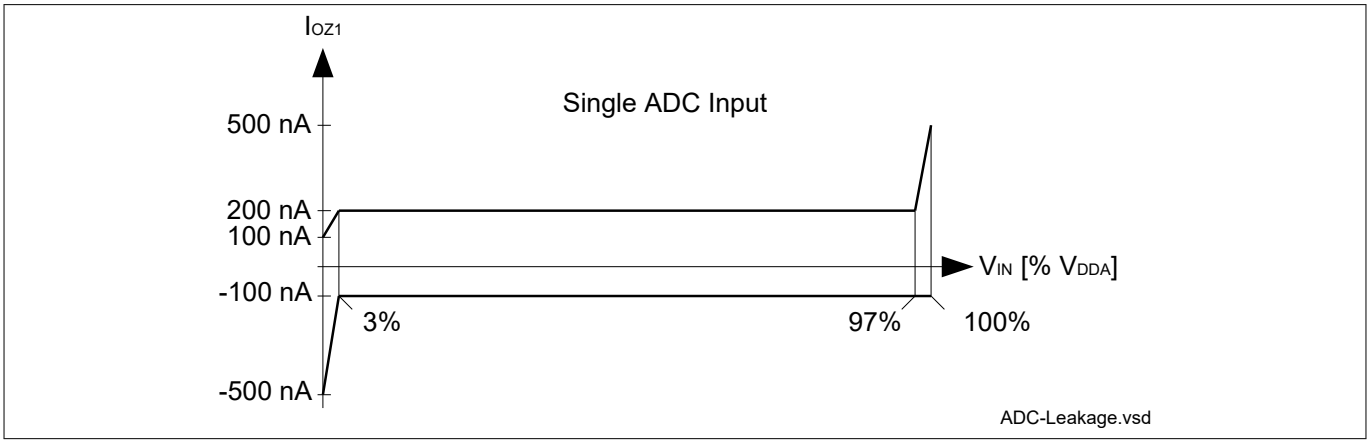

Figure 12 VADC Analog Input Leakage Current

Conversion Time

Table 25 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Values	Unit	Note
Conversion time	t_C CC	$2 \times T_{ADC} + (2 + N + STC + PC + DM) \times T_{ADCI}$	µs	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1/f_{PERIPH}$ $T_{ADCI} = 1/f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

Conversion Time Examples

System assumptions:
f_{ADC} = 144 MHz that is t_{ADC} = 6.9 ns, DIVA = 3, f_{ADCI} = 36 MHz that is t_{ADCI} = 27.8 ns
According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):
12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 27.8\ ns + 2 \times 6.9\ ns = 459\ ns$
12-bit uncalibrated conversion:
$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 27.8\ ns + 2 \times 6.9\ ns = 403\ ns$
10-bit uncalibrated conversion:
$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 27.8\ ns + 2 \times 6.9\ ns = 348\ ns$
8-bit uncalibrated:
$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 27.8\ ns + 2 \times 6.9\ ns = 292\ ns$

3.2.3 Digital to Analog Converters (DAC)

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 26 DAC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
RMS supply current	I_{DD} CC	–	2.5	4	mA	per active DAC channel, without load currents of DAC outputs
Resolution	*RES* CC	–	12	–	Bit	
Update rate	f_{URATE_A} CC	–		2	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 1LSB accuracy
Update rate	f_{URATE_F} CC	–		5	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy
Settling time	t_{SETTLE} CC	–	1	2	µs	at full scale jump, output voltage reaches target value ± 20 LSB
Slew rate	*SR* CC	2	5	–	V/µs	

(table continues...)

Table 26 (continued) DAC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Minimum output voltage	V_{OUT_MIN} CC	–	0.3	–	V	code value unsigned: 000_H; signed: 800_H
Maximum output voltage	V_{OUT_MAX} CC	–	2.5	–	V	code value unsigned: FFF_H; signed: $7FF_H$
Integral non-linearity	*INL* CC	-5.5	±2.5	5.5	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Differential non-linearity	*DNL* CC	-2	±1	2	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Offset error	ED_{OFF} CC		±20		mV	
Gain error	ED_{G_IN} CC	-6.5	-1.5	3	%	
Startup time	$t_{STARTUP}$ CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	f_{C1} CC	2.5	5	–	MHz	verified by design
Output sourcing current	I_{OUT_SOURCE} CC	–	-30	–	mA	
Output sinking current	I_{OUT_SINK} CC	–	0.6	–	mA	
Output resistance	R_{OUT} CC	–	50	–	Ohm	
Load resistance	R_L SR	5	–	–	kOhm	
Load capacitance	C_L SR	–	–	50	pF	
Signal-to-Noise Ratio	*SNR* CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	*THD* CC	–	70	–	dB	examination bandwidth < 25 kHz

(table continues...)

Table 26 (continued) DAC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Power Supply Rejection Ratio	*PSRR* CC	–	56	–	dB	to V_{DDA} verified by design

Conversion Calculation

Unsigned:

DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN})

Signed:

DACxDATA = 4095 × (V_{OUT} - V_{OUT_MIN}) / (V_{OUT_MAX} - V_{OUT_MIN}) - 2048

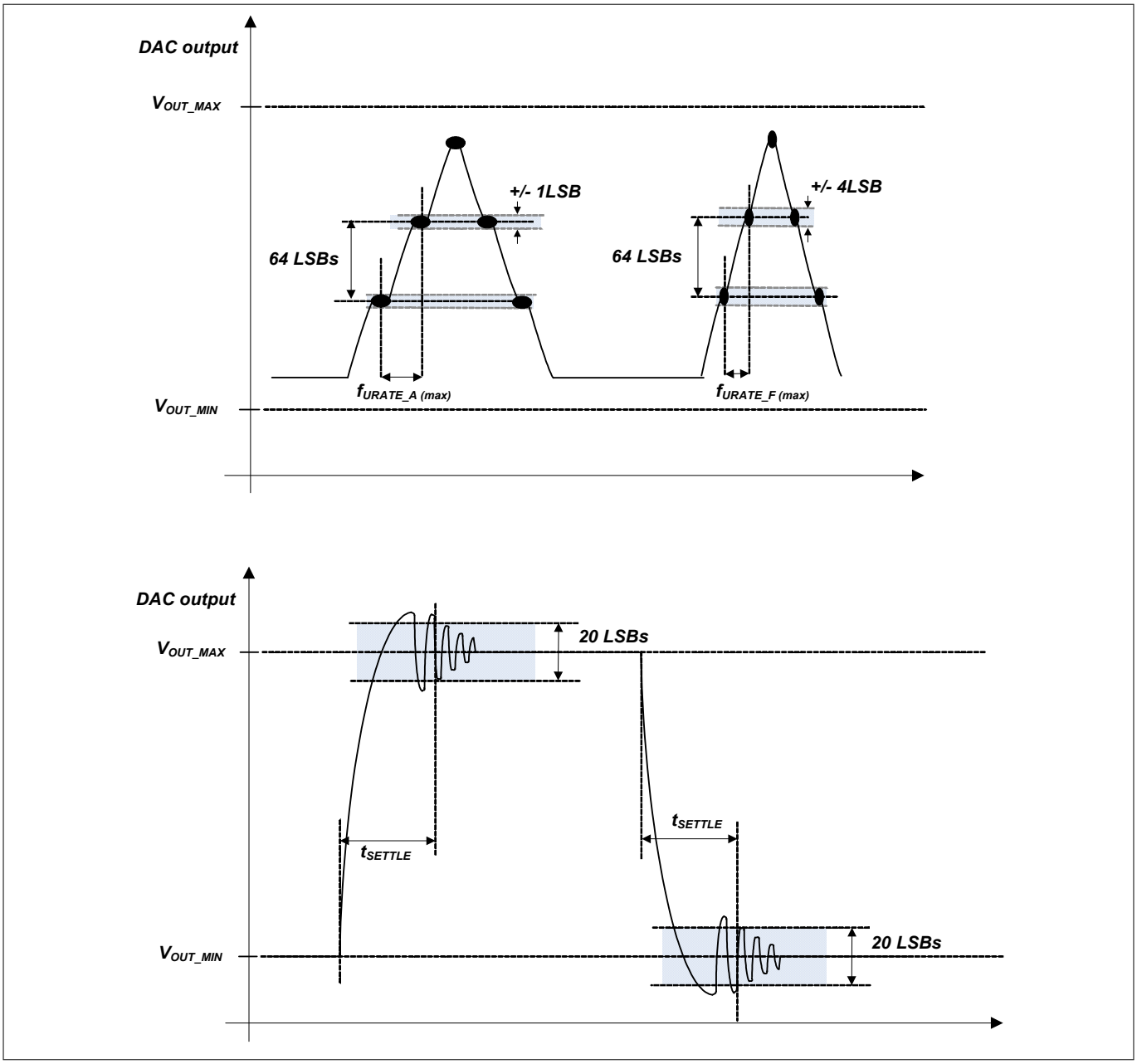

Figure 13 DAC Conversion Examples

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference[1] (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

The parameters in Table 27 apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

Table 27 ORC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
DC Switching Level	V_{ODC} CC	100	125	210	mV	$V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	V_{OHYS} CC	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	t_{ODD} CC	50	–	450	ns	$V_{AIN} \geq V_{AREF} +$ 210 mV
		45	–	105	ns	$V_{AIN} \geq V_{AREF} +$ 400 mV
Always detected Overvoltage Pulse	t_{OPDD} CC	440	–	–	ns	$V_{AIN} \geq V_{AREF} +$ 210 mV
		90	–	–	ns	$V_{AIN} \geq V_{AREF} +$ 400 mV
Never detected Overvoltage Pulse	t_{OPDN} CC	–	–	45	ns	$V_{AIN} \geq V_{AREF} +$ 210 mV
		–	–	30	ns	$V_{AIN} \geq V_{AREF} +$ 400 mV
Release Delay	t_{ORD} CC	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	t_{OED} CC	–	100	200	ns	

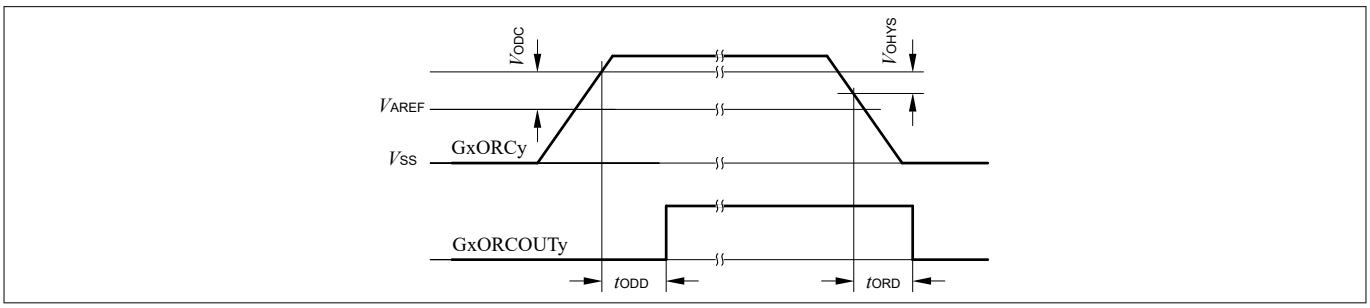

Figure 14 GxORCOUTy Trigger Generation

[1] Always the standard VADC reference, alternate references do not apply to the ORC.

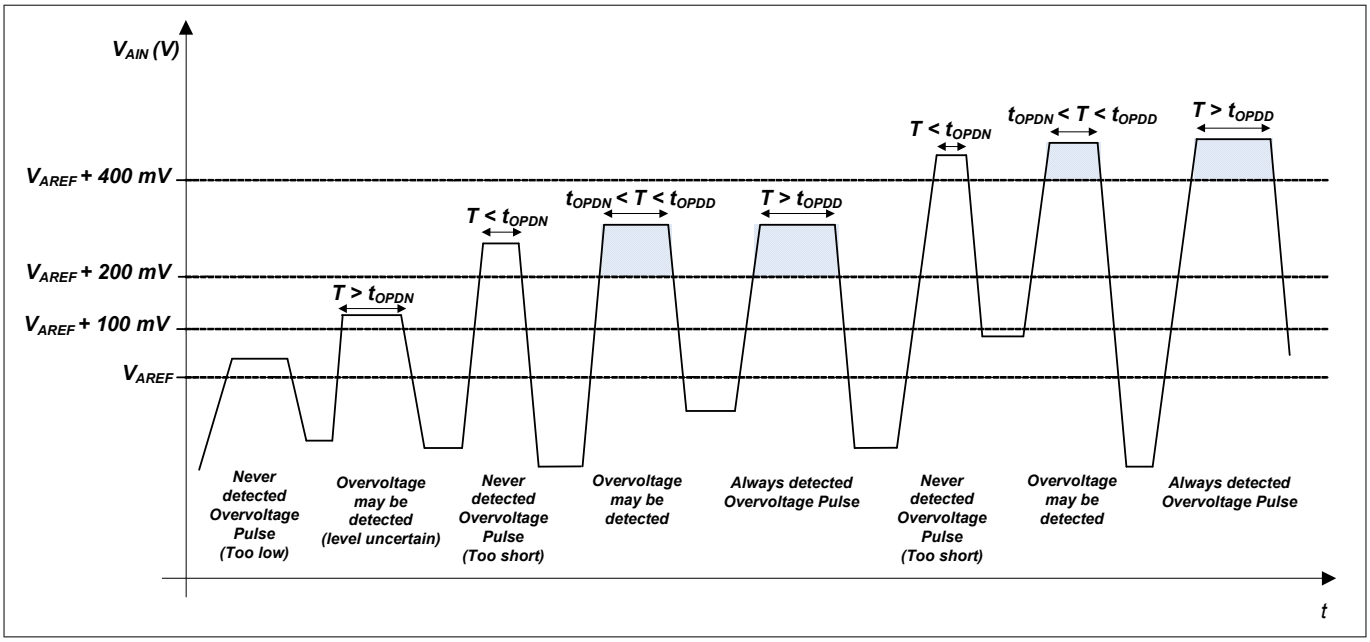

Figure 15 ORC Detection Ranges

3.2.5 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 28 Die Temperature Sensor Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Temperature sensor range	T_{SR} SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	ΔT_{LE} CC	–	±1	–	°C	per $\Delta T_J \leq 30°C$
Offset Error	ΔT_{OE} CC	–	±6	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3$ V[1)]
Measurement time	t_M CC	–	–	100	µs	
Start-up time after reset inactive	t_{TSST} SR	–	–	10	µs	

1) At $V_{DDP\_max} = 3.63$ V the typical offset error increases by an additional $\Delta T_{OE} = ±1°C$.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

Temperature T_{DTS} = (RESULT - 605)/2.05 [°C]

This formula and the values defined in Table 28 apply with the following calibration values:

- DTSCON.BGTRIM = 8_H
- DTSCON.REFTRIM = 4_H

3.2.6 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 29 USB OTG VBUS and ID Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
VBUS input voltage range	V_{IN} CC	0.0	–	5.25	V	
A-device VBUS valid threshold	V_{B1} CC	4.4	–	–	V	
A-device session valid threshold	V_{B2} CC	0.8	–	2.0	V	
B-device session valid threshold	V_{B3} CC	0.8	–	4.0	V	
B-device session end threshold	V_{B4} CC	0.2	–	0.8	V	
VBUS input resistance to ground	R_{VBUS_IN} CC	40	–	100	kOhm	
B-device VBUS pull-up resistor	R_{VBUS_PU} CC	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	R_{VBUS_PD} CC	656	–	–	Ohm	
USB.ID pull-up resistor	R_{UID_PU} CC	14	–	25	kOhm	
VBUS input current	I_{VBUS_IN} CC	–	–	150	µA	0 V ≤ V_{IN} ≤ 5.25 V: T_{AVG} = 1 ms

Table 30 USB OTG Data Line (USB_DP, USB_DM) Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input low voltage	V_{IL} SR	–	–	0.8	V	
Input high voltage (driven)	V_{IH} SR	2.0	–	–	V	
Input high voltage (floating)[1)]	V_{IHZ} SR	2.7	–	3.6	V	
Differential input sensitivity	V_{DIS} CC	0.2	–	–	V	

(table continues...)

Table 30 (continued) USB OTG Data Line (USB_DP, USB_DM) Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Differential common mode range	V_{CM} CC	0.8	–	2.5	V	
Output low voltage	V_{OL} CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH} CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI} CC	900	–	1575	Ohm	
DP pull-up resistor (upstream port receiving)	R_{PUA} CC	1425	–	3090	Ohm	
DP, DM pull-down resistor	R_{PD} CC	14.25	–	24.8	kOhm	
Input impedance DP, DM	Z_{INP} CC	300	–	–	kOhm	$0\ V \le V_{IN} \le V_{DDP}$
Driver output resistance DP, DM	Z_{DRV} CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm ± 5% to 3.3 V ± 0.3 V connected to USB_DP or USB_DM and at B-connector with 15 kOhm ± 5% to ground connected to USB_DP and USB_DM.

3.2.7 Oscillator Pins

***Note**: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.*

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

The oscillator pins can be operated with an external crystal (see Figure 16) or in direct input mode (see Figure 17).

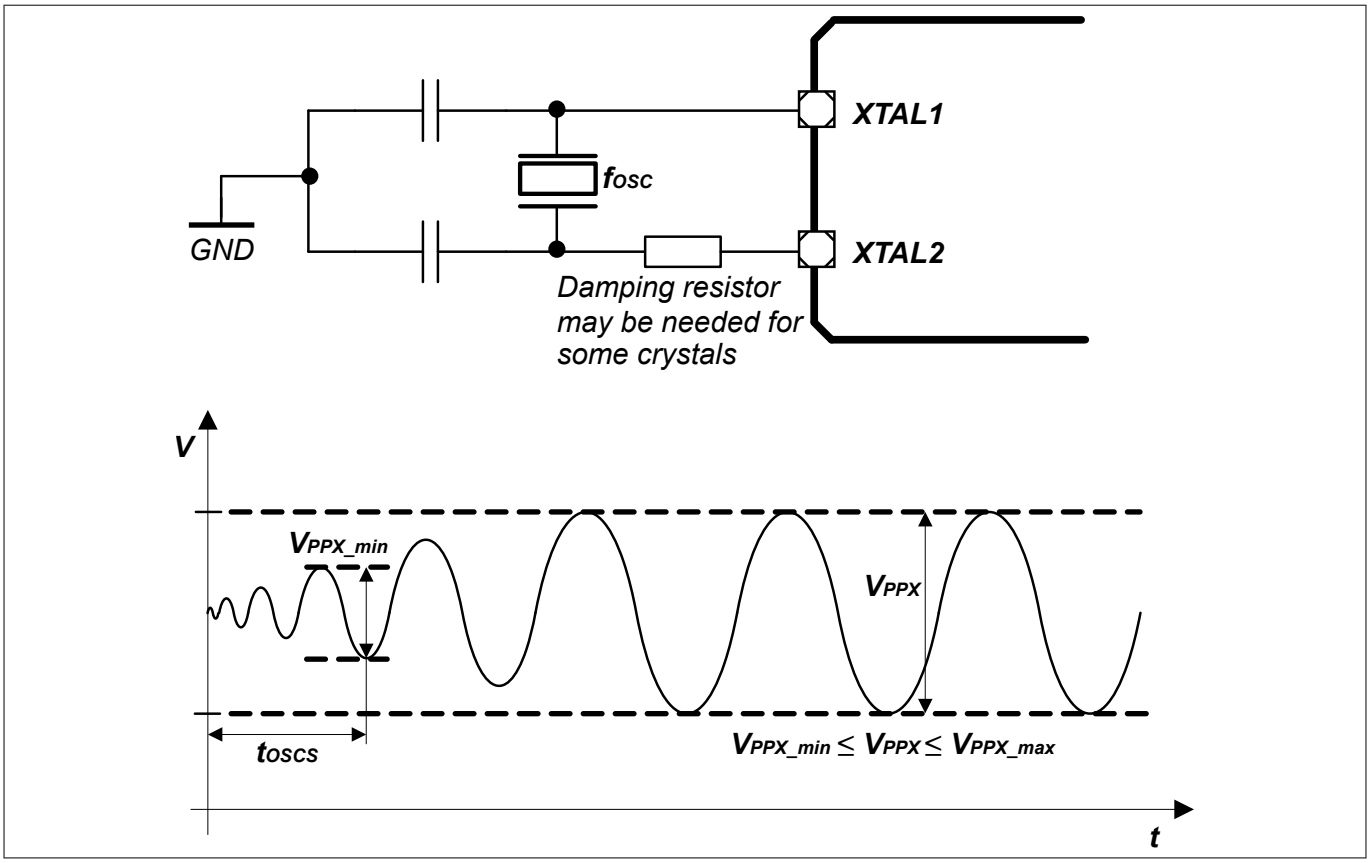

Figure 16 Oscillator in Crystal Mode

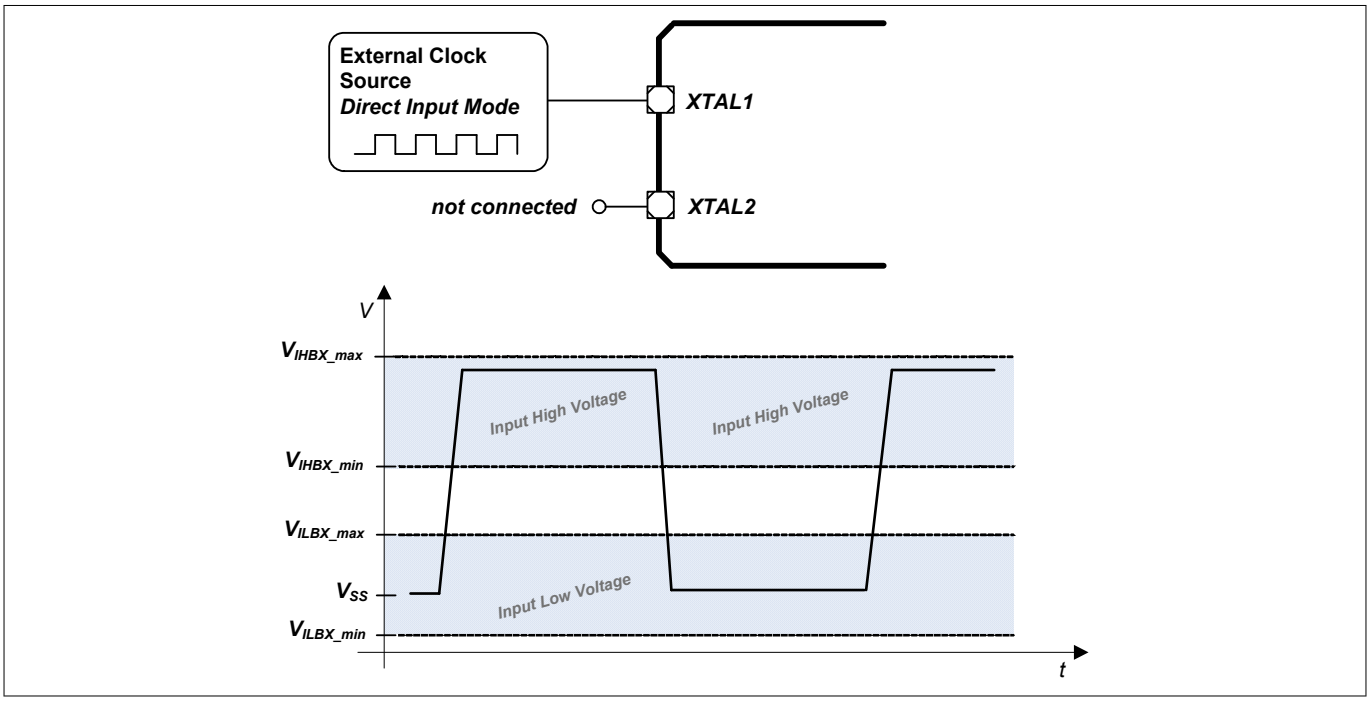

Figure 17 Oscillator in Direct Input Mode

Table 31 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time[1) 2)]	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.5	–	V_{DDP} + 0.5	V	
Input amplitude (peak-to-peak) at XTAL1[2) 3)]	V_{PPX} SR	0.4 × V_{DDP}	–	V_{DDP} + 1.0	V	
Input high voltage at XTAL1[4)]	V_{IHBX} SR	1.0	–	V_{DDP} + 0.5	V	
Input low voltage at XTAL1[4)]	V_{ILBX} SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down 0 V ≤ V_{IX} ≤ V_{DDP}

1) t_{OSCS} is defined from the moment the oscillator is enabled with SCU_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of 0.4 * V_{DDP}.
2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
3) If the shaper unit is enabled and not bypassed.
4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

Table 32 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time[1) 2) 3)]	t_{OSCS} CC	–	–	5	s	
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	V_{BAT} + 0.3	V	
Input amplitude (peak-to-peak) at RTC_XTAL1[2) 4)]	V_{PPX} SR	0.4	–	–	V	
Input high voltage at RTC_XTAL1[5)]	V_{IHBX} SR	0.6 × V_{BAT}	–	V_{BAT} + 0.3	V	
Input low voltage at RTC_XTAL1[5)]	V_{ILBX} SR	-0.3	–	0.36 × V_{BAT}	V	
Input Hysteresis for RTC_XTAL1[5) 6)]	V_{HYSX} CC	0.1 × V_{BAT}		–	V	3.0 V ≤ V_{BAT} < 3.6 V
		0.03 × V_{BAT}		–	V	V_{BAT} < 3.0 V

(table continues...)

Table 32 (continued) RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input leakage current at RTC_XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down $0\ V \le V_{IX} \le V_{BAT}$

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 400 mV.
2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.
3) For a reliable start of the oscillation in crystal mode it is required that $V_{BAT} \ge 3.0$ V. A running oscillation is maintained across the full V_{BAT} voltage range.
4) If the shaper unit is enabled and not bypassed.
5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.
6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

If not stated otherwise, the operating conditions for the parameters in the following table are:

$V_{DDP} = 3.3$ V, $T_A = 25°C$

Table 33 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Active supply current[1) 2)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA} CC	–	135	–	mA	144/144/144
		–	125	–		144/72/72
		–	97	–		72/72/144
		–	80	–		24/24/24
		–	68	–		1/1/1
Active supply current Code execution from RAM Flash in Sleep mode	I_{DDPA} CC	–	108	–	mA	144/144/144
		–	98	–		144/72/72
Active supply current[3)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA} CC	–	86	–	mA	144/144/144
		–	85	–		144/72/72
		–	70	–		72/72/144
		–	55	–		24/24/24
		–	50	–		1/1/1

(table continues...)

Table 33 (continued) Power Supply Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Sleep supply current[4] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	127	–	mA	144/144/144
		–	115	–		144/72/72
		–	93	–		72/72/144
		–	57	–		24/24/24
		–	47	–		1/1/1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	48	–		100/100/100
Sleep supply current[5] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	77	–	mA	144/144/144
		–	76	–		144/72/72
		–	65	–		72/72/144
		–	53	–		24/24/24
		–	46	–		1/1/1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	47	–		100/100/100
Deep Sleep supply current[6] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	11	–	mA	24/24/24
		–	7.0	–		4/4/4
		–	6.6	–		1/1/1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	7.6	–		100/100/100[7]
Hibernate supply current RTC on[8]	I_{DDPH} CC	–	8.7	–	µA	V_{BAT} = 3.3 V
		–	6.5	–		V_{BAT} = 2.4 V
		–	5.7	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[9]	I_{DDPH} CC	–	8.0	–	µA	V_{BAT} = 3.3 V
		–	6.0	–		V_{BAT} = 2.4 V
		–	5.0	–		V_{BAT} = 2.0 V
Hibernate off[10]	I_{DDPH} CC	–	4.4	–	µA	V_{BAT} = 3.3 V
		–	3.5	–		V_{BAT} = 2.4 V
		–	3.1	–		V_{BAT} = 2.0 V
Worst case active supply current[11]	I_{DDPA} CC	–	–	250[2]	mA	V_{DDP} = 3.6 V, T_J = 150°C
V_{DDA} power supply current	I_{DDA} CC	–	–	-[12]	mA	
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST} CC	–	5	10	mA	V_{DDP} = 3.3 V, T_J = 25°C
		–	13	55	mA	V_{DDP} = 3.6 V, T_J = 150°C

(table continues...)

Table 33 (continued) Power Supply Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Power Dissipation	P_{DISS} CC	–	–	1.4	W	V_{DDP} = 3.6 V, T_J = 150°C
Wake-up time from Sleep to Active mode	t_{SSA} CC	–	6	–	cycles	
Wake-up time from Deep Sleep to Active mode		–	–	–	ms	Defined by the wake-up of the Flash module, see "Flash Memory Parameters "
Wake-up time from Hibernate mode		–	–	–	ms	Wake-up via power-on reset event, see "Power-Up and Supply Monitoring"

1) CPU executing code from Flash, all peripherals idle.
2) I_{DDP} decreases typically by approximately 5 mA when f_{SYS} decreases by 10 MHz, at constant T_J.
3) CPU executing code from Flash.
4) CPU in sleep, all peripherals idle, Flash in Active mode.
5) CPU in sleep, Flash in Active mode.
6) CPU in sleep, peripherals disabled, after wake-up code execution from RAM.
7) To wake-up the Flash from its Sleep mode, $f_{CPU} \geq 1$ MHz is required.
8) OSC_ULP operating with external crystal on RTC_XTAL.
9) OSC_ULP off, Hibernate domain operating with OSC_SI clock.
10) V_{BAT} supplied, but Hibernate domain not started; for example state after factory assembly.
11) Test Power Loop: f_{SYS} = 144 MHz, CPU executing benchmark code from Flash, all CCUs in 100 kHz timer mode, all ADC groups in continuous conversion mode, USICs as SPI in internal loop-back mode, CAN in 500 kHz internal loop-back mode, interrupt triggered DMA block transfers to parity protected RAMs and FCE, DTS measurements and FPU calculations.
The power consumption of each customer application will most probably be lower than this value, but must be evaluated separately.
12) Sum of currents of all active converters (ADC and DAC).

Peripheral Idle Currents

Default test conditions:

- f_{sys} and derived clocks at 144 MHz
- V_{DDP} = 3.3 V, T_a = 25°C
- all peripherals are held in reset (see the PRSTAT registers in the Reset Control Unit of the SCU)
- the peripheral clocks are disabled (see CGATSTAT registers in the Clock Control Unit of the SCU
- no I/O activity

The given values are a result of differential measurements with asserted and deasserted peripheral reset as well as disabled and enabled clock of the peripheral under test.

The tested peripheral is left in the state after the peripheral reset is deasserted, no further initialisation or configuration is done. For example no timer is running in the CCUs, no communication active in the USICs, etc.

Table 34 Peripheral Idle Currents

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
PORTS FCE WDT	I_{PER} CC	–	≤0.3	–	mA	
MultiCAN ERU LEDTSCU0 ETH CCU4x[1], CCU8x[1]		–	≤1.0	–		
DAC (digital)[2]		–	1.3	–		
USICx SDMMC		–	3.0	–		
VADC (digital)[2]		–	4.5	–		
DMA0, USB, EtherCAT		–	6.0	–		

1) Enabling the f_{CCU} clock for the CCU4x/CCU8x modules adds approximately I_{PER} = 4.8 mA, disregarding which and how many of those peripherals are enabled.
2) The current consumption of the analog components are given in the dedicated Datasheet sections of the respective peripheral.

3.2.9 Flash Memory Parameters

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 35 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	t_{ERP} CC	–	5	5.5	s	
Erase Time per 64 Kbyte Sector	t_{ERP} CC	–	1.2	1.4	s	
Erase Time per 16 Kbyte Logical Sector	t_{ERP} CC	–	0.3	0.4	s	
Program time per page[1]	t_{PRP} CC	–	5.5	11	ms	
Erase suspend delay	t_{FL_ErSusp} CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	µs	
Wake-up time	t_{WU} CC	–	–	270	µs	
Read access time	t_a CC	22	–	–	ns	For operation with $1/f_{CPU} < t_a$ wait states must be configured[2]
Data Retention Time, Physical Sector[3] [4]	t_{RET} CC	20	–	–	years	Max. 1000 erase/ program cycles
Data Retention Time, Logical Sector[3] [4]	t_{RETL} CC	20	–	–	years	Max. 100 erase/ program cycles
Data Retention Time, User Configuration Block (UCB)[3] [4]	t_{RTU} CC	20	–	–	years	Max. 4 erase/ program cycles per UCB
Endurance on 64 Kbyte Physical Sector PS4	N_{EPS4} CC	10000	–	–	cycles	Cycling distributed over life time[5]

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.
2) The following formula applies to the wait state configuration: FCON.WSPFLASH × $(1/f_{CPU}) \geq t_a$.
3) Storage and inactive time included.
4) Values given are valid for an average weighted junction temperature of $T_J = 110°C$.
5) Only valid with robust EEPROM emulation algorithm, equally cycling the logical sectors. For more details see the Reference Manual.

3.3 AC Parameters

3.3.1 Testing Waveforms

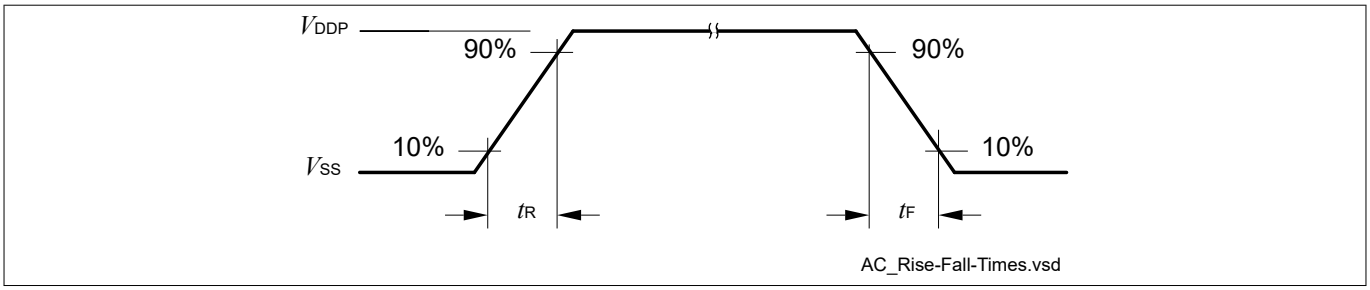

Figure 18 Rise/Fall Time Parameters

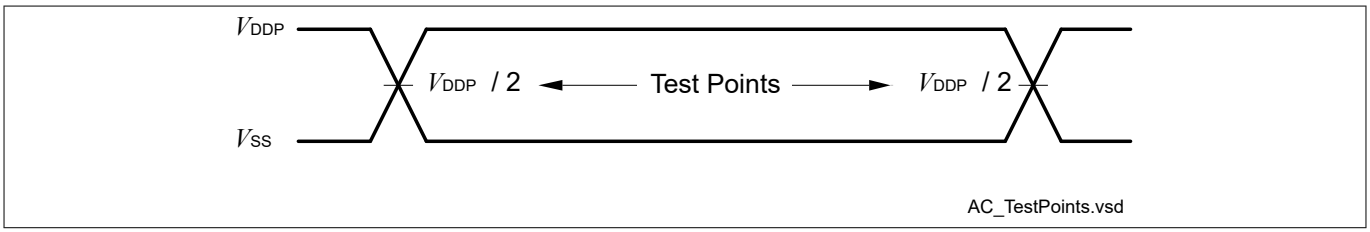

Figure 19 Testing Waveform, Output Delay

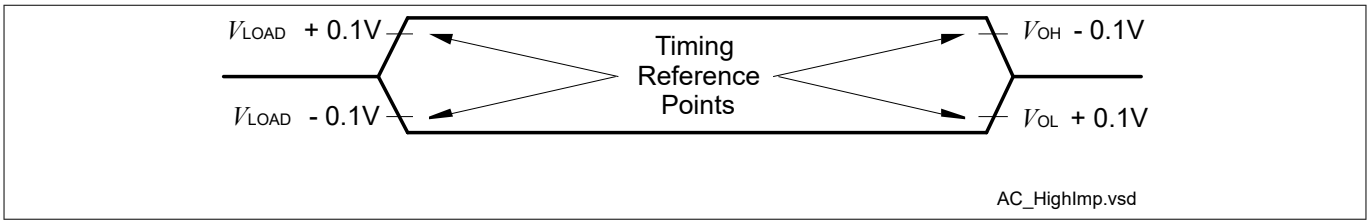

Figure 20 Testing Waveform, Output High Impedance

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

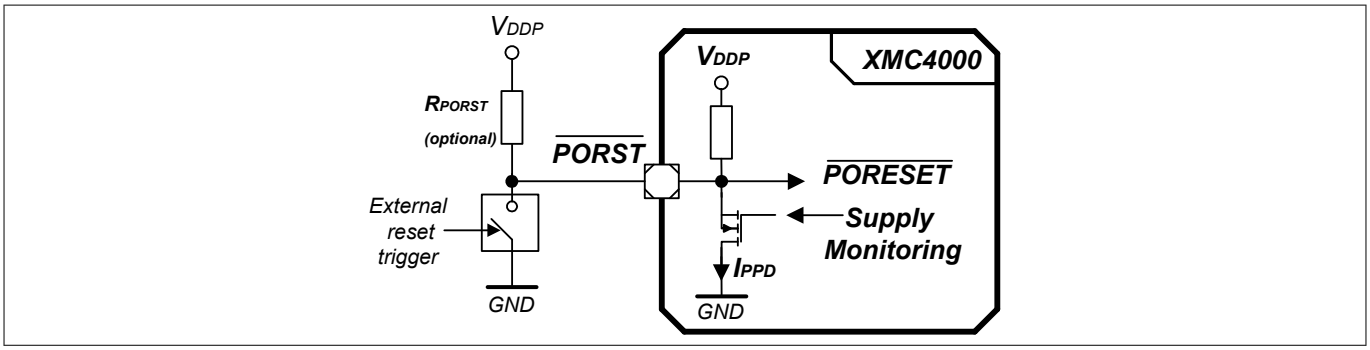

Figure 21 $\overline{\text{PORST}}$ **Circuit**

Table 36 Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79[1]	–	3.05[2]	V	[3]
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	t_{PR} SR	–	–	2	µs	[4]
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	µs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.
2) Maximum threshold for reset deassertion.
3) The V_{DDP} monitoring has a typical hysteresis of V_{PORHYS} = 180 mV.
4) If t_{PR} is not met, low spikes on $\overline{\text{PORST}}$ may be seen during start up (e.g. reset pulses generated by the supply monitoring due to a slow ramping V_{DDP}).

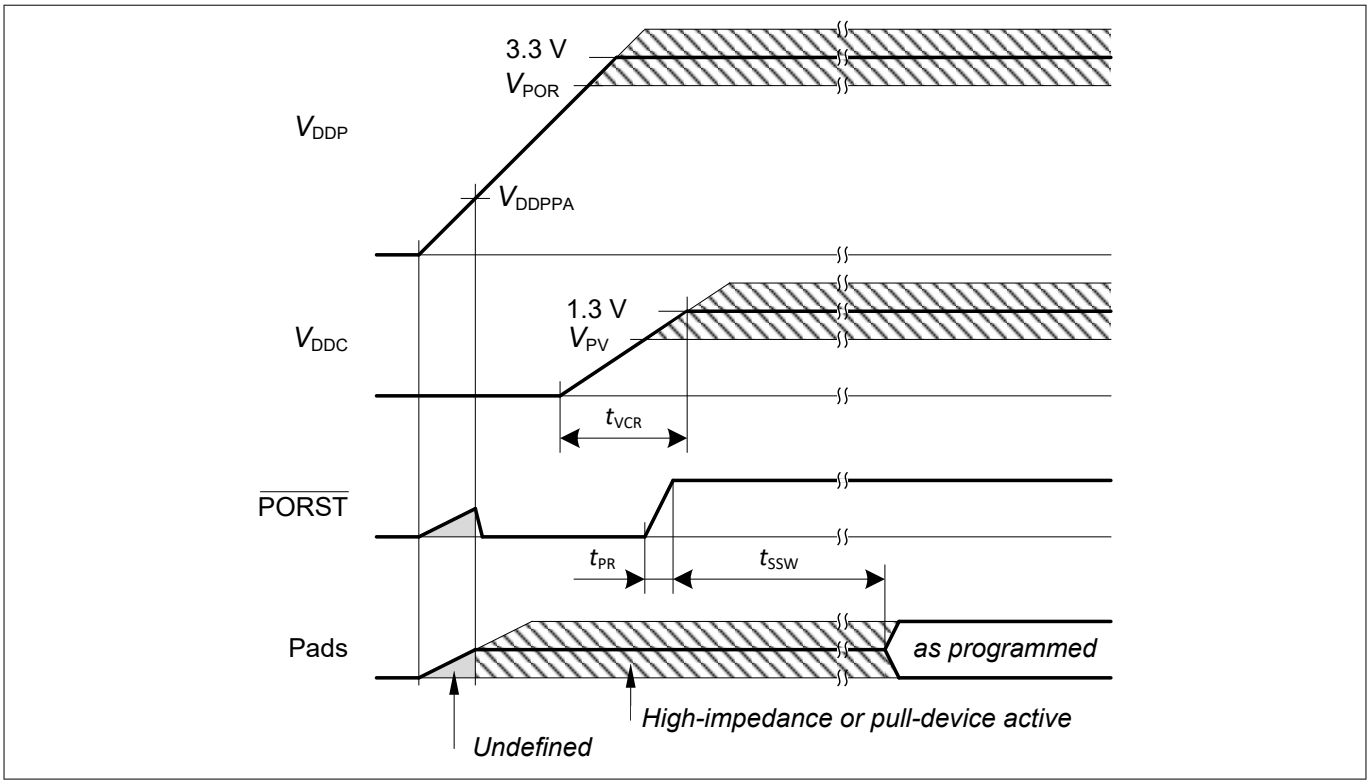

Figure 22 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU}. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 37 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	–	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	–	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over-/ Undershoot from Load Step	ΔV_{LS} CC	–	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	–	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	–	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	–	10	–	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:

$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 144 MHz, main PLL f_{VCO} = 288 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 72 MHz - 96 MHz - 144 MHz (K2 steps 12 - 6 - 4 - 3 - 2)

24 MHz - 48 MHz - 96 MHz - 144 MHz (K2 steps 12 - 6 - 3 - 2)

24 MHz - 72 MHz - 144 MHz (K2 steps 12 - 4 - 2)

3.3.4 Phase Locked Loop (PLL) Characteristics

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Main and USB PLL

Table 38 PLL Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	–	–	±5	ns	accumulated over 300 cycles f_{SYS} = 144 MHz
Duty Cycle[1)]	D_{DC} CC	46	50	54	%	Low pulse to total period, assuming an ideal input clock source
PLL base frequency	$f_{PLLBASE}$ CC	30	–	140	MHz	
VCO input frequency	f_{REF} CC	4	–	16	MHz	
VCO frequency range	f_{VCO} CC	260	–	520	MHz	
PLL lock-in time	t_L CC	–	–	400	µs	

1) 50% for even K2 divider values, 50±(10/K2) for odd K2 divider values.

3.3.5 Internal Clock Source Characteristics

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Fast Internal Clock Source

Table 39 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1) 2)]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3)] 3.13 V ≤ V_{DDP} ≤ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

1) Error in addition to the accuracy of the reference clock.
2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.
3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

Slow Internal Clock Source

Table 40 Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OSI} CC	–	32.768	–	kHz	
Accuracy	Δf_{OSI} CC	-4	–	4	%	V_{BAT} = const. 0°C ≤ T_A ≤ 85°C
		-5	–	5	%	V_{BAT} = const. T_A < 0°C or T_A > 85°C
		-5	–	5	%	2.4 V ≤ V_{BAT}, T_A = 25°C
		-10	–	10	%	1.95 V ≤ V_{BAT} < 2.4 V, T_A = 25°C
Start-up time	t_{OSIS} CC	–	50	–	µs	

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

***Note**: Operating conditions apply.*

Table 41 JTAG Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	–	–	ns	
TCK high time	t_2 SR	10	–	–	ns	
TCK low time	t_3 SR	10	–	–	ns	
TCK clock rise time	t_4 SR	–	–	4	ns	
TCK clock fall time	t_5 SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid after TCK falling edge[1] (propagation delay)	t_8 CC	–	–	13	ns	C_L = 50 pF
		3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18} CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1] [2]	t_9 CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10} CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.
2) The setup time for TDO is given implicitly by the TCK cycle time.

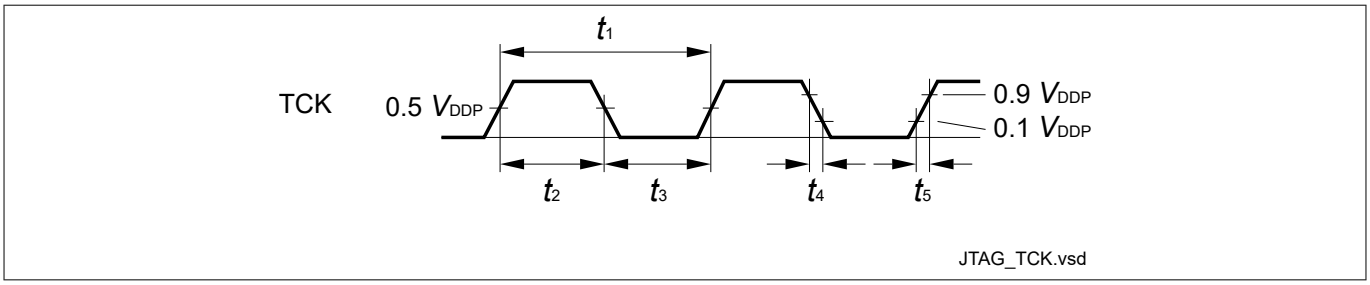

Figure 23 Test Clock Timing (TCK)

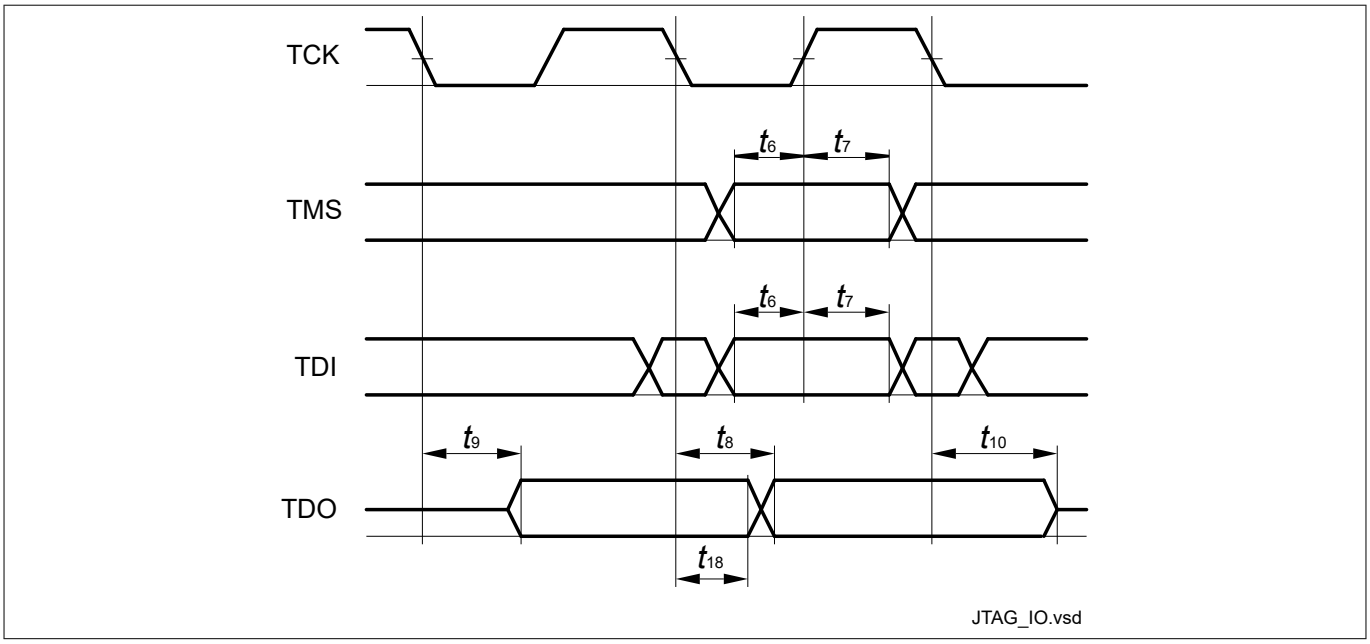

Figure 24 JTAG Timing

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

***Note**: Operating conditions apply.*

Table 42 SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
SWDCLK clock period	t_{SC} SR	25	–	–	ns	C_L = 30 pF
		40	–	–	ns	C_L = 50 pF
SWDCLK high time	t_1 SR	10	–	500000	ns	
SWDCLK low time	t_2 SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	t_3 SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	t_4 SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	t_5 CC	–	–	17	ns	C_L = 50 pF
		–	–	13	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	3	–	–	ns	

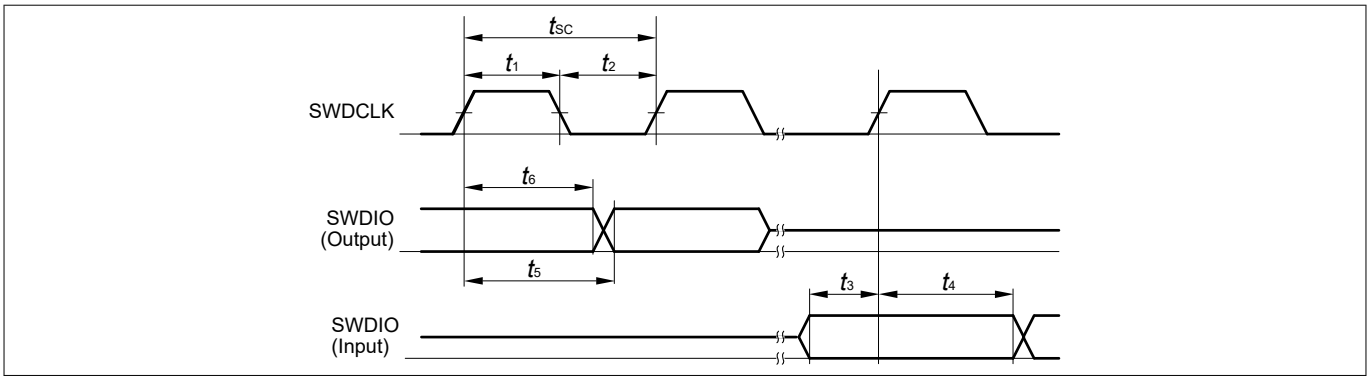

Figure 25 SWD Timing

3.3.8 Peripheral Timing

3.3.8.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 43 USIC SSC Master Mode Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK} CC	33.3	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{PB} - 6.5[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{PB} - 8.5[1)]	–	–	ns	
Data output DOUT[3:0] valid time	t_3 CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4 SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5 SR	1	–	–	ns	

1) $t_{PB} = 1/f_{PB}$

Table 44 USIC SSC Slave Mode Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK} SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10} SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11} SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1)]	t_{12} SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1)]	t_{13} SR	4	–	–	ns	
Data output DOUT[3:0] valid time	t_{14} CC	0	–	24	ns	

1) This input timing is valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

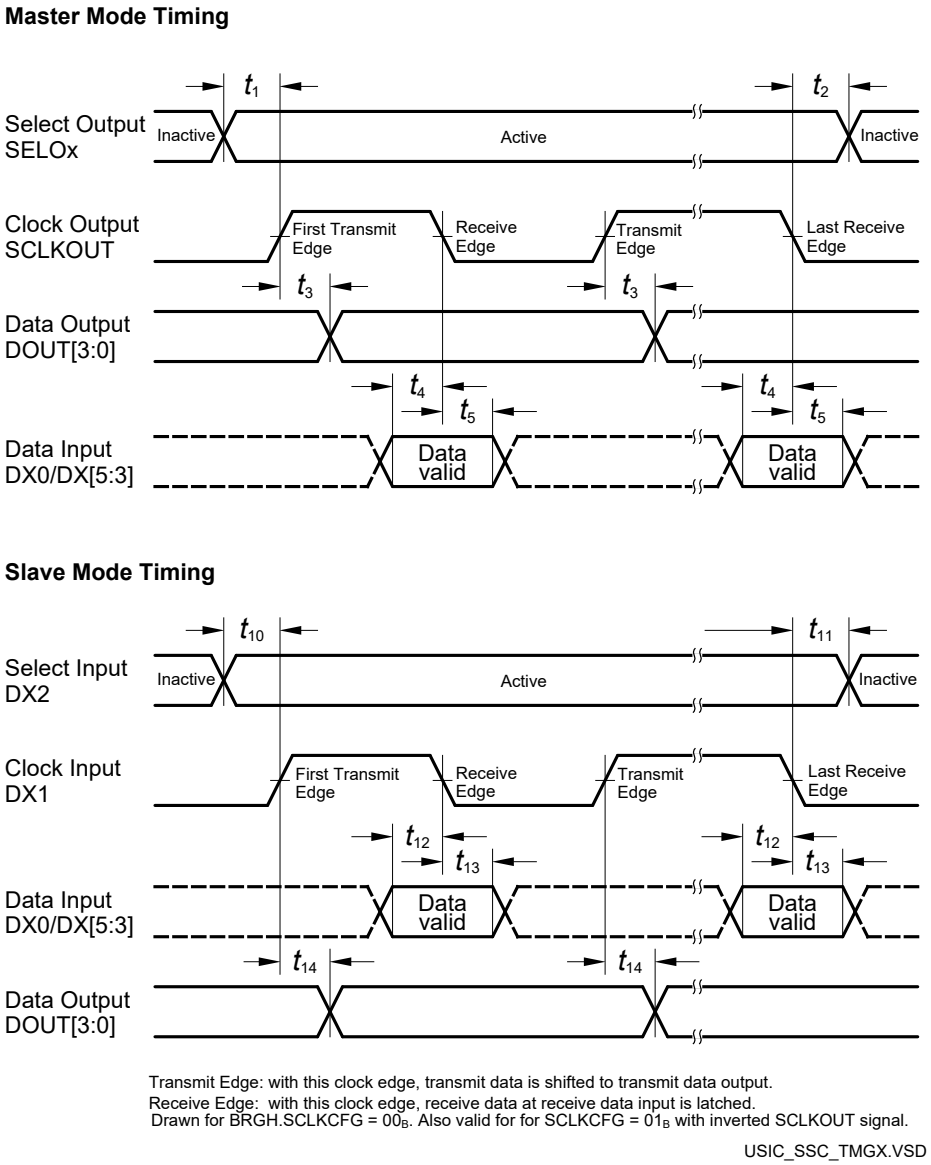

Figure 26 USIC - SSC Master/Slave Mode Timing

***Note**: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

3.3.8.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 45 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	–	–	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	–	–	1000	ns	
Data hold time	t_3 CC/SR	0	–	–	µs	
Data set-up time	t_4 CC/SR	250	–	–	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	–	–	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	–	–	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	–	–	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	–	–	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	–	–	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	–	–	µs	
Capacitive load for each bus line	C_b SR	–	–	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 46 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b[2)]	–	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b[2)]	–	300	ns	
Data hold time	t_3 CC/SR	0	–	–	µs	
Data set-up time	t_4 CC/SR	100	–	–	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	–	–	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	–	–	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	–	–	µs	

(table continues...)

Table 46 (continued) USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Set-up time for repeated START condition	t_8 CC/SR	0.6	–	–	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	–	–	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	–	–	µs	
Capacitive load for each bus line	C_b SR	–	–	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.
2) C_b refers to the total capacitance of one bus line in pF.

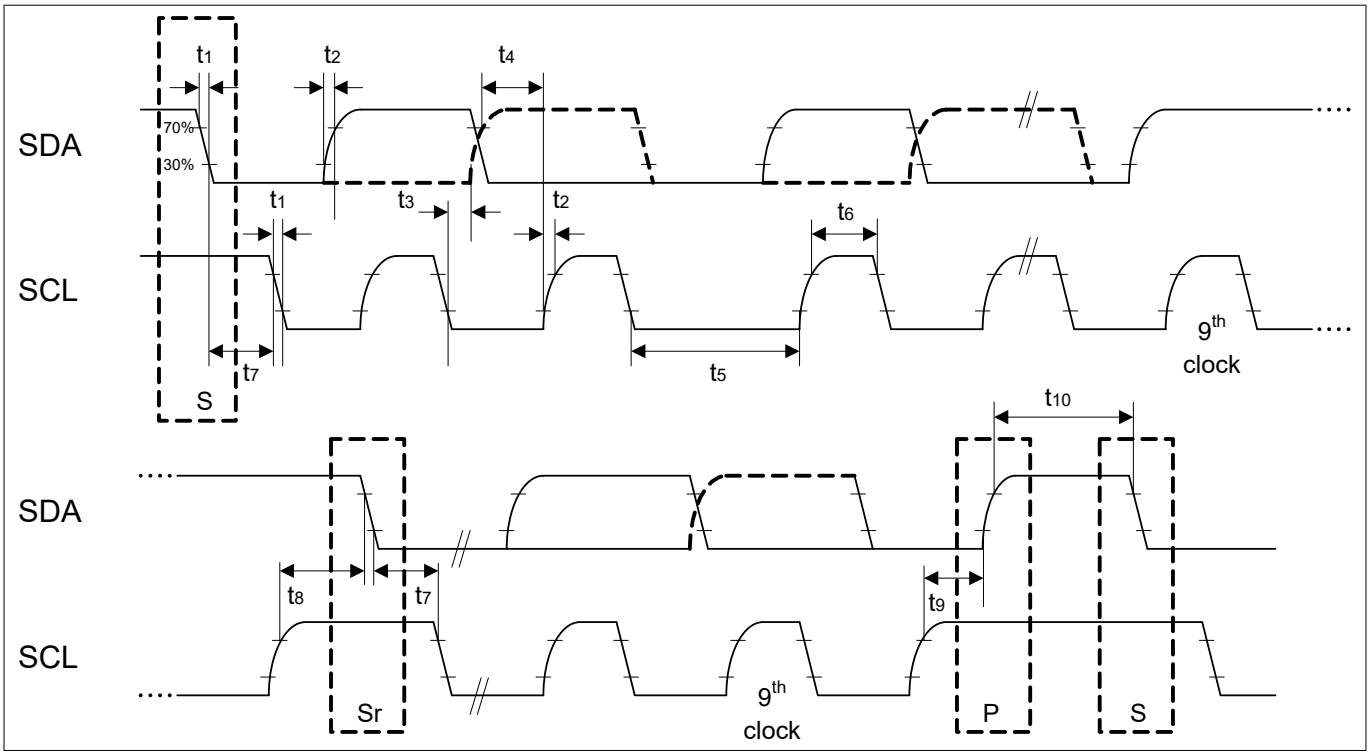

Figure 27 USIC IIC Stand and Fast Mode Timing

3.3.8.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 47 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	33.3	–	–	ns	
Clock high time	t_2 CC	0.35 x t_{1min}	–	–	ns	
Clock low time	t_3 CC	0.35 x t_{1min}	–	–	ns	
Hold time	t_4 CC	0	–	–	ns	
Clock rise time	t_5 CC	–	–	0.15 x t_{1min}	ns	

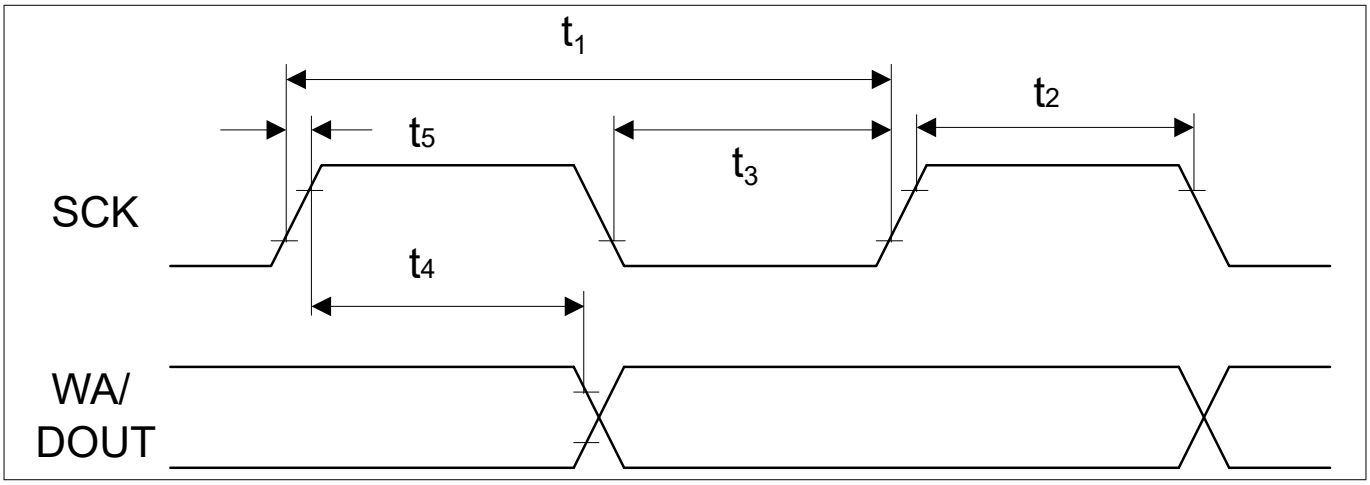

Figure 28 USIC IIS Master Transmitter Timing

Table 48 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	66.6	–	–	ns	
Clock high time	t_7 SR	0.35 x t_{6min}	–	–	ns	
Clock low time	t_8 SR	0.35 x t_{6min}	–	–	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	–	–	ns	
Hold time	t_{10} SR	0	–	–	ns	

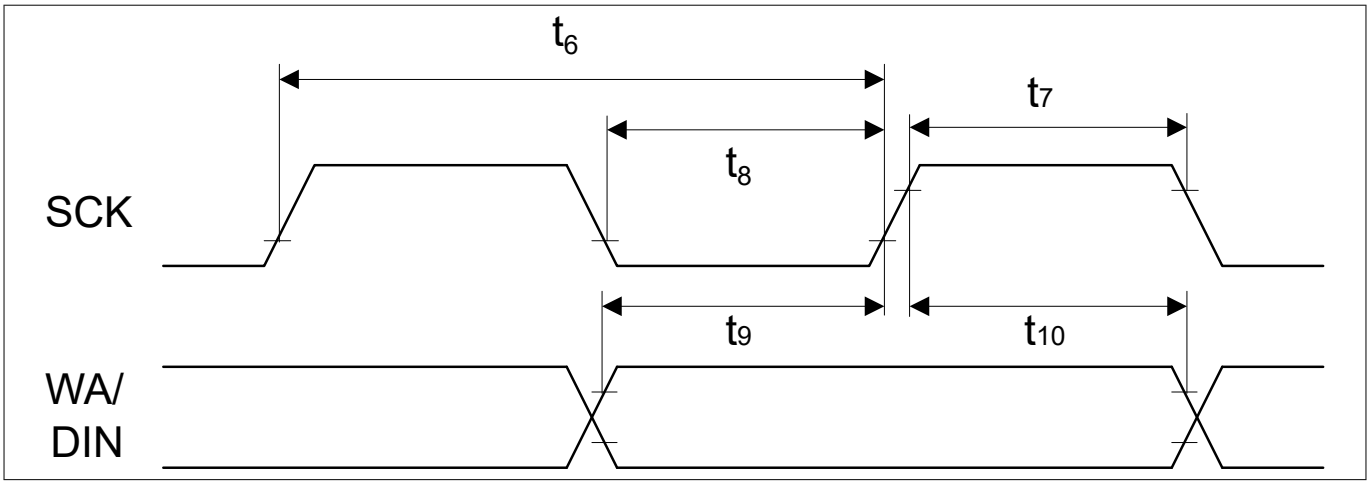

Figure 29 USIC IIS Slave Receiver Timing

3.3.8.4 SDMMC Interface Timing

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

***Note**: Operating Conditions apply, total external capacitive load C_L = 40 pF.*

AC Timing Specifications (Full-Speed Mode)

Table 49 SDMMC Timing for Full-Speed Mode

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Clock frequency in full speed transfer mode (1/t_{pp})	f_{pp} CC	0	24	MHz	
Clock cycle in full speed transfer mode	t_{pp} CC	40	–	ns	
Clock low time	t_{WL} CC	10	–	ns	
Clock high time	t_{WH} CC	10	–	ns	
Clock rise time	t_{TLH} CC	–	10	ns	
Clock fall time	t_{THL} CC	–	10	ns	
Inputs setup to clock rising edge	t_{ISU_F} SR	2	–	ns	
Inputs hold after clock rising edge	t_{IH_F} SR	2	–	ns	
Outputs valid time in full speed mode	t_{ODLY_F} CC	–	10	ns	
Outputs hold time in full speed mode	t_{OH_F} CC	0	–	ns	

Table 50 SD Card Bus Timing for Full-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	5	–	ns	
SD card input hold time	t_{IH}	5	–	ns	
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	0	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

Full-Speed Output Path (Write)

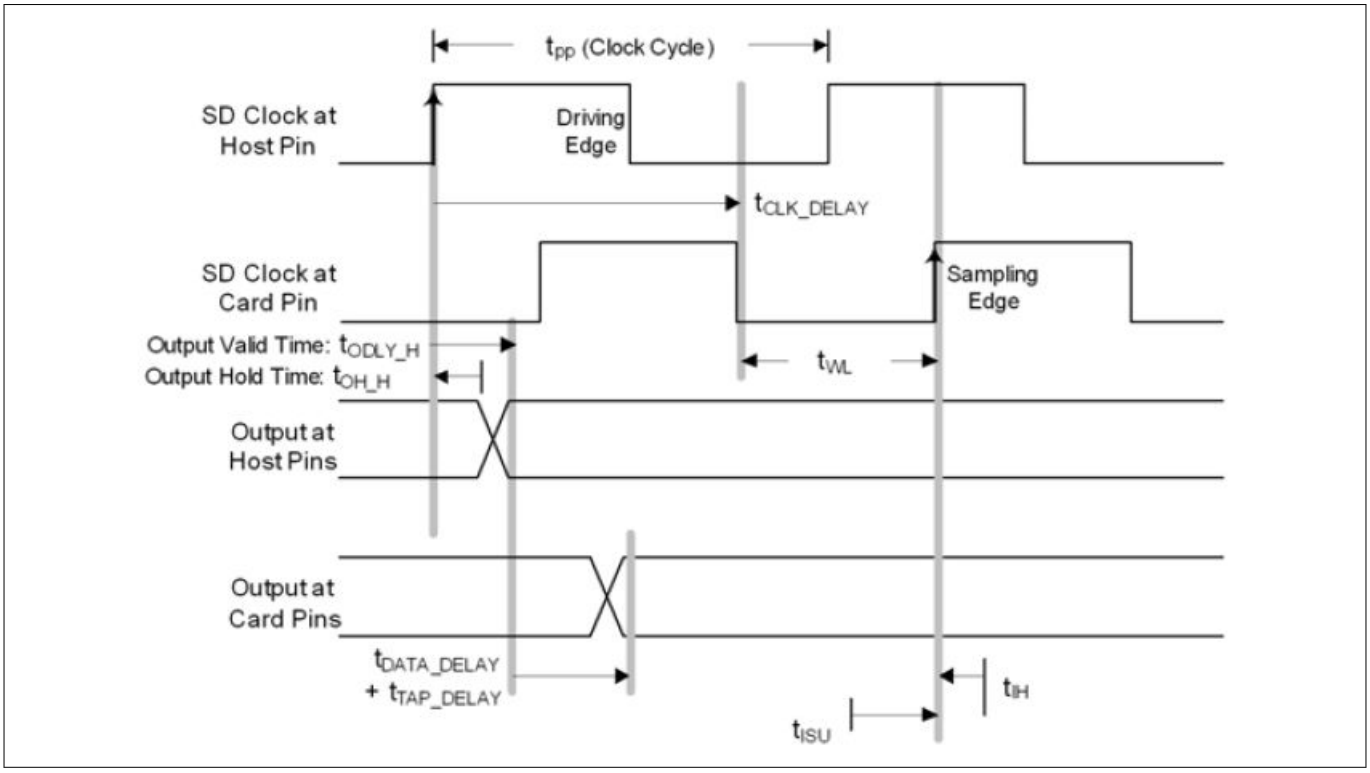

Figure 30 Full-Speed Output Path

Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} \quad (1)$$

With clock delay:

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY} \quad (2)$$

$$\begin{aligned} t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{WL} &< t_{PP} + t_{CLK\_DELAY} - t_{ISU} - t_{ODLY\_F} \\ t_{DATA\_DELAY} + t_{TAP\_DELAY} + 20 &< 40 + t_{CLK\_DELAY} - 5 - 10 \\ t_{DATA\_DELAY} &< 5 + t_{CLK\_DELAY} - t_{TAP\_DELAY} \end{aligned} \quad (3)$$

The data can be delayed versus clock up to 5 ns in ideal case of t_{WL}= 20 ns.

Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned} t_{CLK\_DELAY} &< t_{WL} + t_{OH\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH} \\ t_{CLK\_DELAY} &< 20 + t_{DATA\_DELAY} + t_{TAP\_DELAY} - 5 \\ t_{DATA\_DELAY} &< 15 + t_{CLK\_DELAY} + t_{TAP\_DELAY} \end{aligned} \quad (4)$$

The clock can be delayed versus data up to 18.2 ns (external delay line) in ideal case of t_{WL}= 20 ns, with maximum t_{TAP_DELAY} = 3.2 ns programmed.

Full-Speed Input Path (Read)

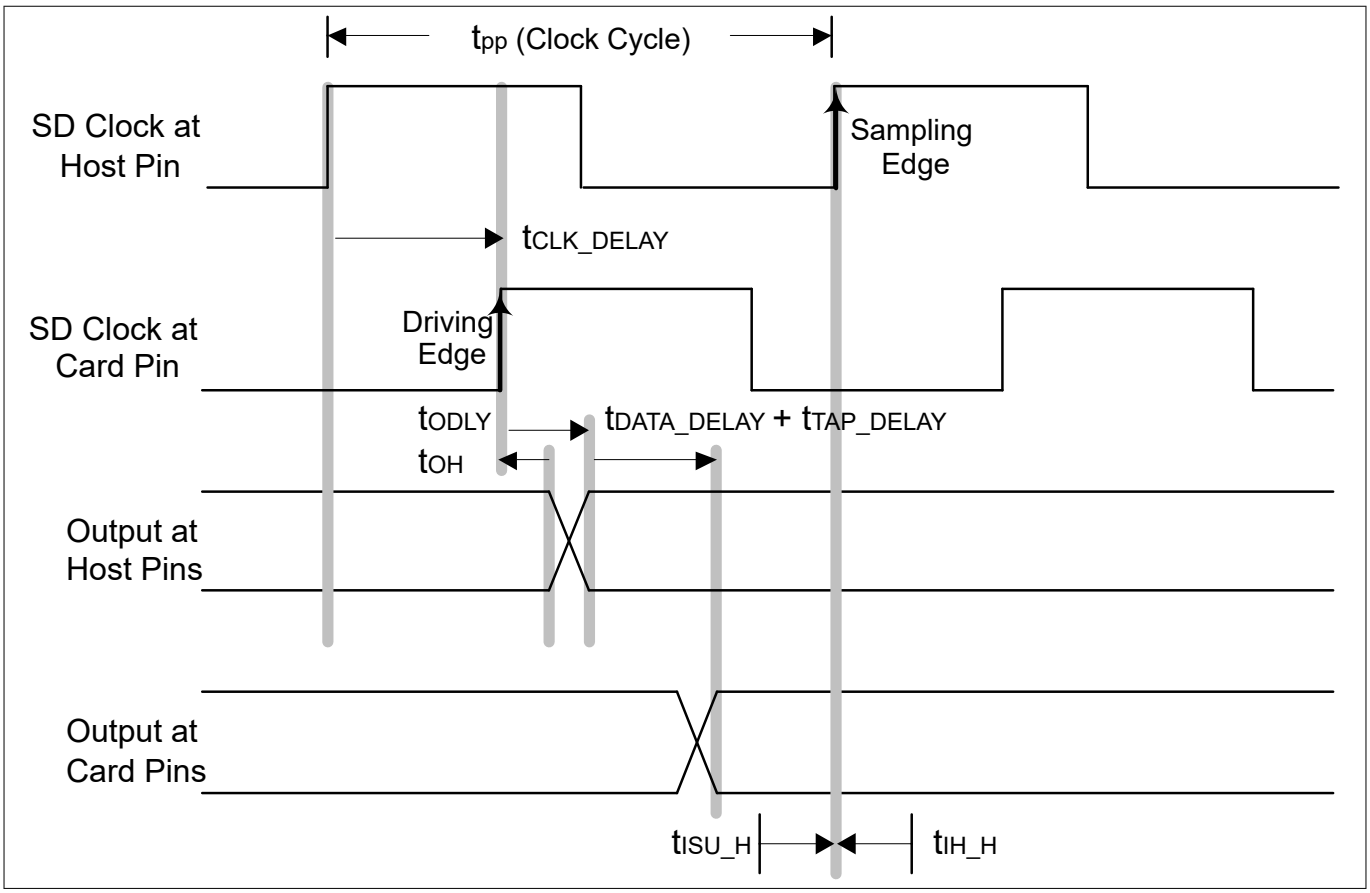

Figure 31 Full-Speed Input Path

Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned} &t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ODLY} + t_{ISU\_F} < 0.5 \times t_{pp} \\ &t_{CLK\_DELAY} + t_{DATA\_DELAY} < 0.5 \times t_{pp} - t_{ODLY} - t_{ISU\_F} - t_{TAP\_DELAY} \\ &t_{CLK\_DELAY} + t_{DATA\_DELAY} < 20 - 14 - 2 - t_{TAP\_DELAY} \\ &t_{CLK\_DELAY} + t_{DATA\_DELAY} < 4 - t_{TAP\_DELAY} \end{aligned} \quad (5)$$

The data + clock delay can be up to 4 ns for a 40 ns clock cycle.

Full-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned} &t_{CLK\_DELAY} + t_{OH} + t_{DATA\_DELAY} + t_{TAP\_DELAY} > t_{IH\_F} \\ &t_{CLK\_DELAY} + t_{DATA\_DELAY} > t_{IH\_F} - t_{OH} - t_{TAP\_DELAY} \\ &t_{CLK\_DELAY} + t_{DATA\_DELAY} > 2 - t_{TAP\_DELAY} \end{aligned} \quad (6)$$

The data + clock delay must be greater than 2 ns if t_{TAP_DELAY} is not used.
If the t_{TAP_DELAY} is programmed to at least 2 ns, the data + clock delay must be greater than 0 ns (or less). This is always fulfilled.

AC Timing Specifications (High-Speed Mode)

Table 51 SDMMC Timing for High-Speed Mode

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
Clock frequency in high speed transfer mode ($1/t_{pp}$)	f_{pp} CC	0	48	MHz	
Clock cycle in high speed transfer mode	t_{pp} CC	20	–	ns	
Clock low time	t_{WL} CC	7	–	ns	
Clock high time	t_{WH} CC	7	–	ns	
Clock rise time	t_{TLH} CC	–	3	ns	
Clock fall time	t_{THL} CC	–	3	ns	
Inputs setup to clock rising edge	t_{ISU_H} SR	2	–	ns	
Inputs hold after clock rising edge	t_{IH_H} SR	2	–	ns	
Outputs valid time in high speed mode	t_{ODLY_H} CC	–	14	ns	
Outputs hold time in high speed mode	t_{OH_H} CC	2	–	ns	

Table 52 SD Card Bus Timing for High-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	6	–	ns	

(table continues...)

Table 52 (continued) SD Card Bus Timing for High-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/Test Condition
		Min.	Max.		
SD card input hold time	t_{IH}	2	–	ns	
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	2.5	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

High-Speed Output Path (Write)

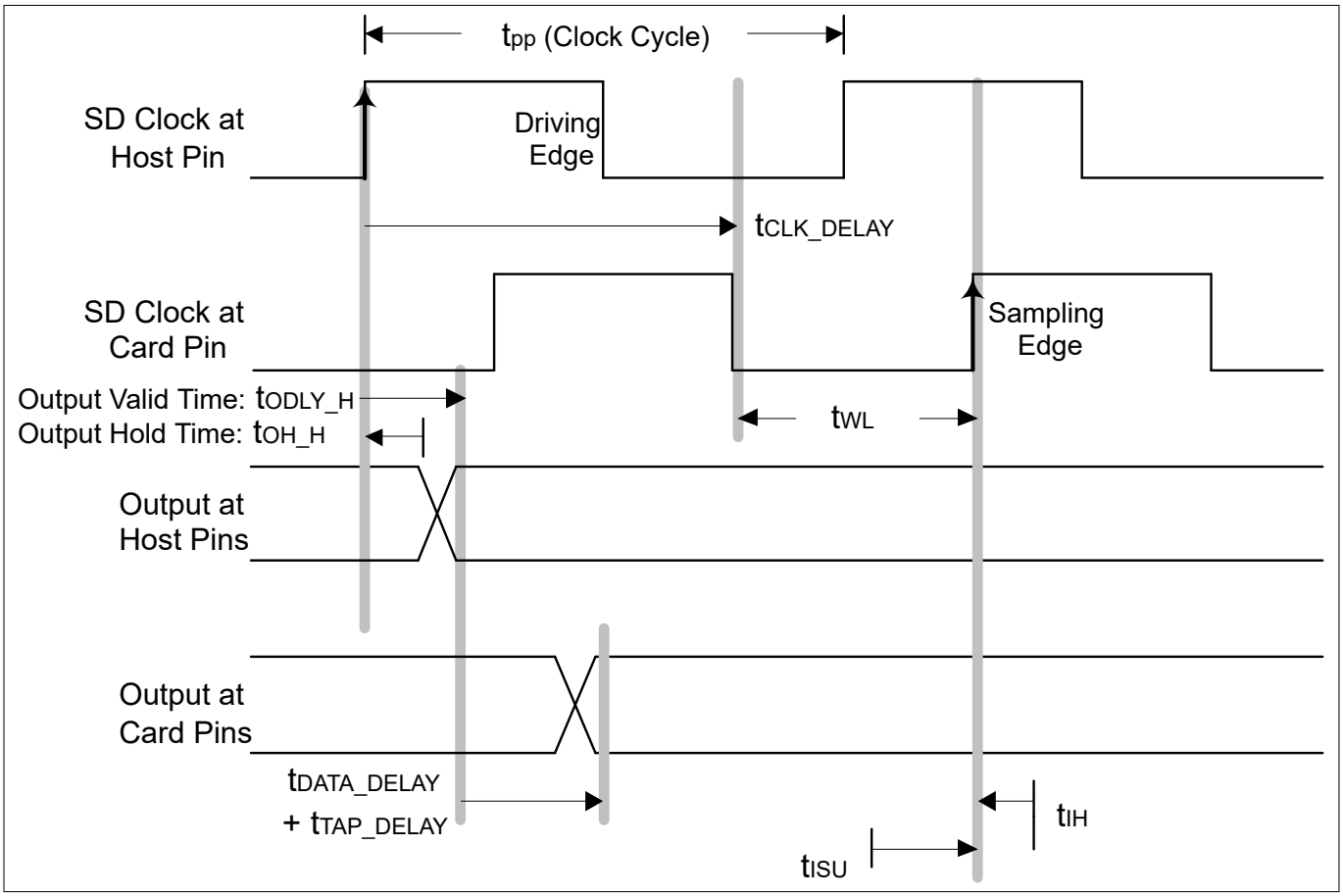

Figure 32 High-Speed Output Path

High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{ODLY\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} \quad (7)$$

With clock delay:

$$t_{ODLY\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY} \quad (8)$$

$$\begin{aligned} t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{CLK\_DELAY} &< t_{WL} - t_{ISU} - t_{ODLY\_H} \\ t_{DATA\_DELAY} - t_{CLK\_DELAY} &< t_{WL} - t_{ISU} - t_{ODLY\_H} - t_{TAP\_DELAY} \\ t_{DATA\_DELAY} - t_{CLK\_DELAY} &< 10 - 6 - 14 - t_{TAP\_DELAY} \\ t_{DATA\_DELAY} - t_{CLK\_DELAY} &< -10 - t_{TAP\_DELAY} \end{aligned} \quad (9)$$

The data delay is less than the clock delay by at least 10 ns in the ideal case where t_{WL}= 10 ns.

High-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned} t_{CLK\_DELAY} &< t_{WL} + t_{OH\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH} \\ t_{CLK\_DELAY} - t_{DATA\_DELAY} &< t_{WL} + t_{OH\_H} + t_{TAP\_DELAY} - t_{IH} \\ t_{CLK\_DELAY} - t_{DATA\_DELAY} &< 10 + 2 + t_{TAP\_DELAY} - 2 \\ t_{CLK\_DELAY} - t_{DATA\_DELAY} &< 10 + t_{TAP\_DELAY} \end{aligned} \quad (10)$$

The clock can be delayed versus data up to 13.2 ns (external delay line) in ideal case of t_{WL}= 10 ns, with maximum t_{TAP_DELAY} = 3.2 ns programmed.

High-Speed Input Path (Read)

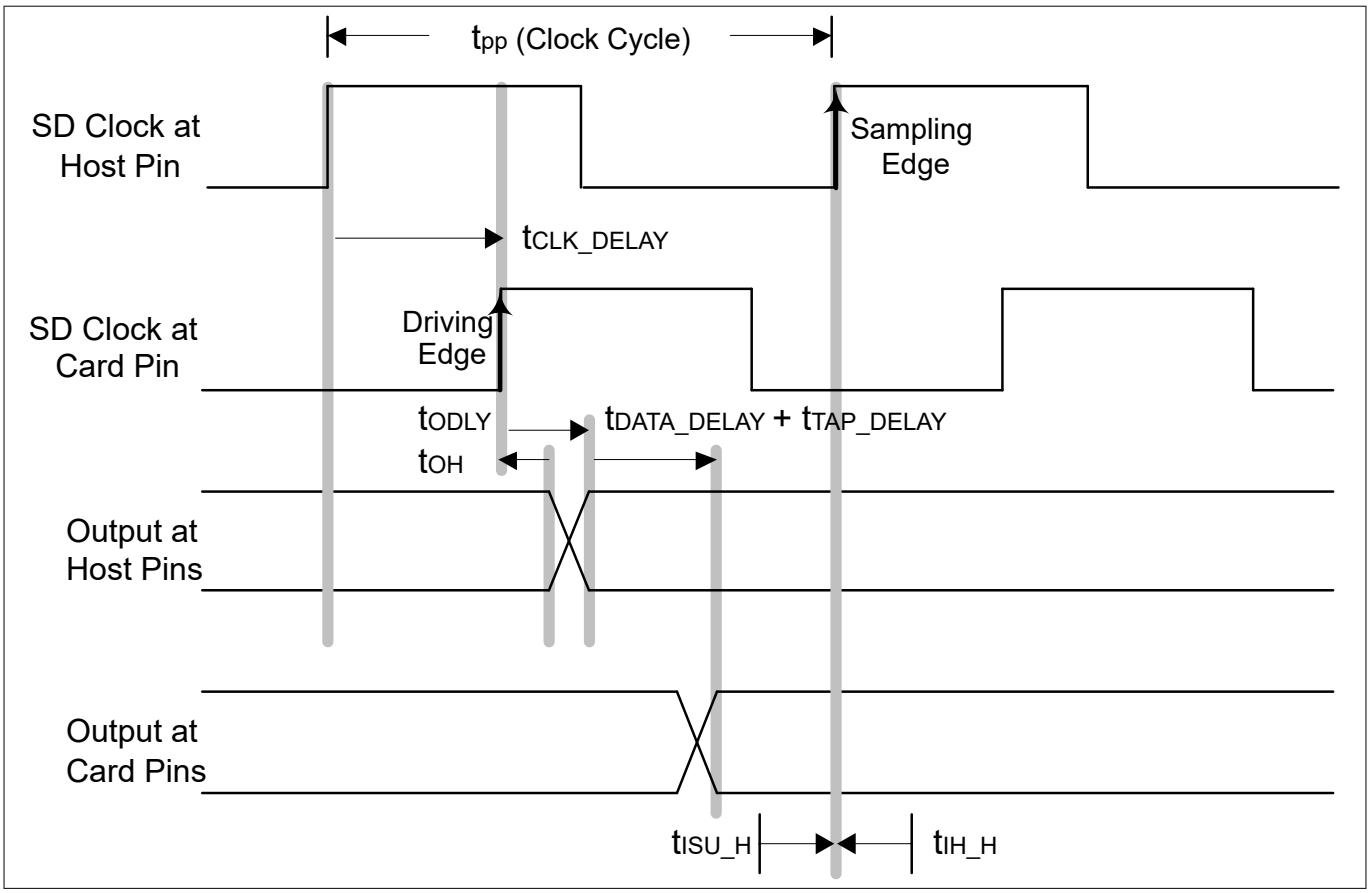

Figure 33 High-Speed Input Path

High-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned} t_{\text{CLK\_DELAY}} + t_{\text{DATA\_DELAY}} + t_{\text{TAP\_DELAY}} + t_{\text{ODLY}} + t_{\text{ISU\_H}} &< t_{\text{pp}} \\ t_{\text{CLK\_DELAY}} + t_{\text{DATA\_DELAY}} &< t_{\text{pp}} - t_{\text{ODLY}} - t_{\text{ISU\_H}} - t_{\text{TAP\_DELAY}} \\ t_{\text{CLK\_DELAY}} + t_{\text{DATA\_DELAY}} &< 20 - 14 - 2 - t_{\text{TAP\_DELAY}} \\ t_{\text{CLK\_DELAY}} + t_{\text{DATA\_DELAY}} &< 4 - t_{\text{TAP\_DELAY}} \end{aligned} \tag{11}$$

The data + clock delay can be up to 4 ns for a 20 ns clock cycle.

High-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

$$\begin{aligned} t_{\text{CLK\_DELAY}} + t_{\text{OH}} + t_{\text{DATA\_DELAY}} + t_{\text{TAP\_DELAY}} &> t_{\text{IH\_H}} \\ t_{\text{CLK\_DELAY}} + t_{\text{DATA\_DELAY}} &> t_{\text{IH\_H}} - t_{\text{OH}} - t_{\text{TAP\_DELAY}} \\ t_{\text{CLK\_DELAY}} + t_{\text{DATA\_DELAY}} &> 2 - 2.5 - t_{\text{TAP\_DELAY}} \\ t_{\text{CLK\_DELAY}} + t_{\text{DATA\_DELAY}} &> -0.5 - t_{\text{TAP\_DELAY}} \end{aligned} \tag{12}$$

The data + clock delay must be greater than -0.5 ns for a 20 ns clock cycle. This is always fulfilled.

3.3.9 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 53 USB Timing Parameters (operating conditions apply)

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Rise time	t_R CC	4	–	20	ns	C_L = 50 pF
Fall time	t_F CC	4	–	20	ns	C_L = 50 pF
Rise/Fall time matching	t_R/t_F CC	90	–	111.11	%	C_L = 50 pF
Crossover voltage	V_{CRS} CC	1.3	–	2.0	V	C_L = 50 pF

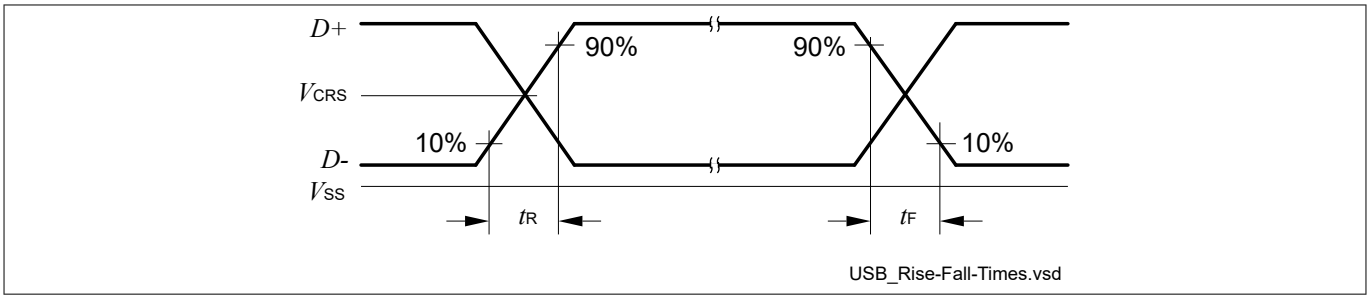

Figure 34 USB Signal Timing

3.3.10 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

***Note**: These parameters are not subject to production test, but verified by design and/or characterization.*

3.3.10.1 ETH Measurement Reference Points

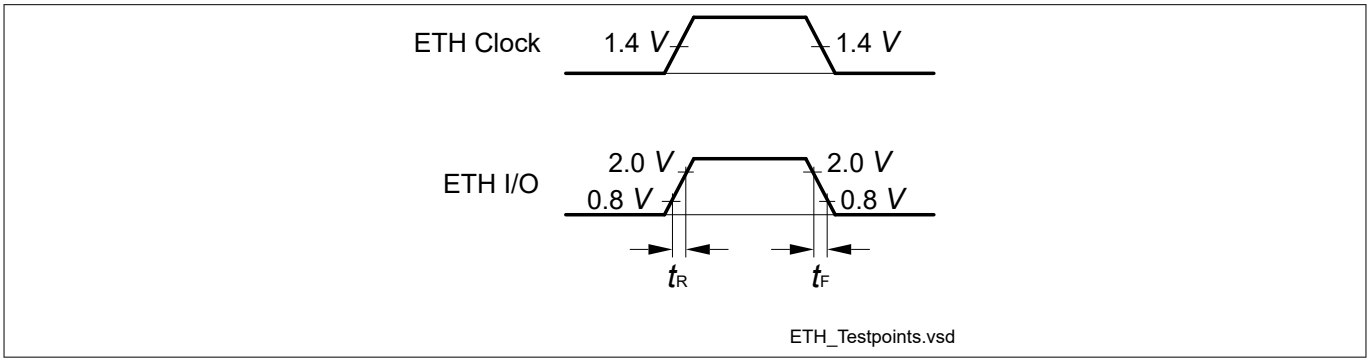

Figure 35 ETH Measurement Reference Points

3.3.10.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 54 ETH Management Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
ETH_MDC period	t_1 CC	400	–	–	ns	C_L = 25 pF
ETH_MDC high time	t_2 CC	160	–	–	ns	
ETH_MDC low time	t_3 CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4 CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5 CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6 SR	0	–	300	ns	

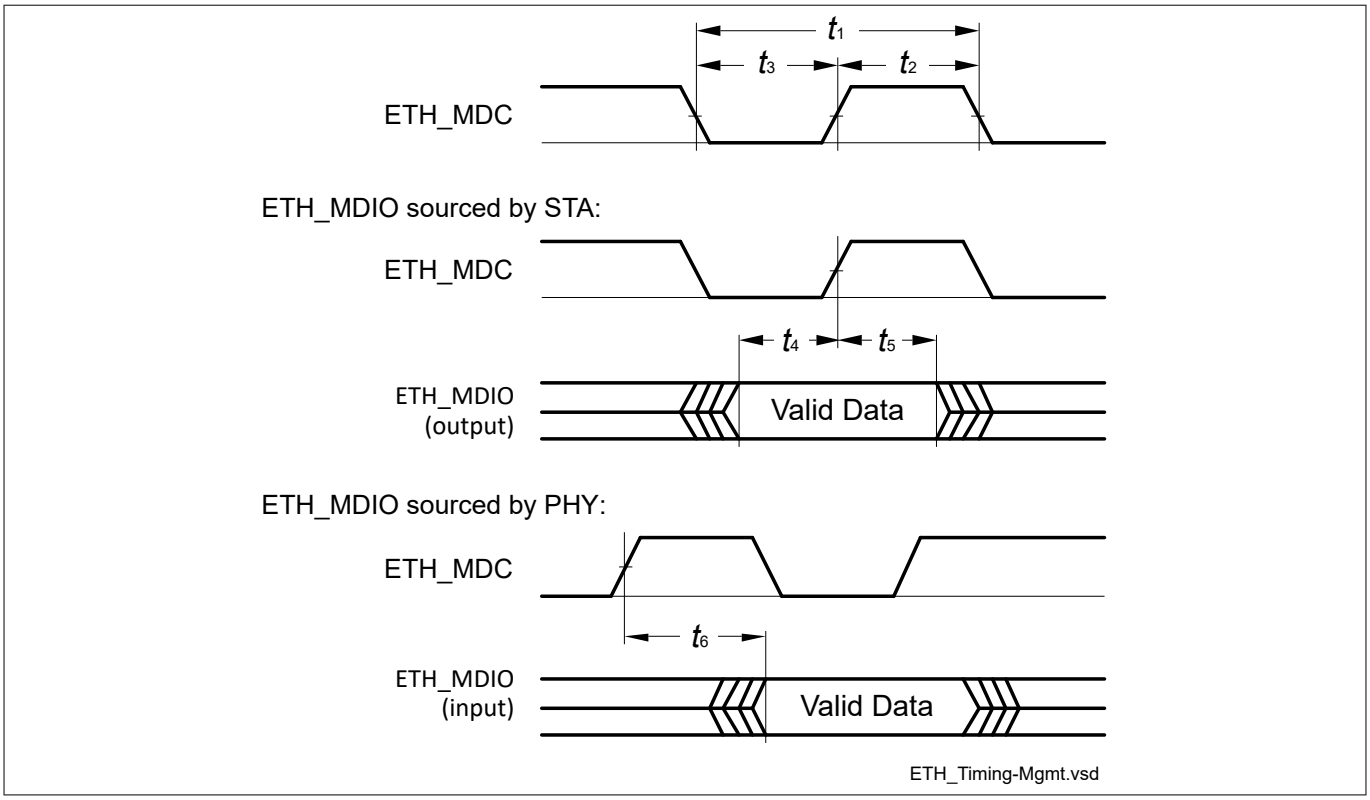

Figure 36 ETH Management Signal Timing

3.3.10.3 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 55 ETH RMII Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13} SR	20	–	–	ns	C_L = 25 pF; 50 ppm
ETH_RMII_REF_CL clock high time	t_{14} SR	7	–	13	ns	C_L = 25 pF
ETH_RMII_REF_CL clock low time	t_{15} SR	7	–	13	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time	t_{16} SR	4	–	–	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time	t_{17} SR	2	–	–	ns	
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18} CC	4	–	15	ns	

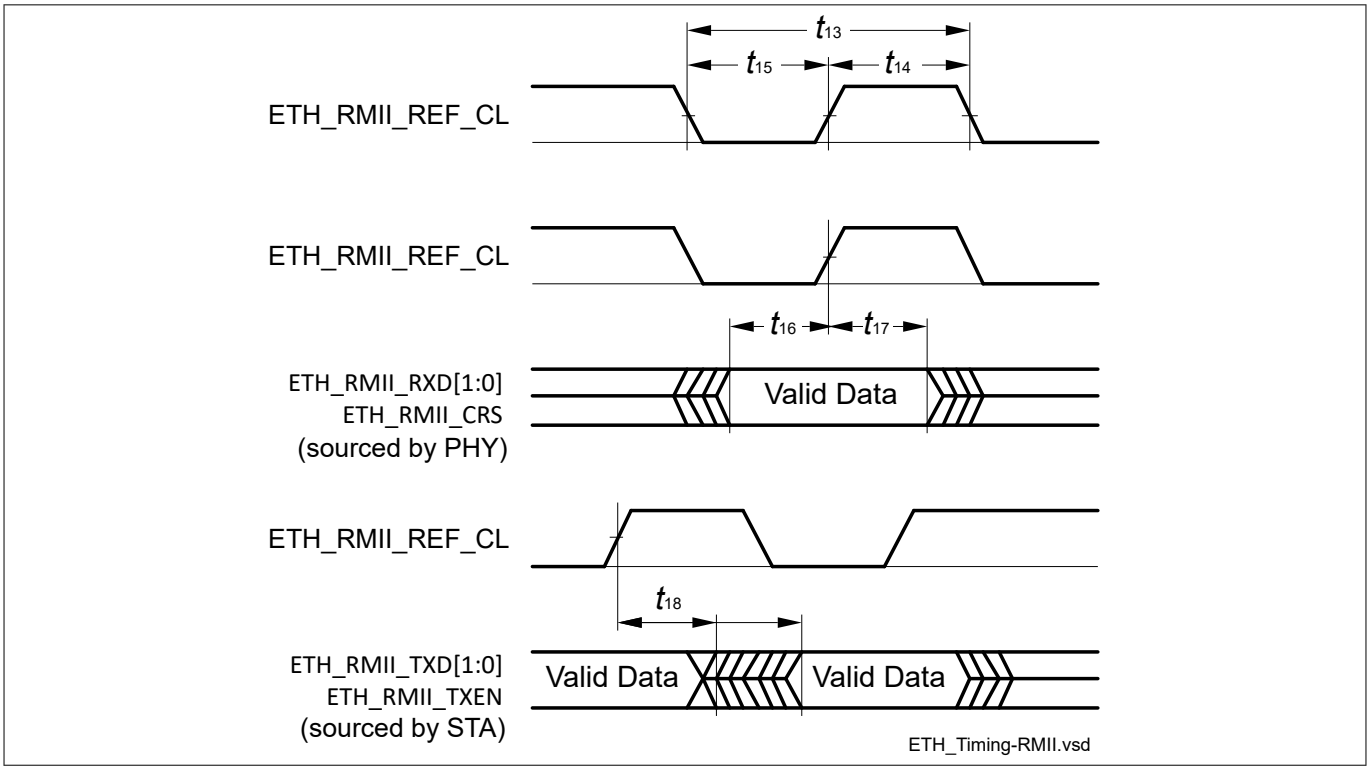

Figure 37 ETH RMII Signal Timing

3.3.11 EtherCAT (ECAT) Characteristics

3.3.11.1 ECAT Measurement Reference Points

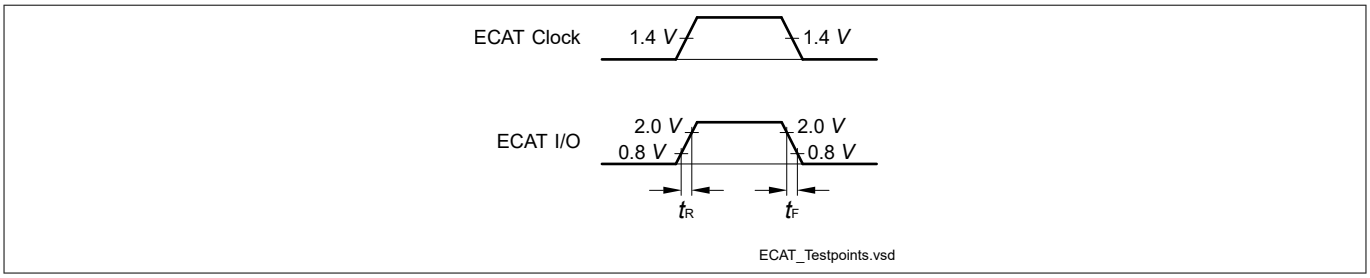

Figure 38 Measurement Reference Points

3.3.11.2 ETH Management Signal Parameters (MCLK, MDIO)

Table 56 ECAT Management Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
ECAT_MCLK period	t_{MCLK} CC	–	400	–	ns	IEEE802.3 requirement (2.5 MHz) C_L = 25 pF
ECAT_MCLK high time	t_{MCLK_h} CC	160	–	–	ns	
ECAT_MCLK low time	t_{MCLK_l} CC	160	–	–	ns	
ECAT_MDIO setup time (output)	t_{D_setup} CC	10	–	–	ns	
ECAT_MDIO hold time (output)	t_{D_hold} CC	10	–	–	ns	
ECAT_MDIO data valid (input)	t_{D_valid} SR	0	–	300	ns	

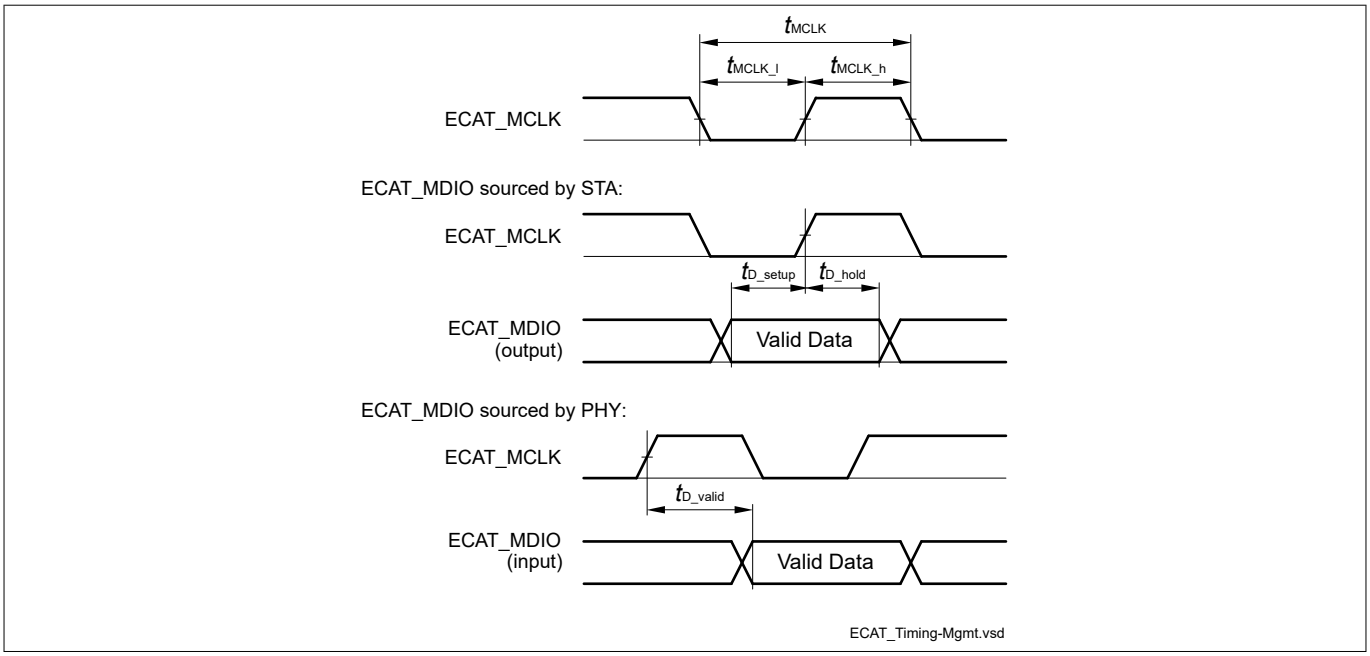

Figure 39 ECAT Management Signal Timing

3.3.11.3 MII Timing TX Characteristics

Table 57 ETH MII TX Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
PHY_CLK25, TX_CLK period	t_{TX_CLK} SR	–	40	–	ns	
Delay between PHY clock source PHY_CLK25 and TX_CLK output of the PHY	t_{PHY_delay} SR	–	–	–	ns	PHY dependent
PHY setup requirement: TXEN/TXD[3:0] with respect to TX_CLK	t_{TX_setup} SR	15	–	0	ns	PHY dependent IEEE802.3 limit is 15 ns
PHY hold requirement: TXEN/TXD[3:0] with respect to TX_CLK	t_{TX_hold} CC	0	–	25	ns	PHY dependent IEEE802.3 limit is 0 ns

***Note**: ECAT0_CONPx.TX_SHIFT can be adjusted by displaying TX_CLK of a PHY and TXEN/TXD[3:0] on an oscilloscope. TXEN/TXD[3:0] is allowed to change between 0 ns and 25 ns after a rising edge of TX_CLK (according to IEEE802.3 – check your PHY's documentation). Configure TX_SHIFT so that TXEN/TXD[3:0] change near the middle of this range. It is sufficient to check just one of the TXEN/TXD[3:0] signals, because they are nearly generated at the same time.*

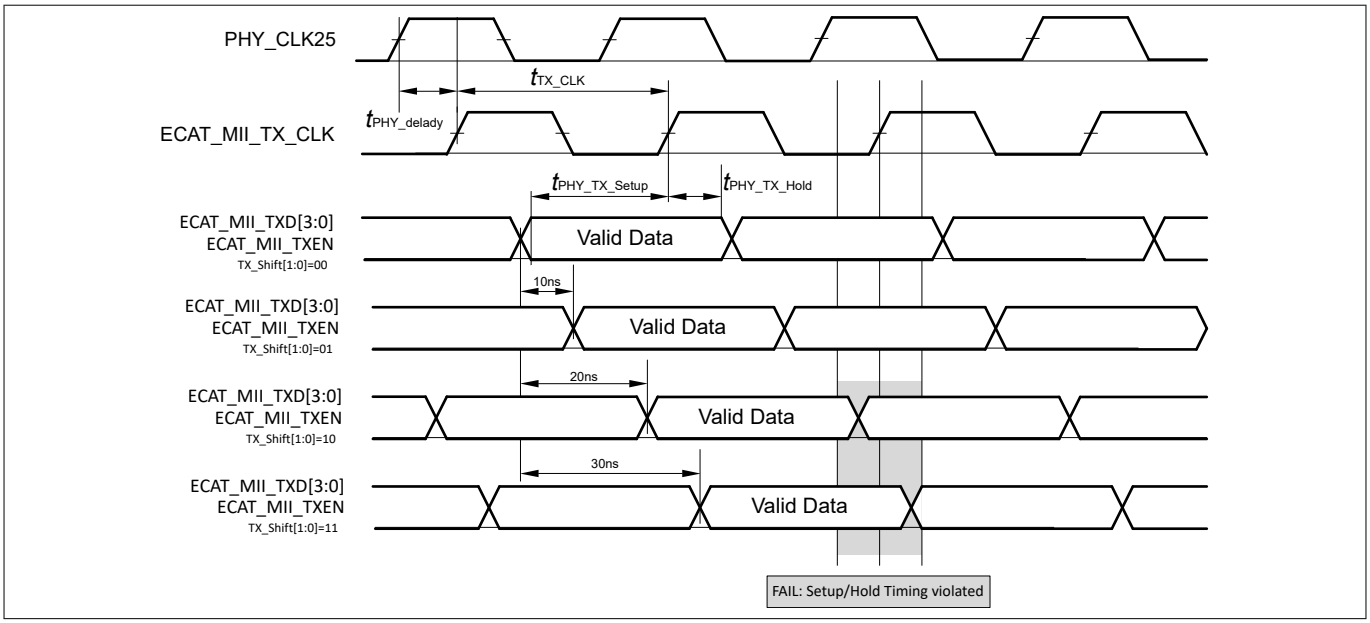

Figure 40 MII TX Characteristics

3.3.11.4 MII Timing RX Characteristics

Table 58 ETH MII RX Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
RX_CLK period	t_{RX_CLK} SR	–	40	–	ns	C_L = 25 pF, IEEE802.3 requirement
RX_DV/RX_DV/RXD[3:0] valid before rising edge of RX_CLK	t_{RX_setup} SR	10	–	–	ns	
RX_DV/RX_DV/RXD[3:0] valid after rising edge of RX_CLK	t_{RX_hold} SR	10	–	–	ns	

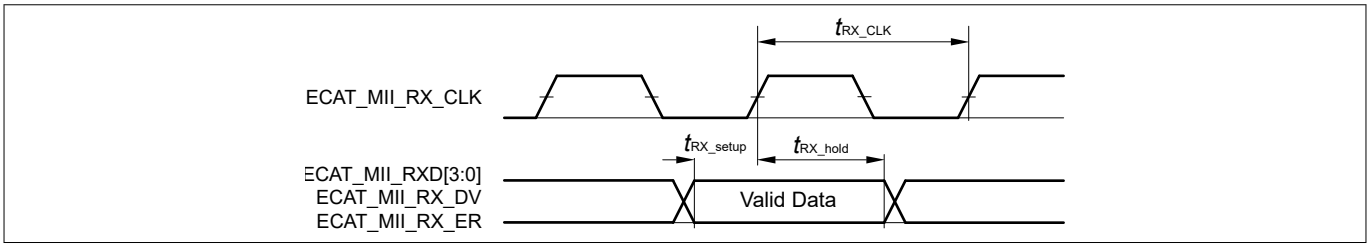

Figure 41 MII RX characteristics

3.3.11.5 Sync/Latch Timings

Table 59 Sync/Latch Timings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
SYNC0/1	$t_{DC\_SYNC\_Jitter}$ SR	–	–	11 + m[1)]	ns	
LATCH0/1	t_{DC_LATCH} SR	12 + n[2)]	–	–	ns	

1) additional delay form logic and pad, number is added after characterization
2) additional shaping delay, number is added after characterization

***Note**: SYNC0/1 pulse length are initially loaded by EEPROM content ADR 0x0002. The actual used value can be read back from Register DC_PULSE_LEN.*

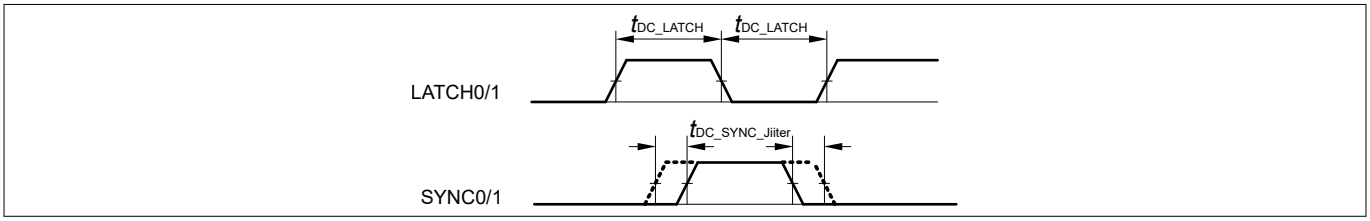

Figure 42 Sync/Latch Timings

4 Package and Reliability

The XMC4300 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 60 provides the thermal characteristics of the packages used in XMC4300.

Table 60 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad dimensions including U-Groove	Ex × Ey CC	–	7.0 × 7.0	mm	PG-LQFP-100-25
Exposed Die Pad dimensions excluding U-Groove	Ax × Ay CC	–	6.2 × 6.2	mm	PG-LQFP-100-25
Exposed Die Pad dimensions	–	–	7.0 × 7.0	mm	PG-LQFP-100-29
Thermal resistance Junction-Ambient $T_J \le 150°C$	$R_{\Theta JA}$ CC	–	22.5	K/W	PG-LQFP-100-25[1)] PG-LQFP-100-29[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

***Note**: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS}, independent of EMC and thermal requirements.*

4.1.1 Thermal Considerations

When operating the XMC4300 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150°C.

The difference between junction temperature and ambient temperature is determined by

$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as

$P_{IOSTAT} = \Sigma((V_{DDP}\text{-}V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

The exposed die pad dimensions are listed in Table 60.

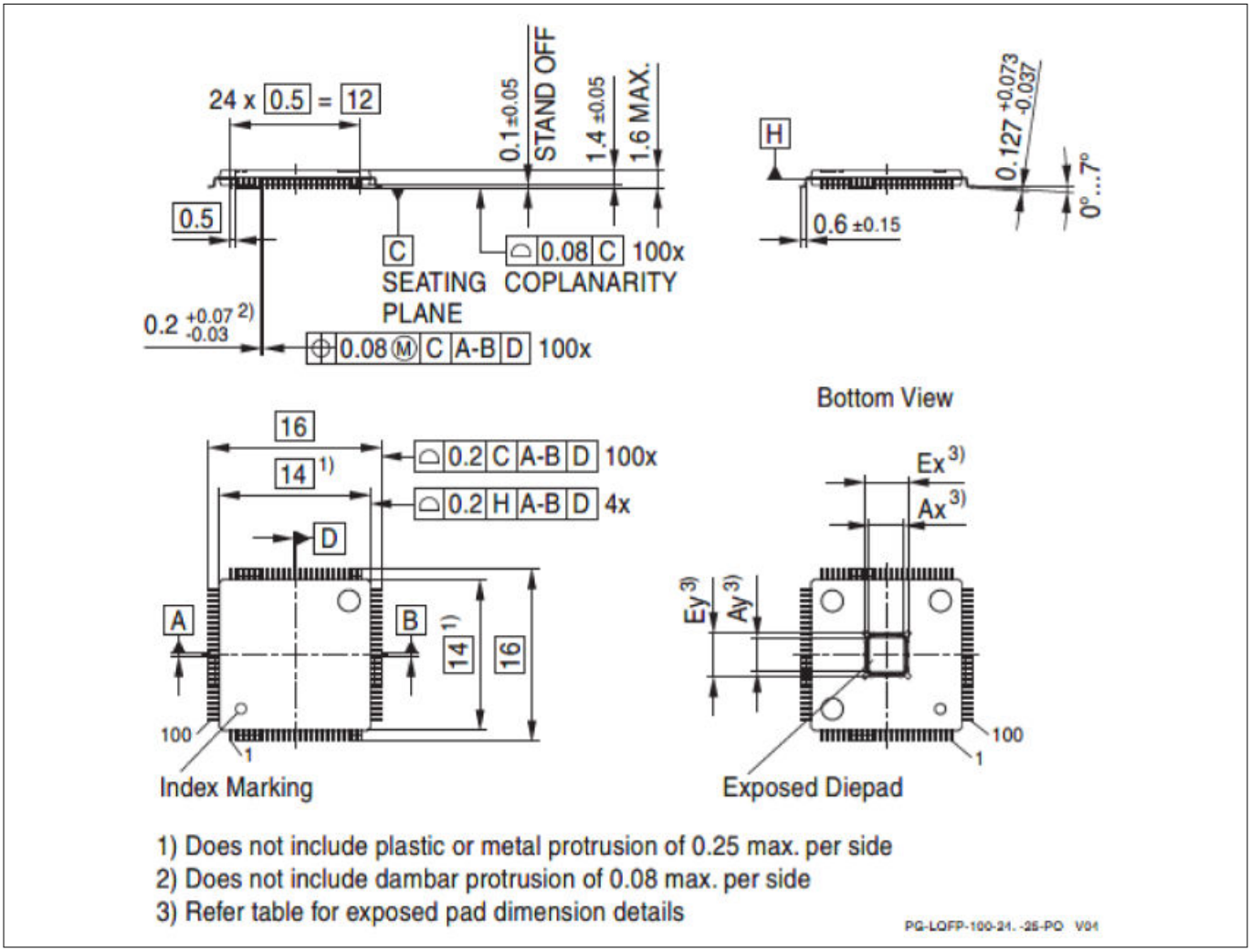

Figure 43 PG-LQFP-100-25 (Plastic Green Low Profile Quad Flat Package)

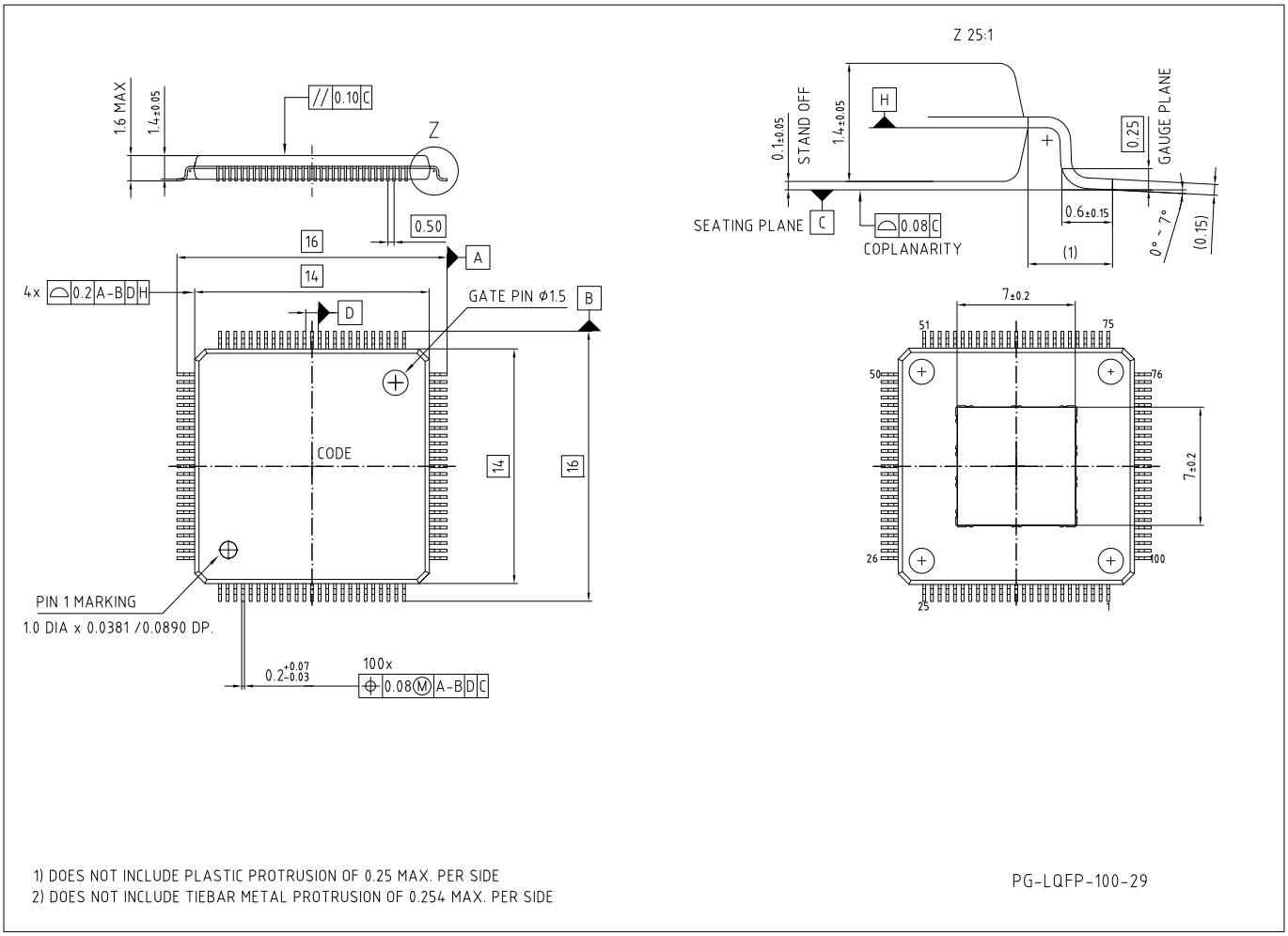

Figure 44 PG-LQFP-100-29 (Plastic Green Low Profile Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: http://www.infineon.com/packages

5 Quality Declarations

The qualification of the XMC4300 is executed according to the JEDEC standard JESD471.

***Note**: For automotive applications refer to the Infineon automotive microcontrollers.*

Table 61 Quality Parameters

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	3000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	1000	V	Conforming to JESD22-C101-C
Moisture sensitivity level	*MSL* CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D

Revision history

Document revision	Date	Description of changes
V1.2	2023-04-01	Summary of Features: Updated number of breakpoints from 8 to 6. Table 60: Added PG-LQFP-100-29 details. Figure 44: Added package diagram: PG-LQFP-100-29.
V1.3	2024-11-25	Template update; no content update

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