更高集成度的家电设计目标带来的散热挑战和解决方案

IPC ISD SYS
2022-03-25

restricted

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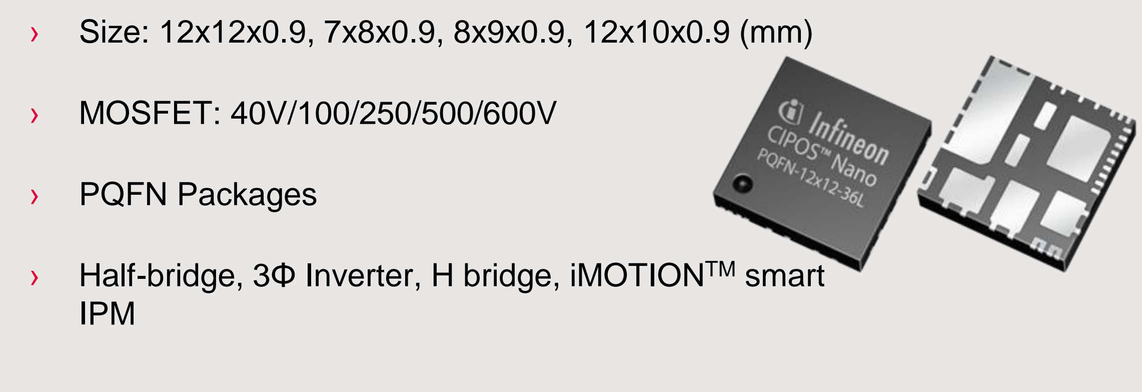
CIPOS™ Nano IPM: PQFN package

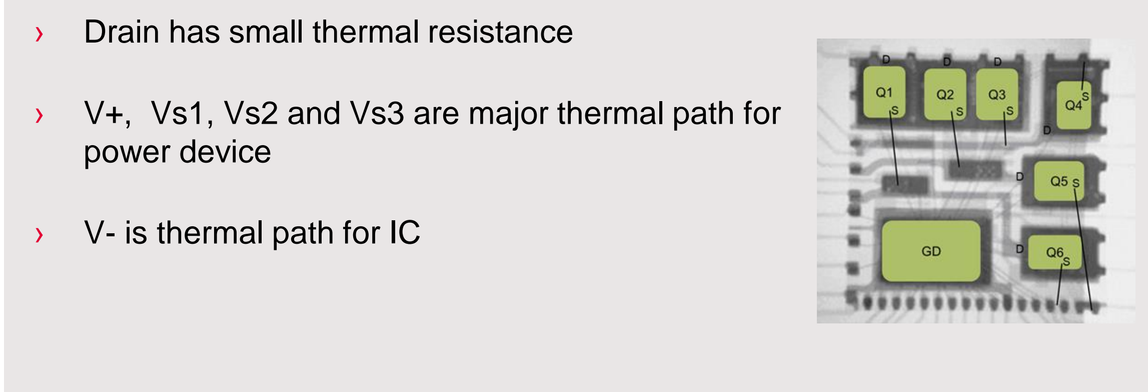
CIPOSTM Nano IPM

- Size: 12x12x0.9, 7x8x0.9, 8x9x0.9, 12x10x0.9 (mm)
- MOSFET: 40V/100/250/500/600V
- PQFN Packages
- Half-bridge, 3Φ Inverter, H bridge, iMOTION™ smart IPM

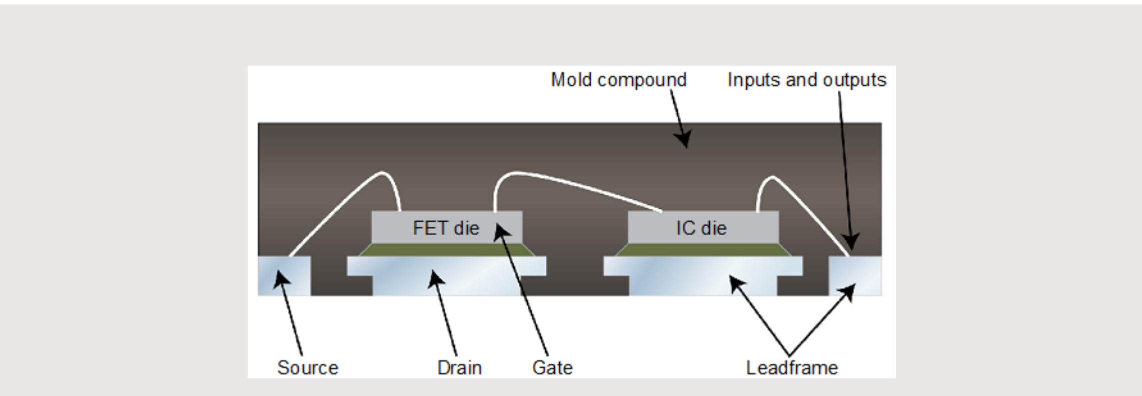


Connection X ray photo

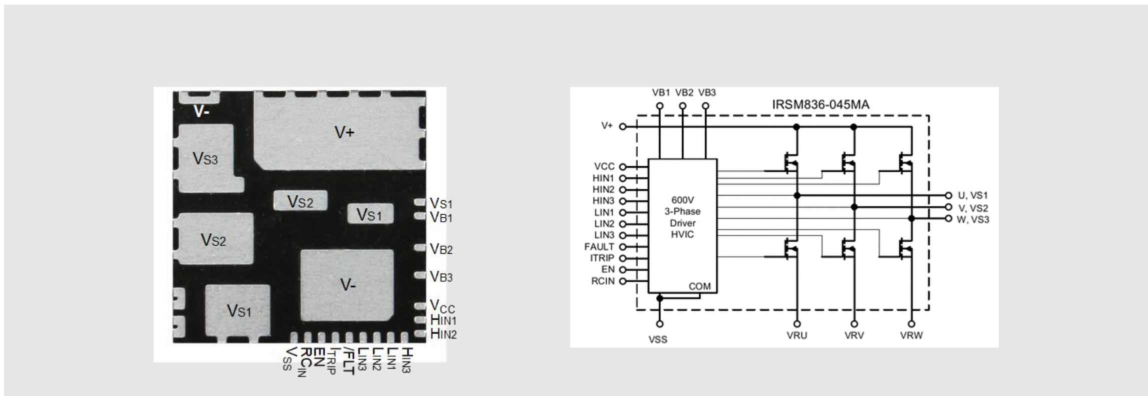
- Drain has small thermal resistance
- V+, Vs1, Vs2 and Vs3 are major thermal path for power device
- V- is thermal path for IC



Sectional view of PQFN package



A sample contact configuration



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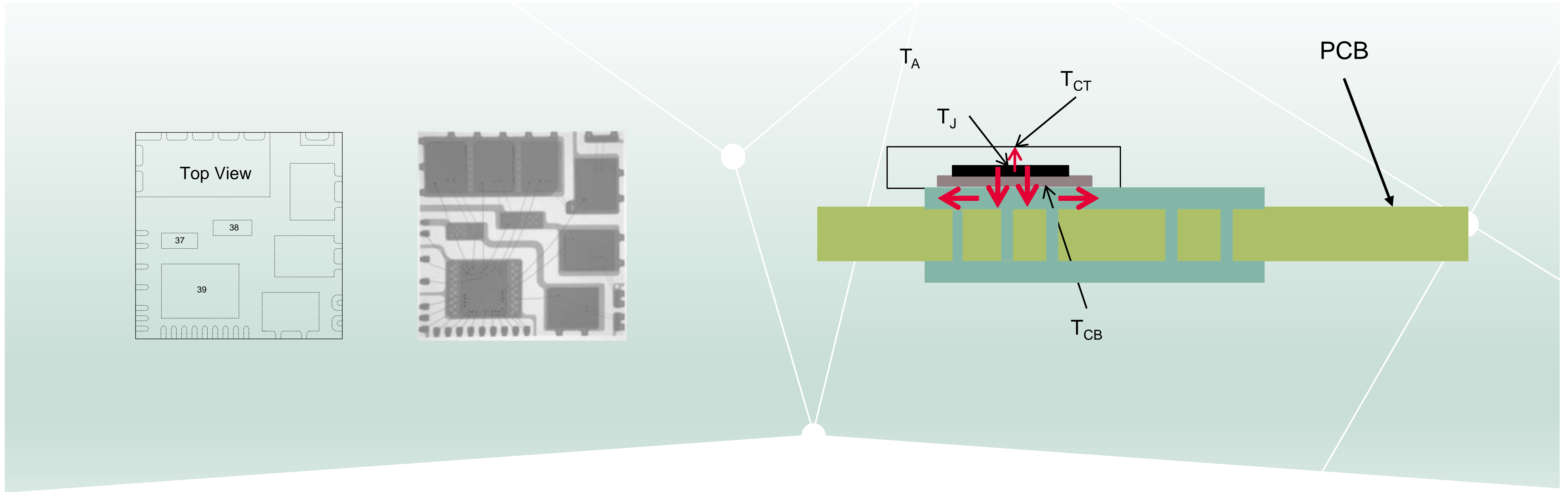
Thermal spread path of PQFN



CIPOS™ Nano IPM is first in the IPM industry to utilize PCB as heat sink: die is bonded to lead frame which is exposed and soldered to PCB

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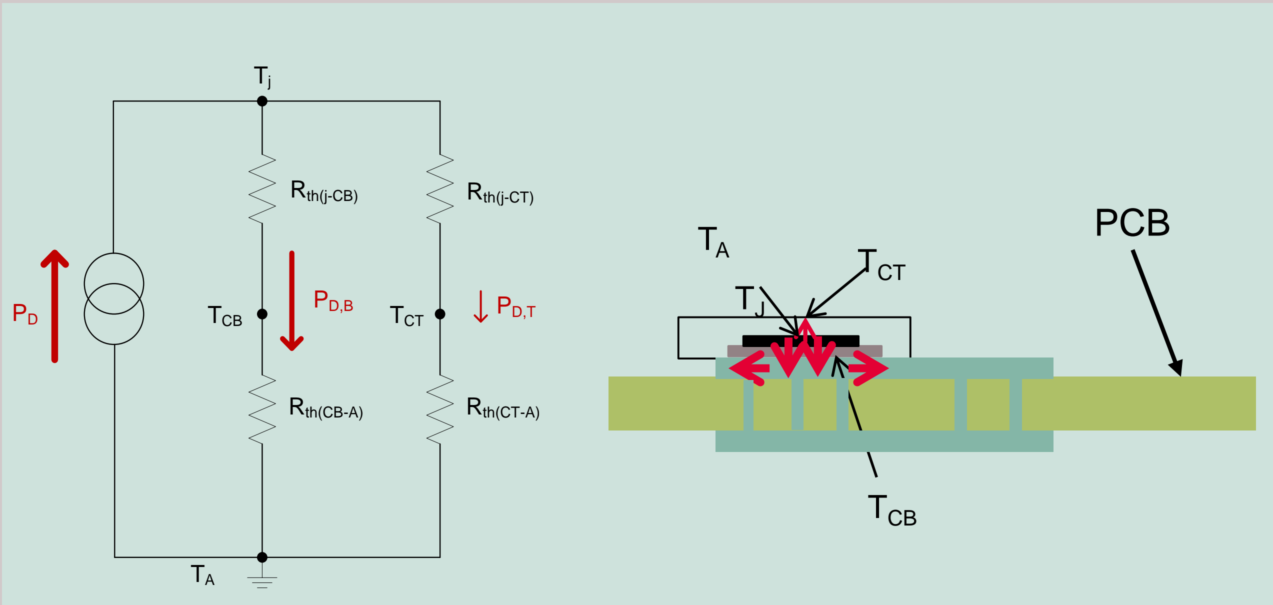
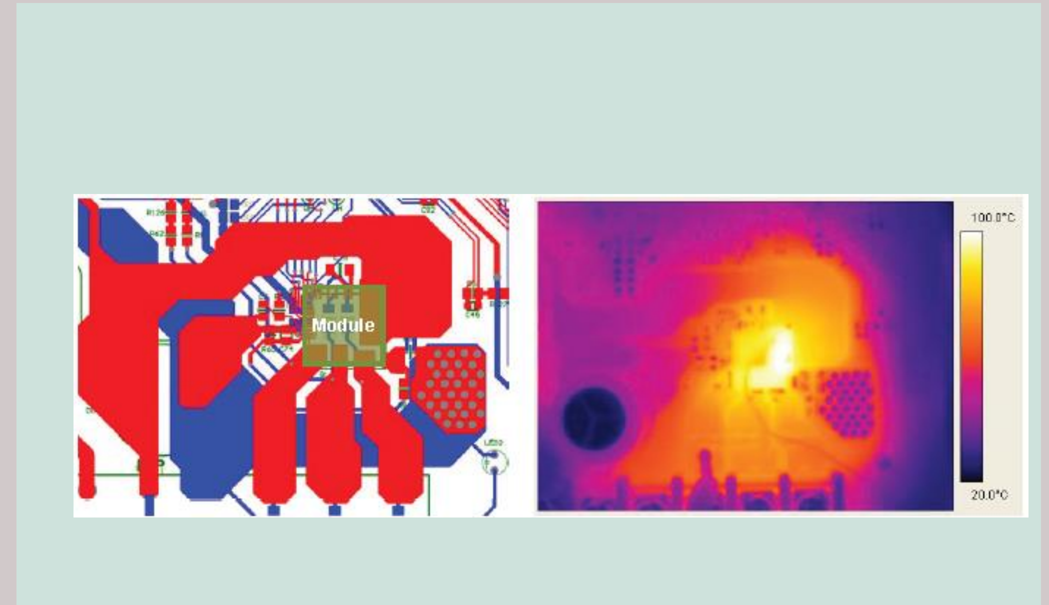
About Temperature





- About thermal resistance
  - $R_{th(j-c)} = (T_j - T_c)/P_D$
- In an application where no heat sink is used:
  - Most of the dissipated heat travels down into the PCB, i.e. $P_{D,B} >> P_{D,T}$
  - Thus, $P_{D,T} \times R_{th(j-CT)} \approx 0$
  - Thus, $T_{CT} \approx T_J$
- T_j is less critical than T_{PCB} i.e junction temperature is unlikely to ever reach limit in steady state operation

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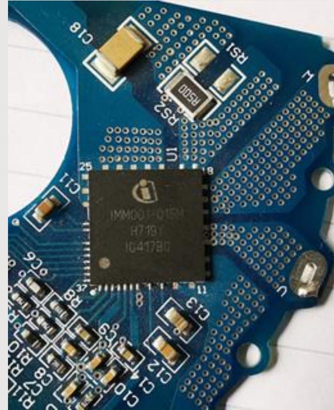
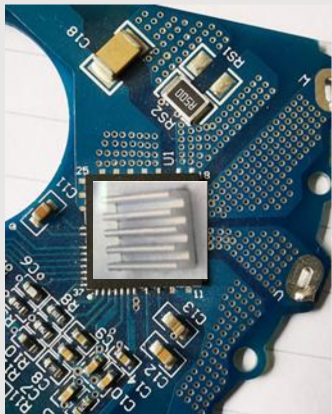
PQFN package heat spread styles

w/o heatsink

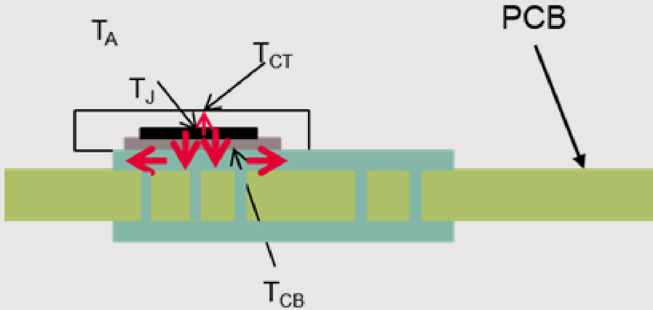


With heatsink



Cooling fan

Thermal model



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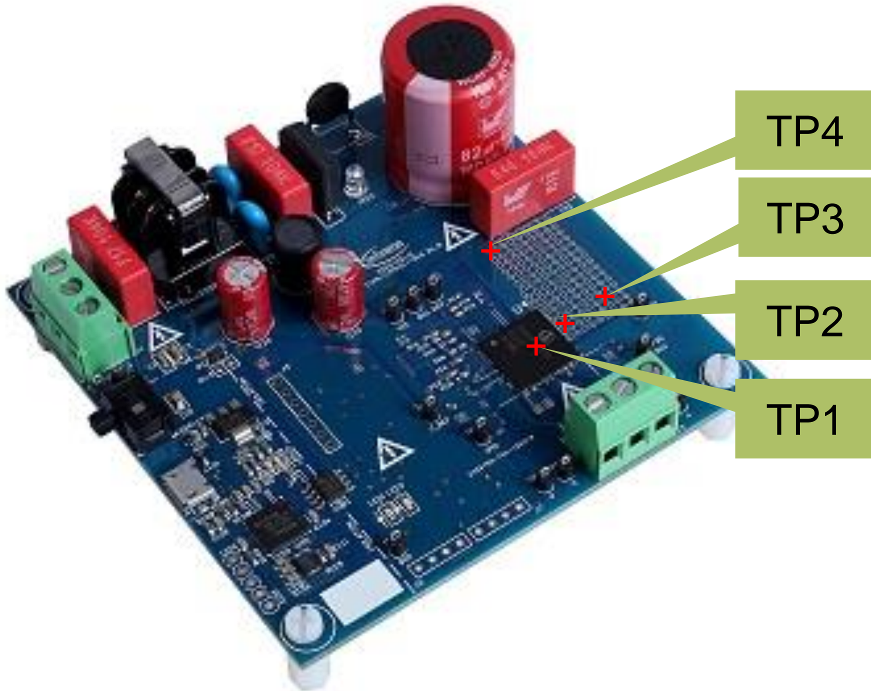
Example : Thermal test data

- Tested with EVAL-IMM101T-015 R1.0 board
- PWM: 10kHz
- Vbus voltage:300Vdc
- Ta: 24 ℃
- Load: fan
- Cooling fan: 12Vdc, 0.11A



IMM101T-015M		Input voltage (VDC)	Input power (W)	Phase current(mA)	Ta(℃)	Case temp (TP1)(℃)	Copper temp (near Vbus pin, (TP2)(℃)	Copper temp (1CM, TP3)(℃)	Copper temp (2CM, TP4)(℃)
1oz	Without heatsink	300.2	20	137	26.1	50.4	45.5	39.4	36.2
		300.2	30	181	26.2	58.5	50.8	43.8	40.5
		300.2	40	223	26.4	70.4	58.1	50	45.1
		300.2	50	257	25.1	79.4	66.9	54.3	47.6
		300.5	60	291	25.6	99.2	81.4	64.1	54.2
	With heatsink	300.7	20	135	25.5	44.4	44.3	38.8	37
		300.7	30	178	25.7	50.2	49.1	42.4	39.1
		300.7	40	220	25.7	57.3	55.9	46.5	41.9
		300.7	50	258	25.6	65.8	63.7	51.4	45.1
		300.5	60	294	23.5	73.4	66.1	55	47.2
		300.5	70	323	24.2	87	76.8	62.4	52.6
		300.5	80	348	24.3	102	98	73.3	58.3
	Cooling fan	300.1	20	137	22.9	34.5	31.5	26.7	25.5
		300.2	30	180	23.6	38.5	35	28.2	26.5
		300.2	40	222	24	43.7	38.8	29.7	27.7
		300.2	50	258	24.4	48.3	43.3	31.4	28.8
		300.2	60	296	24.4	55.4	49.8	33.7	29.8
		300.2	70	328	24.5	62.3	55.3	35.3	30.8
		300.1	80	355	23.1	69.1	60.1	36.1	29.9
2oz	Without heatsink	300.3	20	134	23.8	43.6	41.9	37.8	36.3
		300.3	30	176	24.3	47.3	46.7	41.3	38.9
		300.3	40	221	24.4	55.7	54.2	47.2	42.9
		300.3	50	258	24.2	65.1	62	53.4	46.8
		300.3	60	292	24.6	77.4	71.6	60.5	51.4
		300.3	70	322	24.9	89.8	82.5	65.3	57.2
	With heatsink	300.3	20	134	25.5	42.2	41.7	38.6	37.5
		300.3	30	178	25.4	46.6	46.1	41.8	39.9
		300.3	40	221	25.2	51.7	50.4	45.4	42.4
		300.2	50	258	22.6	56.4	53.5	47	43.5
		300.2	60	296	23.7	65.3	61.9	53	48.2
		300.2	70	326	24.2	75.5	69.5	58.9	53
		300.2	80	358	24.4	84.2	77.5	64.2	56.6
	Cooling fan	300.3	20	134	25.6	35.1	31.8	29.4	28.8
		300.3	30	177	26.2	38.4	34.2	31	30.1
		300.3	40	220	26.4	42.2	36.5	32.2	30.8
		300.3	50	258	26.8	45.8	38.9	33.4	31.5
		300.3	60	298	26.6	50.7	43	34.7	32.1
		300.3	70	330	26.6	55.8	46.6	36.3	33.1
		300.2	80	358	26.2	62	49.8	37.8	33

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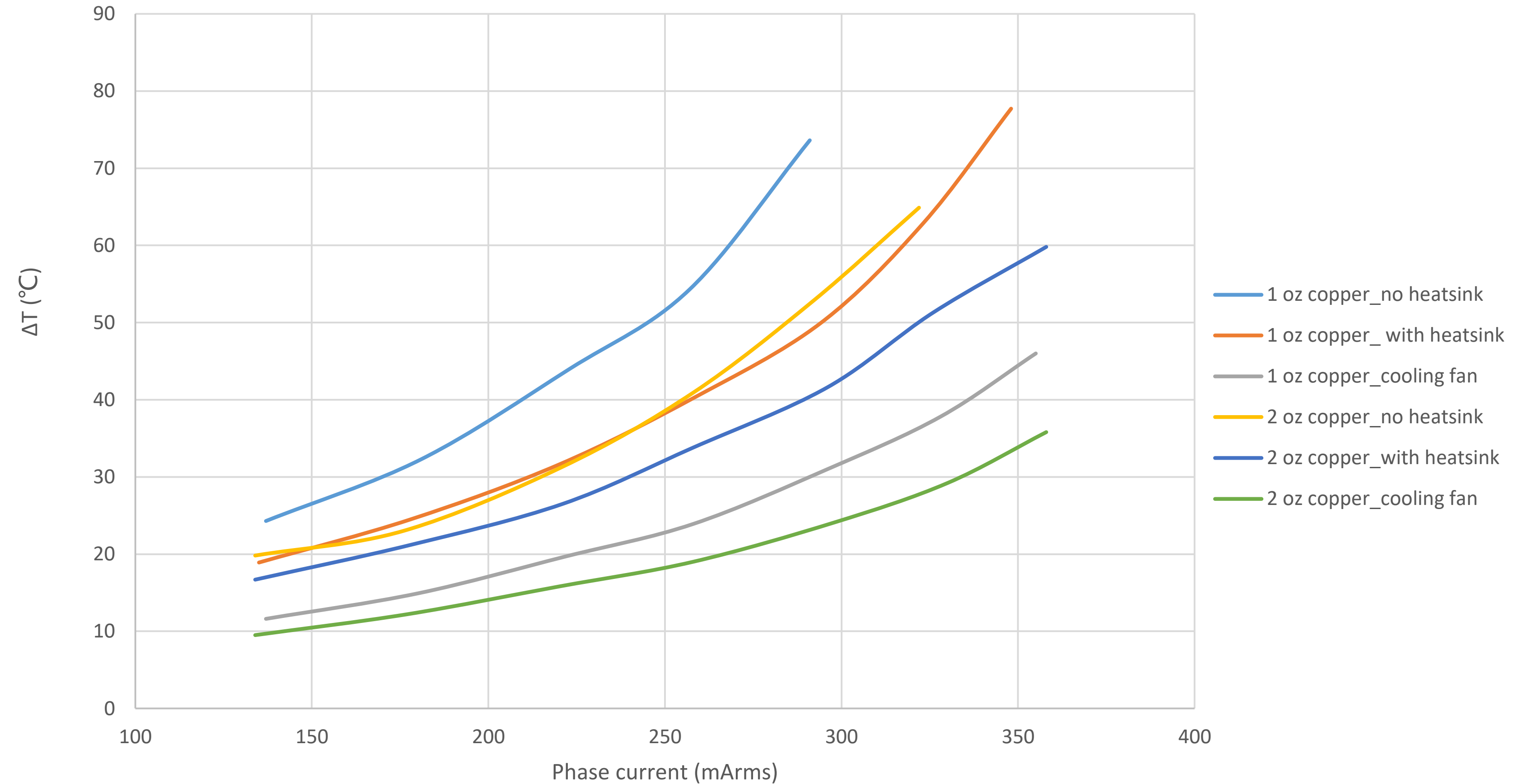
Example : Thermal test

- EVAL-IMM101T-015 R1.0 Board:
- PWM: 10kHz
- Vbus voltage:300Vdc
- Ta: 24 ℃
- Load: fan
- Cooling fan: 12Vdc, 0.11A



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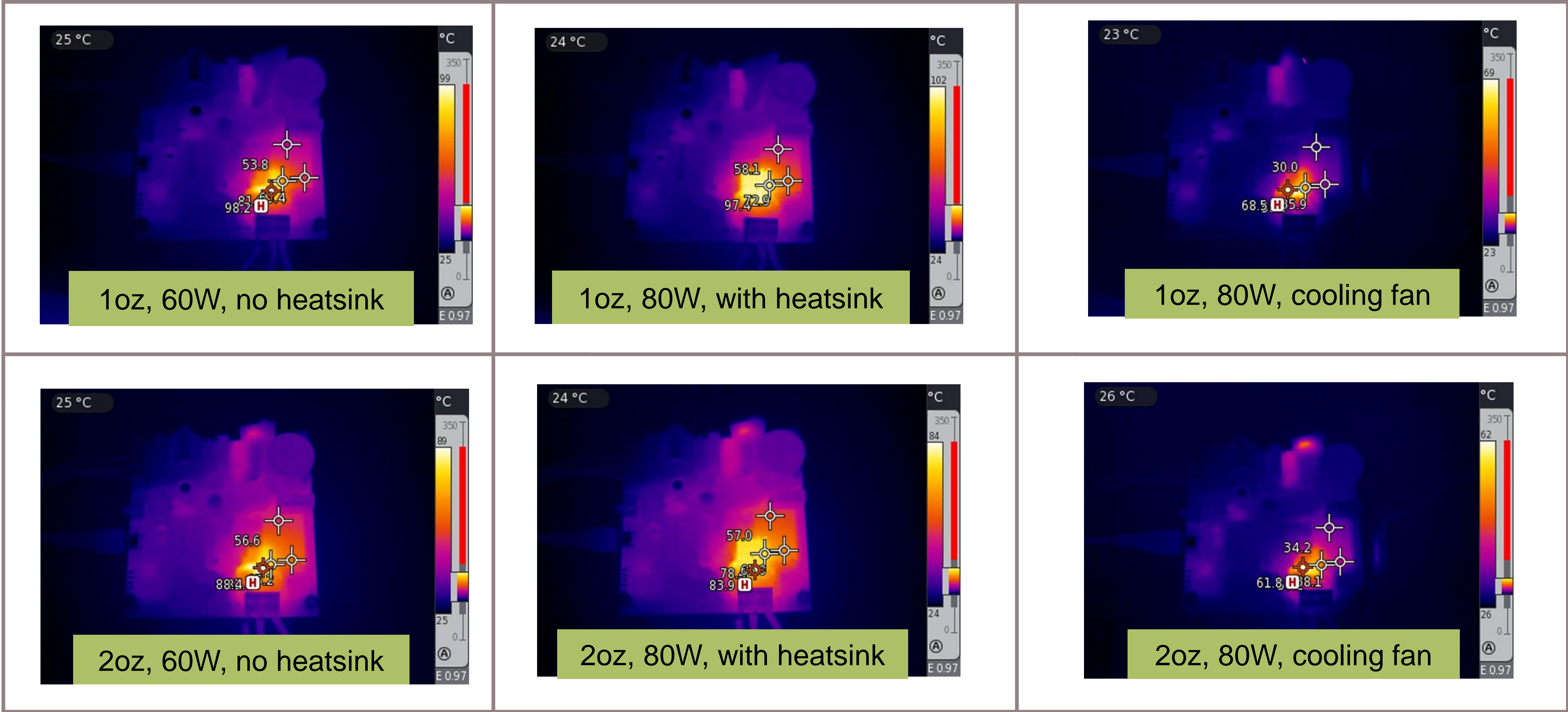
IR camera photo



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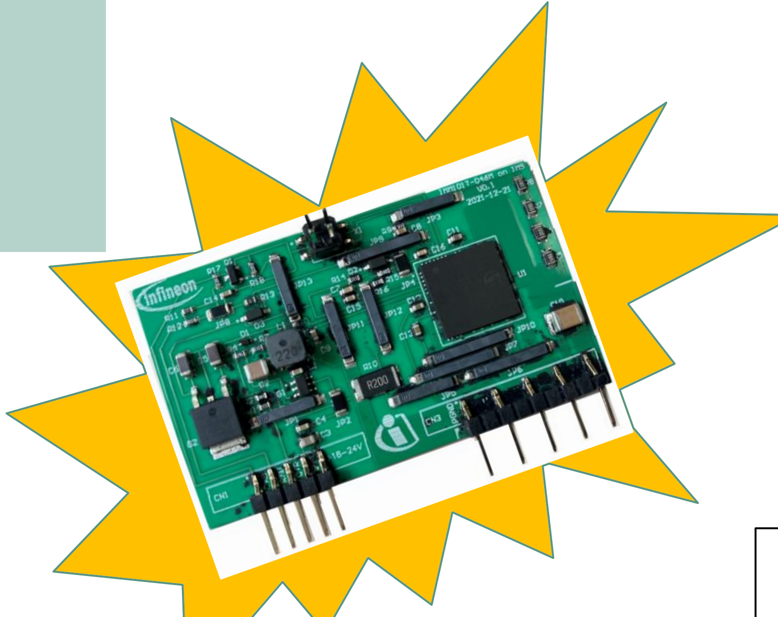
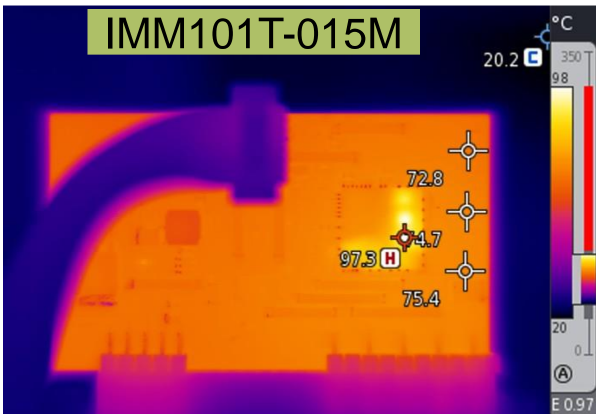
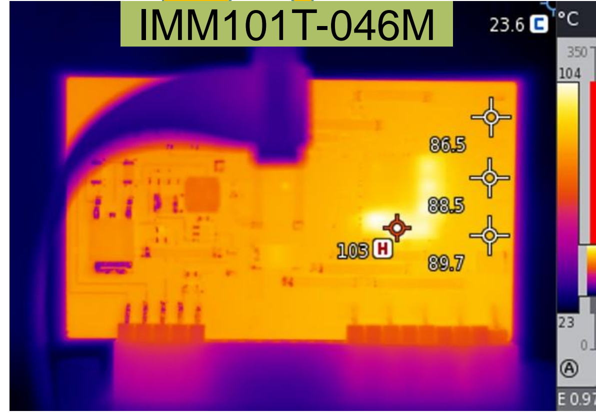
Example: thermal test with IMS board(Aluminum substrate)

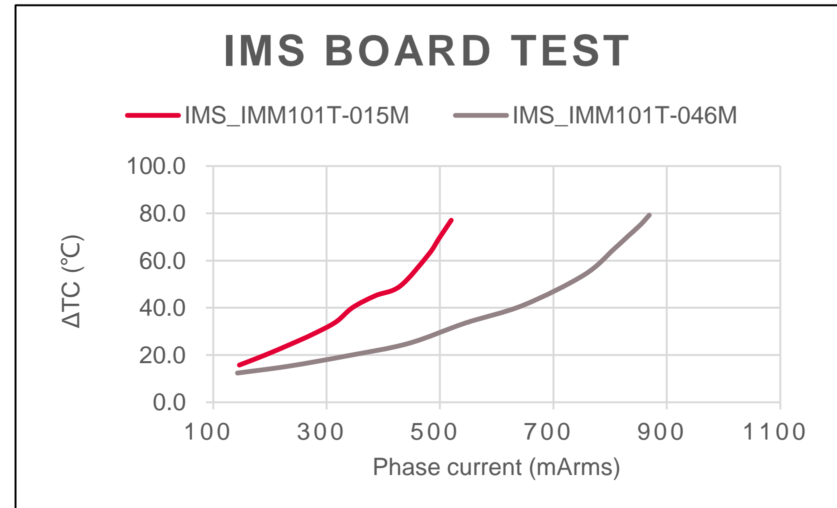
- EVAL-IMS Board
- PWM: 10kHz
- Vbus voltage:300Vdc
- Load: GK6040
- Aluminum substrate thickness: 1.6mm



IMM101T-015M			IMM101T-046M		
Phase current(mA)	Ta (℃)	Case temp (℃)	Phase current(mA)	Ta (℃)	Case temp (℃)
146	18.4	34.1	143	21.4	33.8
192	18.1	38.1	233	21.7	37.0
237	17.7	42.3	337	21.6	41.3
275	17.5	46.2	444	20.6	45.5
316	17.6	51.5	544	20.1	53.6
346	17.1	57.2	647	22.3	63.4
386	17.3	62.4	754	23.3	77.2
430	20.6	69.8	807	23.8	88.7
480	20.4	83.0	831	24.2	94.4
498	20.5	89.7	853	24.0	99.0
520	20.2	97.3	869	23.8	103.0







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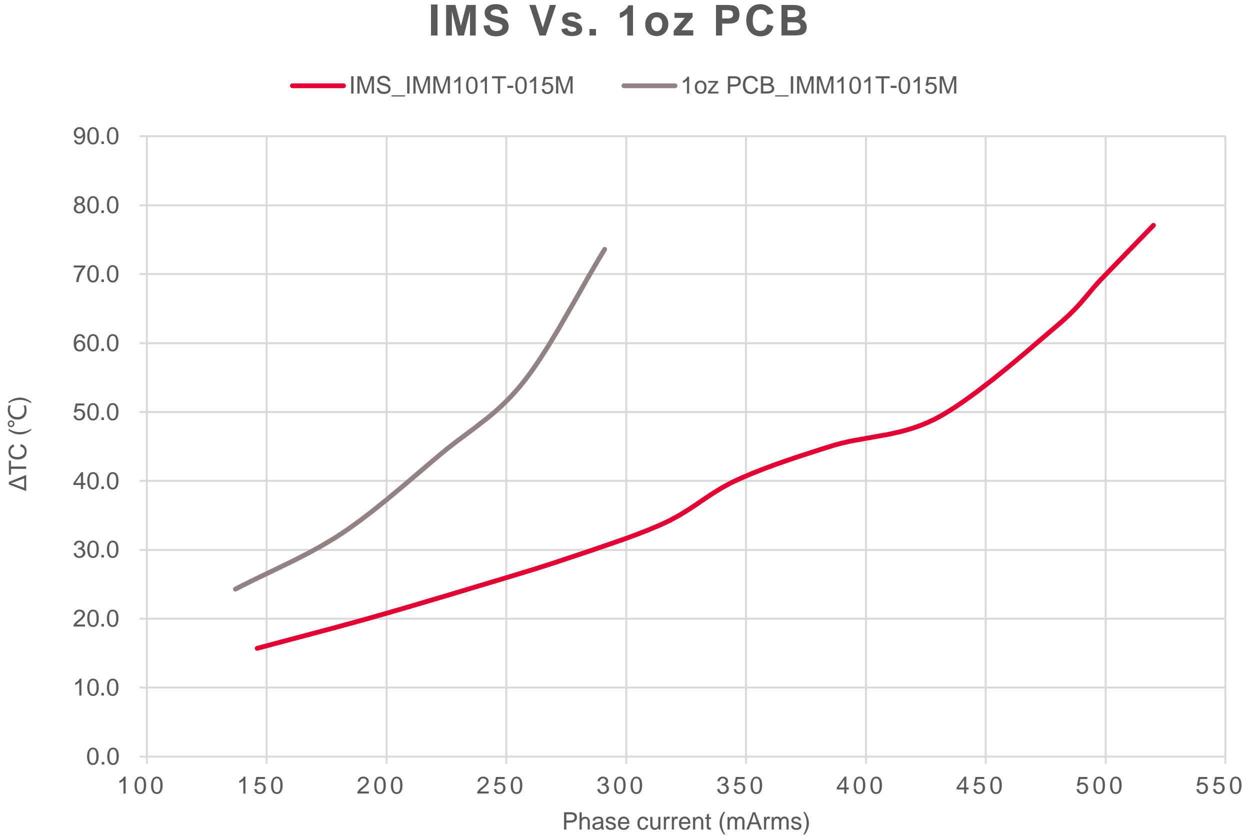
IMM101T-015M output current capability on the IMS and PCB board

- PCB board:1oz, 1.6mm, FR4
- IMS board: 1.6mm Al substrate, 1oz copper
- PWM: 10kHz
- Vbus voltage:300Vdc
- Ta: 24 ℃,
- Load: fan
- Cooling: w/o heatsink or cooling fan



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3. Stencil design 16
   - Dividing large pads into smaller blocks
   - Vias selection for dual layer copper board
4. Reflow temperature profile 20

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PQFN package stencil design guide

➢ AN1168 - PQFN IPM board mounting application note

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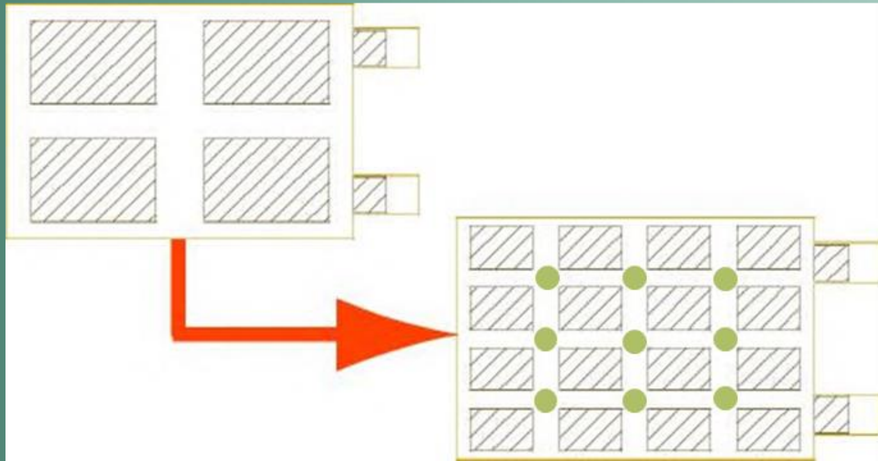
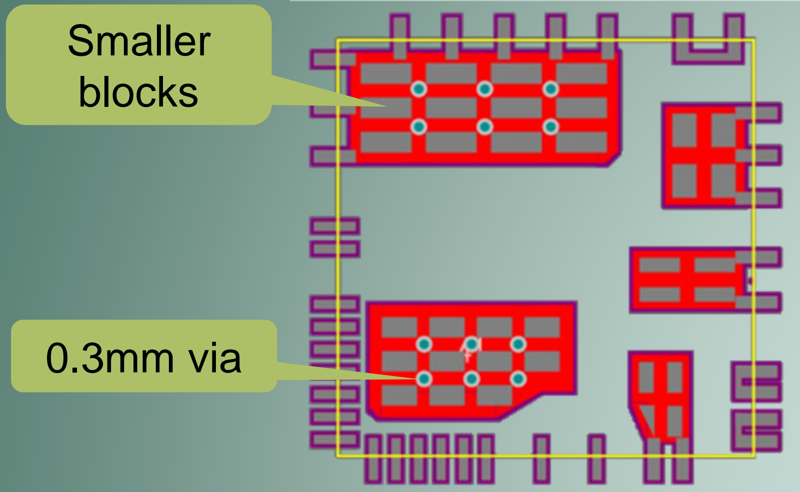
Stencil design and recommend Altium Designer PCB library





- Dividing larger pads into smaller blocks
- Place via in between smaller blocks or cross

- Recommend Altium Designer PCB library

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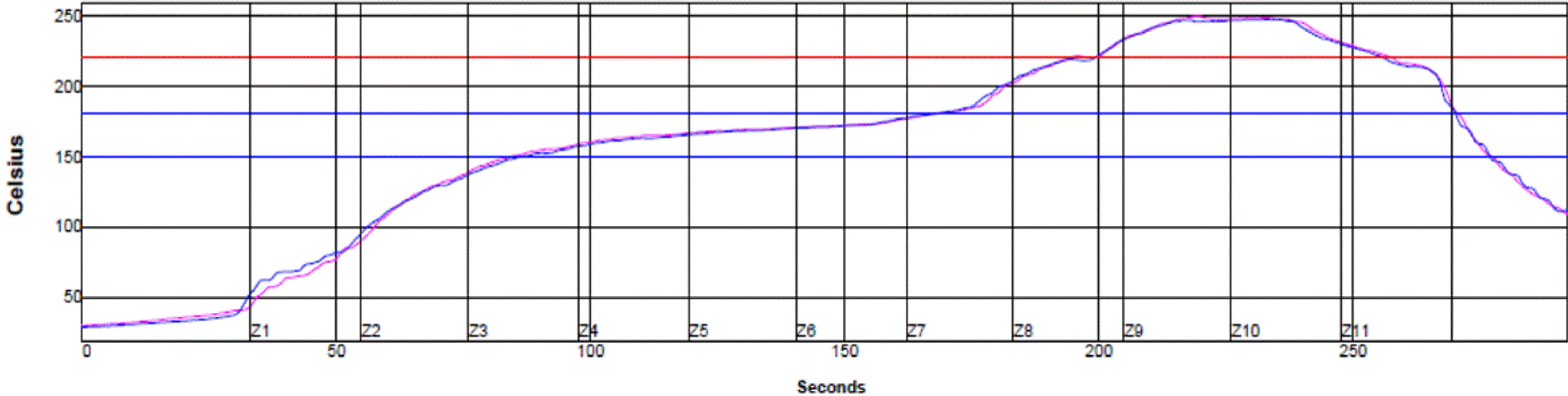
Recommend reflow temperature profile



Setpoints (Celsius)

Zone	1	2	3	4	5	6	7	8	9	10	11
Top	120.0	170.0	175.0	175.0	175.0	175.0	195.0	250.0	270.0	250.0	200.0
Bottom	120.0	170.0	175.0	175.0	175.0	175.0	195.0	250.0	270.0	250.0	200.0

Conveyor Speed (cm/min): 95.00

PWI= 122%	Soak Time 150-180C		Reflow Time /220C		Peak Temp		Slope1		Slope2		Slope3	
TC1	82.9	-24%	63.3	122%	249.5	95%	3.0	19%	1.7	-2%	-4.8	-53%
TC2	80.6	-31%	56.7	78%	247.5	75%	2.8	1%	1.7	-3%	-4.8	-52%
Delta	2.3		6.6		2.0		0.2		0.0		0.0	

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Back up slides show the test details for different stencil design

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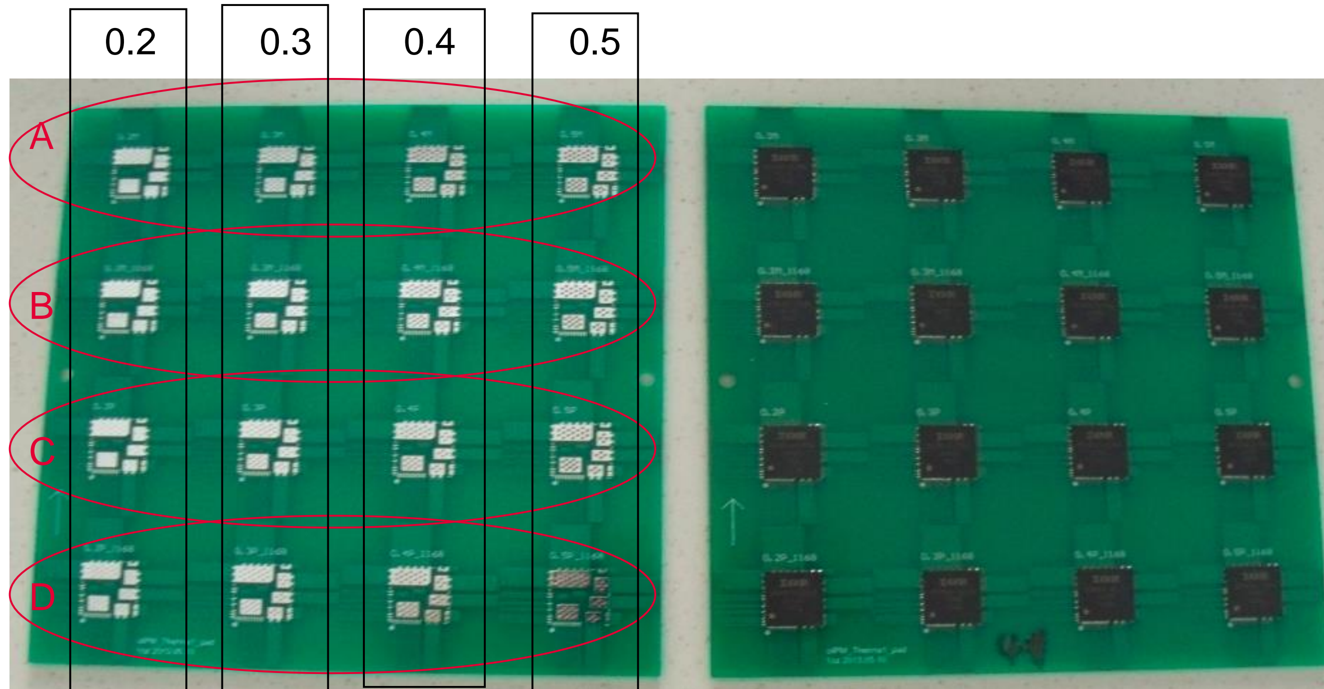
PCB design for PQFN package soldering test



PCB: HASL

Solder: Senju M705-GRN360-K2-V

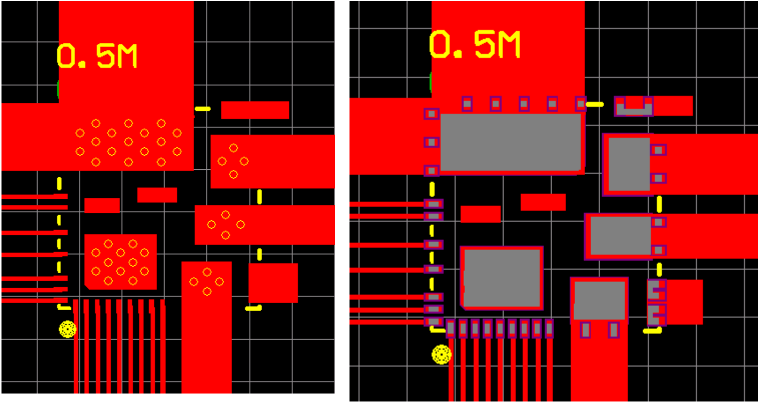
A: mechanical hole diameter:0.2~0.5mm. Without large pad dividing to small blocks

B: mechanical hole diameter:0.2~0.5mm. large pad dividing to small blocks.

C: Through-hole pad(Via) diameter:0.2~0.5mm. Without large pad dividing to small blocks:

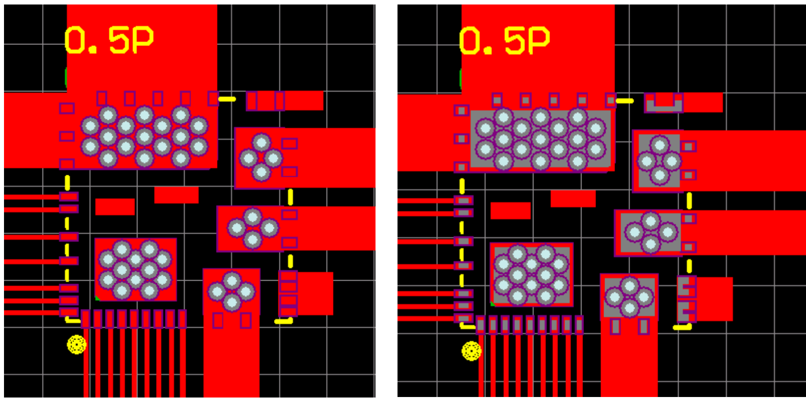
D: Through-hole Pad(via) diameter:0.2~0.5mm. large pad dividing to small blocks.

About Pattern A/B/C/D layout



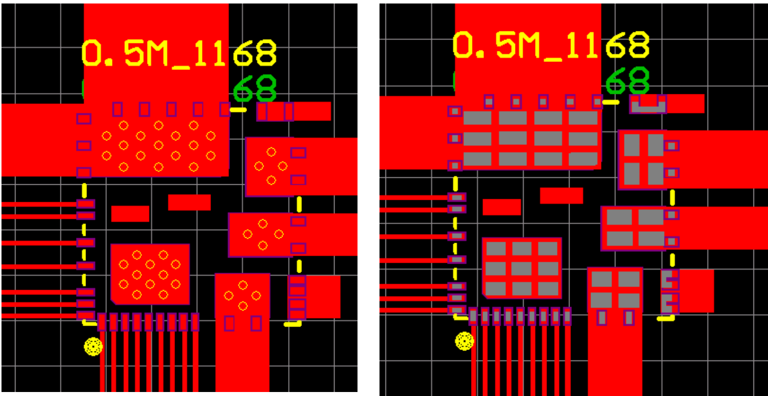
Pattern A layout.

The yellow circle is hole on the SMT Pad.



Pattern C layout.

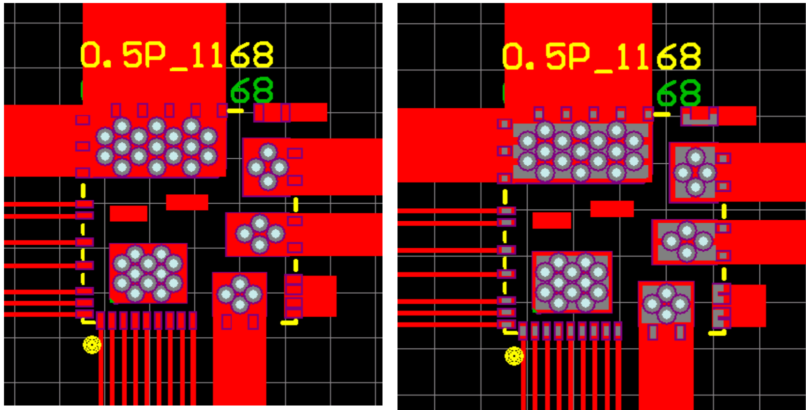
The purple circle is through-hole Pad(via) on the SMT Pad.



Pattern B layout.

The yellow circle is hole between small solder pad.

Refer to AN1168 recommended stencil design



Pattern D layout.

The purple circle is through-hole Pad(via) between small solder pad.

Refer to AN1168 recommended stencil design

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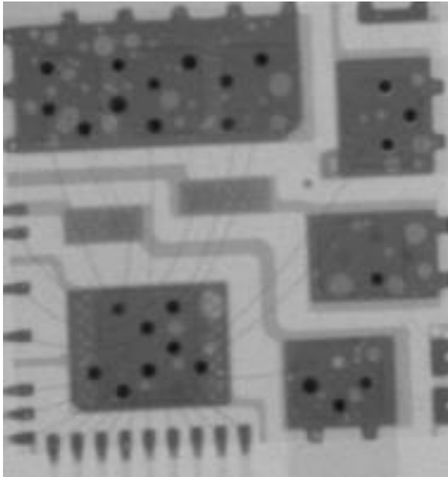
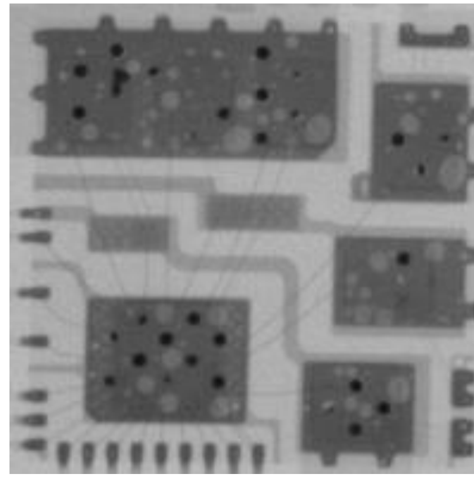
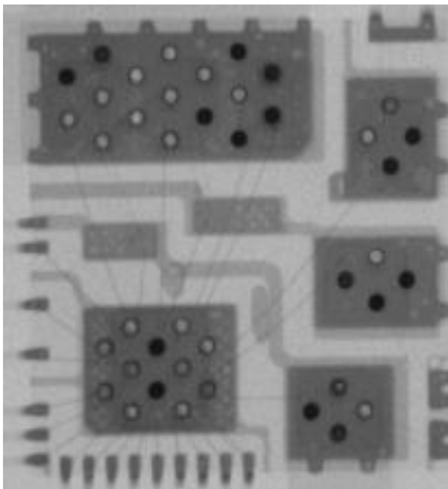
X3-ray result



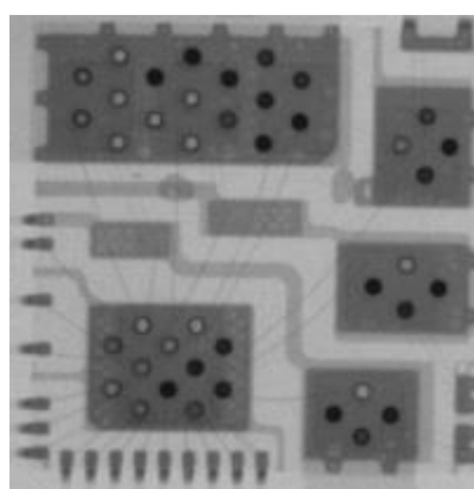
Pattern A: 0.3mm



Pattern B: 0.3mm



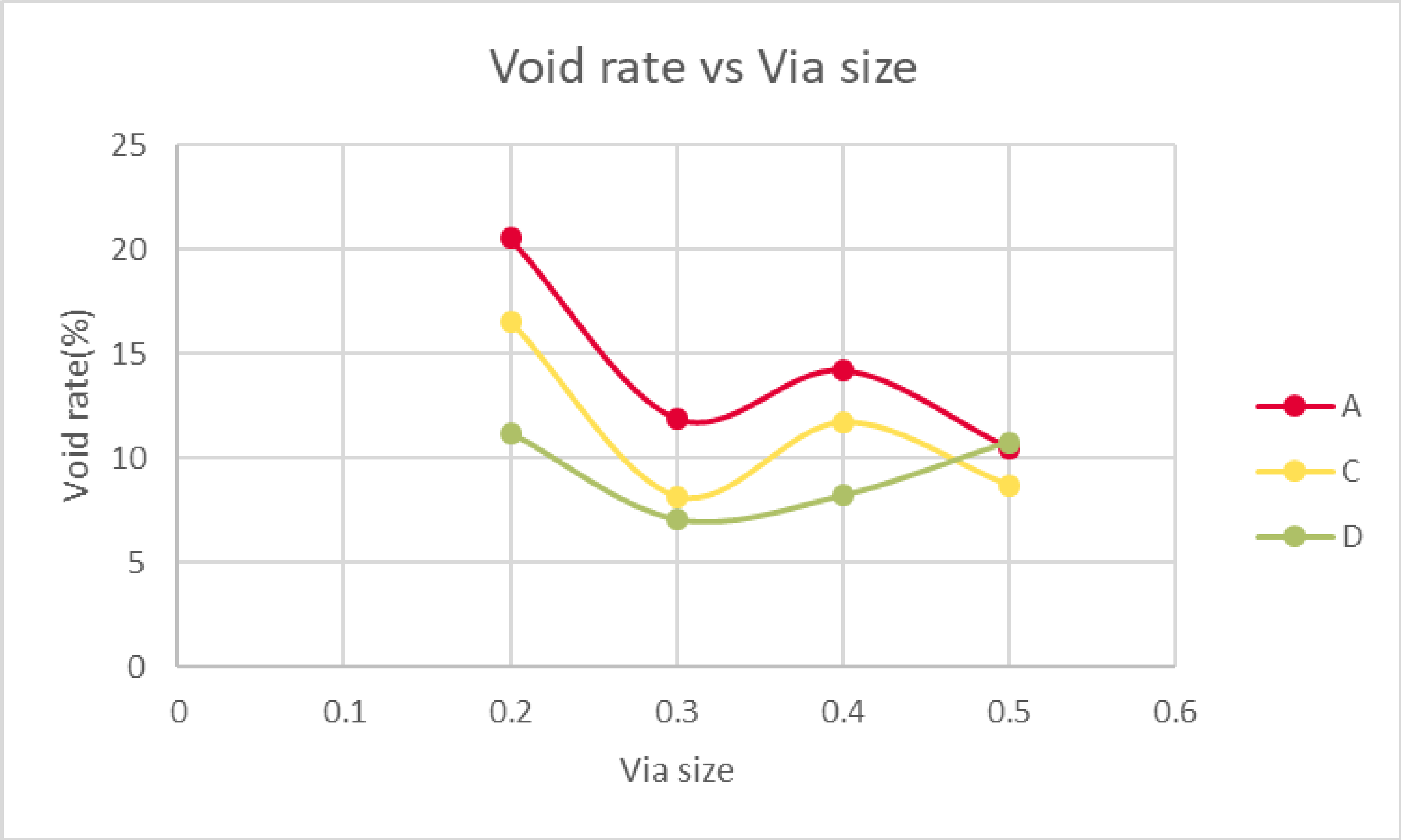
Pattern C: 0.3mm



Pattern D:0.3

The lowest void rate is achieved by using pattern D: divided bigger pad to several smaller blocks with 0.3mm via.

Voids test data



0.3 via has lowest void rate

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